

# Murata Power Solutions OBSOLETE PRODUCT 8-Bit, 50MI z Video A/D Converter

**Contact Factory for Replacement Model** 

### **FEATURES**

- Low power dissipation (180mW max.)
- Input signal bandwith (100MHz)
- Optional synchronized clamp function
- Low input capacitance (15pF typ.)
- +5V or +5V /+3.3V power supply operation
- Differential nonlinearity (±½LSB max.)
- Optional self-biased reference
- CMOS/TTL compatible inputs
- Outputs 3-state TTL compatible
- Surface mount package

### **PRODUCT OVERVIEW**

The ADC-321 is an 8-bit, high speed, monolithic CMOS, sub-ranging A/D converter. The ADC-321 achieves a sampling rate comparable to flash converters by employing a sub-ran single +5V or dual +5V and +3.3V power source to allow easy interfacing with 3.3V logic.

An optional synchronous clamp function useful for video signal processing is provided. The ADC-321 is well suited for the portable video signal processors due to its low 125mW typical power dissipation. The ADC-321 also features ±0.5 LSB max. differential non-linearity, a self bias function that can eliminate the need for external references, SNR with THD of 45dB, a small 32-pin QFP package and an operating temperature range of -40 to +85°C

INPUT/OUTPUT CONNECTIONS			
Pin	Function	Pin	Function
1	BIT 8 (LSB)	32	NO CONNECTION
2	BIT 7	31	DIGITAL GROUND (DGND)
3	BIT 6	30	OUTPUT ENABLE (OE)
4	BIT 5	29	CLAMP ENABLE (CLE)
5	BIT 4	28	DIGITAL GROUND (DGND)
6	BIT 3	27	CLAMP CONTROL (COP)
7	BIT 2	26	CLAMP REF. (VREF)
8	BIT 1 (MSB)	25	REF. BOTTOM SENSE (VRBS)
9	TEST	24	REF. BOTTOM (VRB)
10	+DVS (Digital)	23	ANALOG GROUND (AGND)
11	TEST	22	ANALOG GROUND (AGND)
12	A/D CLOCK	21	ANALOG IN (VIN)
13	NO CONNECTION	20	+AVS (Analog)
14	NO CONNECTION	19	+AVS (Analog)
15	CLAMP IN (CLP)	18	REF. TOP (VRT)
16	+AVS (Analog)	17	REF. TOP SENSE (VRTS)

		7
+AVs 16		30 OUTPUT ENABLE
VRTS 17		31 DGND
VRT 18		1 BIT 8 (LSB)
	Reference 4-Bit 4-Bit Lower	2 BIT 7
+AVs 19	Supply Sampling Lower Data Comparator Encoder Latch	3 BIT 6
+AVs 20	B B	4 BIT 5
Vin 21		
AGND 22		
4040 00	4-Bit 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	5 BIT 4
AGND 23	Clock Upper Sampling 4-Bit Upper Data	- 6 BIT 3 - 7 BIT 2
V <sub>RB</sub> 24	Comparator Encoder Latch	8 BIT 1 (MSB)
\/ o=		To Bit I (WSB)
VRBS 25		12 A/D CLOCK
		12 A/D CLOCK
VREF 26	+ D-FF	- 15 CLAMP IN
DGND 28		9 TEST (Open)
CONTROL 27		10 +DVs
MP ENABLE 29	<u> </u>	11 TEST (Open)
IP ENABLE 29	- ///	
		<b>_</b>





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### **ABSOLUTE MAXIMUM RATINGS** (TA = +25°C)

PARAMETERS	LIMITS	UNITS
Power Supply Voltage (+AVs, +DVs)	-0.5 to 7	Volts
Analog Input Voltage, (VIN)	-0.5 to $+AVs + 0.5$	Volts
Reference Input Voltage (VRT, VRB)	-0.5 to +AVs + 0.5	Volts
Digital Input Voltage (VIH, VIL)	-0.5 to $+AVs + 0.5$	Volts
Digital Output Voltage (VOH, VOL)	-0.5 to +DVs + 0.5	Volts

### **FUNCTIONAL SPECIFICATIONS**

Typical at Ta =  $25^{\circ}$ C, VRT = +2.5V, VRB = +0.5V, +AVs = +5V, +DVs = +3V to +5.5V, Fs = 50MHz unless otherwise specified.

Input Capacitance	ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
(@ Vin = +1.5Vdc +0.07VRMS)   Input Signal Bandwidth		+0.5	_	+2.5	Volts
-1dB (@ Rin = 33Ω)	(@ $VIN = +1.5Vdc +0.07VRMS$ )	_	15	_	pF
REFERENCE INPUTS		_	60	_	MHz
Reference Resistance	,	_	100	_	
VRT - VRB   Reference Current   4.1   5.4   7.7   mA	REFERENCE INPUTS	1		<u>I</u>	ı
Reference Current Reference Voltage  VRT VRB  VRB  VRB  VRB  VRB  VRB  VRB	Reference Resistance				
Neference Voltage   VRT	VRT – VRB	260	370	480	Ω
VRT         VRB         —         —         +2.7         Volts           VRB         0         —         —         Volts           Self Bias Voltage ②         —         1.7         —         —         Volts           Self Bias Voltage ②         +0.52         +0.56         +0.60         Volts         Volts           I/NT – VRel         1.80         1.92         2.04         Volts           Capacitance (VRT, VRTS, VRB, VRBS)         —         —         11         pF           Offset Voltage         —         —         —         11         pF           Offset Voltage         —         —         —         11         pF           DIGITAL INPUTS         —         —         —         —         —         Volts         mV           DIGITAL INPUTS         —         —         —         —         —         —         Volts         np         —         —         —         —         Volts         np         —         —         —         —         Volts         np         —         —         —         —         —         Volts         np         —         —         —         —         — <td>Reference Current</td> <td>4.1</td> <td>5.4</td> <td>7.7</td> <td>mA</td>	Reference Current	4.1	5.4	7.7	mA
VRT         VRB         —         —         +2.7         Volts           VRB         0         —         —         Volts           Self Bias Voltage ②         —         1.7         —         —         Volts           Self Bias Voltage ②         +0.52         +0.56         +0.60         Volts         Volts           I/NT – VRel         1.80         1.92         2.04         Volts           Capacitance (VRT, VRTS, VRB, VRBS)         —         —         11         pF           Offset Voltage         —         —         —         11         pF           Offset Voltage         —         —         —         11         pF           DIGITAL INPUTS         —         —         —         —         —         Volts         mV           DIGITAL INPUTS         —         —         —         —         —         —         Volts         np         —         —         —         —         Volts         np         —         —         —         —         Volts         np         —         —         —         —         —         Volts         np         —         —         —         —         — <td>Reference Voltage</td> <td></td> <td></td> <td></td> <td></td>	Reference Voltage				
VRT − VRB    1.7	•	_	_	+2.7	Volts
Self Bias Voltage ②           VRB         +0.52         +0.56         +0.60         Volts           IVRT − VRid         1.80         1.92         2.04         Volts           Capacitance (VRT, VRTS, VRBS, VRBS)         —         —         11         pF           Offset Voltage         VRT         —70         —50         —30         mV           VRB         20         40         60         mV           DIGITAL INPUTS           Logic Levels ③           Input Voltage "1"         2.2         —         —         Volts           Input Current ④         A/D CLK         —240         —         240         µA           A/D CLK         —240         —         240         µA           Input Capacitance         —         —         —         11         pF           A/D Clock Pulse Width         (tpw1)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤         —         —         —         —         —         —         mA           Output Current (OE = 0V) ⑤         —	VRB	0	_	_	Volts
Self Bias Voltage ②           VRB         +0.52         +0.56         +0.60         Volts           IVRT − VRid         1.80         1.92         2.04         Volts           Capacitance (VRT, VRTS, VRBS, VRBS)         —         —         11         pF           Offset Voltage         VRT         —70         —50         —30         mV           VRB         20         40         60         mV           DIGITAL INPUTS           Logic Levels ③           Input Voltage "1"         2.2         —         —         Volts           Input Current ④         A/D CLK         —240         —         240         µA           A/D CLK         —240         —         240         µA           Input Capacitance         —         —         —         11         pF           A/D Clock Pulse Width         (tpw1)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤         —         —         —         —         —         —         mA           Output Current (OE = 0V) ⑤         —	VRT – VRB	1.7	_	_	Volts
VRB  VRT − VRel         +0.52 1.80         +0.56 1.92         +0.60 2.04         Volts Volts Volts Polts           Capacitance (VRT, VRTS, VRB, VRBS) Offset Voltage VRT VRB         −70 20         −50 40         −30 60         mV           DIGITAL INPUTS           Logic Levels ③ Input Voltage "1" Input Voltage "0"         −         −         −         Volts Volts           Input Current ④ A/D CLK CLP, CLE         −240         −         240         µA           Input Capacitance A/D Clock Pulse Width (tpw1) (tpw0)         −         −         11         pF           A/D Clock Pulse Width (tpw0)         10         −         −         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤ (@ +DVs = +3.3V) "1"	·				
VRT − VRE  Capacitance (VRT, VRTS, VRB, VRBS)   Diffset Voltage   VRT		+0.52	+0.56	+0.60	Volts
Capacitance (VRT, VRTS, VRB, VRBS)         —         —         —         111         pF           Offset Voltage         VRT         —					
Offset Voltage         VRT         -70         -50         -30         mV           DIGITAL INPUTS           Logic Levels ③         Input Voltage "1"         2.2         —         —         Volts           Input Voltage "0"         —         —         +0.8         Volts           Input Current ④         A/D CLK         —         240         —         40         µA           A/D CLK         —         240         —         40         µA           Input Capacitance         —         —         11         pF           A/D Clock Pulse Width (tpw1) (tpw0)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤         —         —         —         —         —         mA           Output Current (OE = 0V) ⑥         —         —         —         —         —         mA           Output Current ⑥         —         —         —         —         —         —         —         —         —         —         —         —         <	· · · · · · · · · · · · · · · · · · ·		1.52		
VRT VRB         -70 20         -50 40         -30 60         mV           DIGITAL INPUTS           Logic Levels ③ Input Voltage "1" Input Voltage "0"         2.2         —         —         Volts Volts           Input Current ④ A/D CLK CLP, CLE OE         -240         —         240         µA           CLP, CLE OE         -240         —         40         µA           Input Capacitance A/D Clock Pulse Width (tpw1) (tpw0)         —         —         11         pF           A/D Clock Pulse Width (tpw0)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤ (@ +DVs = +5V) "1" "0"         —         —         —         —         —         mA           Output Current (OE = 0V) ⑥ (@ +DVs = +3.3V) "1" "0"         —         —         —         —         —         —         mA           Output Current ©         —         —         —         —         —         —         —         —         —         mA           Output Current ©         —         —         —         —         —         —         —         —         —         —         —         —<		) <sub> </sub> –	_	11	þг
VRB         20         40         60         mV           DIGITAL INPUTS           Logic Levels ③         Input Voltage "1"         2.2         —         —         Volts           Input Voltage "0"         —         —         +0.8         Volts           Input Current ④         A/D CLK         —240         —         240         µA           CLP, CLE         —240         —         240         µA           Input Capacitance         —         —         11         pF           A/D Clock Pulse Width (tpw1) (tpw0)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤         ⑥         —         —         —         —         mA           Output Current (OE = 0V) ⑤         ⑥         —         —         —         —         —         mA           Output Current (OE = 0V) ⑤         ⑥         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         MA         Output Supplies         —	<u> </u>	70	E0	20	m\/
DIGITAL INPUTS   Logic Levels ③	****	-			
Logic Levels ③         Input Voltage "1"         2.2         —         —         Volts           Input Voltage "0"         —         —         +0.8         Volts           Input Current ④         —         —         +0.8         Volts           Input CLK         —         —         240         —           A/D CLK         —         —         40         —           Input Capacitance         —         —         —         11         pF           A/D Clock Pulse Width (tpw1)         10         —         —         ns         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Digital Current (OE = 0V) ⑤         —         —         —         —         mA           Output Current (OE = 0V) ⑤         —         —         —         —         mA           Output Current (OE = 0V) ⑤         —         —         —         —         —         mA           Output Current (OE = 0V) ⑤         —         —         —         —         —         —         —         —         —         —         —         —         —         MA         —         —         —         —         <	VRB	20	40	60	mv
Input Voltage "1"   2.2	DIGITAL INPUTS		1	1	
Input Voltage "0"					
Input Current ⊕		2.2	_	_	Volts
A/D CLK CLP, CLE OE OE OE A/D Clock Pulse Width (tpw1) (tpw0) DIGITAL OUTPUTS  C(@ +DVs = +5V) Output Current (OE = 0V) (@ +DVs = +3.3V) Output Current (ΘΕ OUTPUTS  -240 -40 -40 -40 -40 -40 -40 -40 -40 -40 -		_	_	+0.8	Volts
CLP, CLE         -240         -         40         μA           Input Capacitance         -40         -         240         μA           A/D Clock Pulse Width (tpw1) (tpw0)         10         -         -         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) (@ +DVs = +5V)         "1"         -         -         -2         mA           Output Current (OE = 0V) (@ +DVs = +3.3V)         "1"         -         -         -         -1.2         mA           Output Current (© = 0V) (@ +DVs = +3.3V)         "0"         2.4         -         -         mA           Output Current (© = 0V) (@ +DVs = +3.3V)         "0"         2.4         -         -         mA	Input Current ④				
CLP, CLE         -240         -         40         µA           Input Capacitance         -40         -         240         µA           Input Capacitance         -         -         11         pF           A/D Clock Pulse Width (tpw1)         10         -         -         ns           Itpw0)         10         -         -         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) (® (@ +DVs = +5V) "1" 2 mA         mA         -         -         mA           Output Current (OE = 0V) (® +DVs = +3.3V) "1"1.2 mA         mA         -         -         mA           Output Current (®         -         -         -         -         mA	A/D CLK	-240	_	240	μΑ
OE         -40         —         240         μA           Input Capacitance         —         —         11         pF           A/D Clock Pulse Width (tpw1) (tpw0)         10         —         —         ns           Item (tpw0)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) (@ +DVs = +5V)         "1"         —         —         —         2         mA           Output Current (OE = 0V) (@ +DVs = +3.3V)         "1"         —         —         —         —         mA           Output Current (@         —         —         —         —         mA           Output Current (@         —         —         —         —         mA	CLP. CLE	-240	_	40	
Input Capacitance	·	-	_	240	
A/D Clock Pulse Width (tpw1) (tpw0)         10         —         —         ns ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) (© + DVs = +5V)         "1"         —         —         —2         mA           Output Current (OE = 0V) (© + DVs = +3.3V)         "1"         —         —         —1.2         mA           Output Current (© De + DVs = +3.3V)         "0"         2.4         —         —         mA           Output Current (© De + DVs = +3.3V)         "0"         2.4         —         —         mA           Output Current (© De + DVs = +3.3V)         "0"         2.4         —         —         mA		1	l _	-	
(tpw1) (tpw0)         10		1	i		۲,
(tpw0)         10         —         —         ns           DIGITAL OUTPUTS         MIN.         TYP.         MAX.         UNITS           Output Current (OE = 0V) ⑤         —         —         —         —         —         mA           Output Current (OE = 0V) ⑥         —         —         —         —         mA           Output Current ⑥         —         —         —         —         mA           Output Current ⑥         —         —         —         mA					
DIGITAL OUTPUTS  MIN. TYP. MAX. UNITS  Output Current (OE = 0V) ⑤ (@ +DVS = +5V) "1"		10	_		ne
Output Current (OE = 0V) (S)         (@ +DVs = +5V)       "1"       —       —       —       —       mA         Output Current (OE = 0V) (S)       —       —       —       —       —       MA         Output Current (S)	(tpw1)			_	-
(@ +DVs = +5V) "1" — — — —2 mA "0" 4 — — mA Output Current (OE = 0V) (S) (@ +DVs = +3.3V) "1" — — — —1.2 mA "0" 2.4 — — mA Output Current (S)	(tpw1) (tpw0)	10	_ _ TYP	— — MAY	ns
	(tpw1) (tpw0) DIGITAL OUTPUTS	10	- TYP.	MAX.	-
	(tpw1) (tpw0)  DIGITAL OUTPUTS  Output Current (OE = 0V) ⑤	10	- TYP.		ns UNITS
(@ +DVs = +3.3V) "1"	(tpw1) (tpw0)  DIGITAL OUTPUTS  Output Current (OE = 0V) (® (@ +DVs = +5V) "1"	10 MIN.			ns UNITS mA
"0" 2.4 — mA  Output <u>Cu</u> rrent ©	(tpw1) (tpw0)  DIGITAL OUTPUTS  Output Current (\overline{OE} = 0V) \( \bigsimes \) (@ +DVs = +5V) "1" "0"	10 MIN.			ns UNITS mA
Output Current ®		10 MIN.	_  TYP.	-2 -	ns UNITS mA
· · · · · —		10 MIN.		-2 -	ns UNITS  mA mA
· —	$(tpw1) \\ (tpw0) \\ \hline \textbf{DIGITAL OUTPUTS} \\ \hline \textbf{Output Current } (\overline{OE} = 0V) & \\ (@ +DVS = +5V) & "1" \\ "0" \\ \hline \textbf{Output Current } (\overline{OE} = 0V) & \\ (@ +DVS = +3.3V) & "1" \\ \hline \end{tabular}$	10 MIN. — 4		-2 -	mA mA
(@ OE = $+3V$ ) "1" $-40$ — 40 $\mu$ A	$(tpw1) \\ (tpw0) \\ \hline \textbf{DIGITAL OUTPUTS} \\ \hline \textbf{Output Current } (\overline{OE} = 0V) \\ (@ +DVS = +5V) \\ "1" \\ "0" \\ \hline \textbf{Output Current } (\overline{OE} = 0V) \\ (@ +DVS = +3.3V) \\ "1" \\ "0" \\ \hline \end{cases}$	10 MIN. — 4		-2 -	mA mA
"0" -40 — 40 µA	$(tpw1) \\ (tpw0) \\ \hline \textbf{DIGITAL OUTPUTS} \\ \hline \textbf{Output Current } (\overline{OE} = 0V) \ \ \textcircled{\$} \\ (\textcircled{@} + DVS = +5V) \qquad \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	10 MIN. — 4		-2 - -1.2	mA mA mA mA
Capacitance — 11 pF	$\begin{array}{c} \text{(tpw1)} \\ \text{(tpw0)} \\ \\ \hline \textbf{DIGITAL OUTPUTS} \\ \\ \hline \textbf{Output Current } (\overline{OE} = 0V)  \textcircled{s} \\ \text{($@+DVs=+5V$)} & \text{"1"} \\ \text{"0"} \\ \hline \textbf{Output Current } (\overline{OE} = 0V)  \textcircled{s} \\ \text{($@+DVs=+3.3V$)} & \text{"1"} \\ \text{"0"} \\ \hline \textbf{Output Current } \textcircled{s} \\ \text{($@\overline{OE}=+3V$)} & \text{"1"} \\ \\ \hline \end{array}$	10 MIN.  4		-2 - -1.2 - 40	mA mA mA mA

DIGITAL OUTPUTS	(continued)	MIN.	TYP.	MAX.	UNITS
Output Data Delay					
$(\overline{OE} = 0V, CL = 15pF)$					
(@ +DVs = +5V)	t PLH	5.5	9.5	12.0	ns
(0.12.0	t PHL	5.5	8.5	12.0	ns
(@+DVs = +3.3V)	t PLH	4.3	11.8	16.3	ns
(0.210 .0.01)	t PHL	4.3	7.6	16.3	ns
3-State Output Enable	-	1.0	7.0	10.0	110
$(RL = 1k\Omega, CL = 15pF)$					
(@ +DVs = +5V)	t PZH	2.5	4.5	8.0	ns
(8 1575 = 157)	t PZL	2.5	6.0	8.0	ns
(@+DVs = +3.3V)	t PZH	3.0	7.0	9.0	ns
(@1000 = 10.00)	t PZL	3.0	5.0	9.0	ns
3-State Output Disable	-	0.0	0.0	0.0	110
$(RL = 1k\Omega, CL = 15pF)$	Time w				
(@+DVs = +5V)	t PHZ, t PLZ	3.5	5.5	7.5	ns
,		2.5	5.5	7.5 8.0	
(@+DVs = +3.3V)	t PHZ, t PLZ	2.5	5.5	0.0	ns
CLAM CIRCUIT		•	1	1	
Clamp Offset Voltage @	)	0	20	40	mV
Clamp Pulse Width ®		1.75	2.75	3.75	μΑ
PERFORMANCE					
PERFORMANCE			<u> </u>	I	
Resolution		8	_	_	Bit
<b>Sampling Rate,</b> maximu	m, Fs	50	_	_	MHz
minimum, Fs		_	_	0.5	MHz
Aperature Delay (Tds)		_	0	_	ns
Integral Linearity Error		_	±0.7	±1.5	LSB
Diff. Linearity Error		_	±0.3	±0.5	LSB
Diff. Gain Error <sup>11</sup>		_	3	_	%
Diff. Phase Error 11		_	1.5	_	deg
S/N Ratio with THD					
(fin = 100kHz)		_	45	_	dB
(fin = 500kHz)		_	44	_	dB
(fin = 1MHz)		_	44	_	dB
(fin = 3MHz)		_	43	_	dB
(fin = 10MHz)		_	38	_	dB
(fin = 25MHz)		_	32	_	dB
Spurious Free Dynamic	: Range		0_		""
(fin = 100kHz)		_	51	_	dB
(fin = 500kHz)		_	46	l _	dB
(fin = 1MHz)		_	49	_	dB
(fin = 3MHz)		_	46	l _	dB
(fin = 10MHz)		_	45	l _	dB
(fin = 25MHz)		_	45	_	dB
POWER REQUIRE	AENTO.				
POWER REQUIRE	MENIS				1
Power Supply		. 4 75	.50	. 5 05	\/-II.
+AVs		+4.75	+5.0	+5.25	Volts
+DVs		+3.0	-	+5.5	Volts
IAGND – DGNDI	ก	0	_	100	mW
Power Supply Current					
<ol> <li>Als, Dls (@ +DVs = +</li> </ol>	-5V)	_	25	36	mA
2. Als		_	23	33	mA
DIs (@ +DVs = +3.3)	/)	_	2	3	mA
Power Dissipation			125	180	mW
ENVIRONMENTAL/	PHYSICA	L			
Operating Temp. Range	e, Case	-40	_	+85	°C
Storage Temperature F		-55	_	+150	°C
Package Type	J.		. 32-nin n	lastic QFP	
Waiaht	l		e (0.2 aram		

## Footnotes:

- See technical note 6
- ② Pin 25 tied to AGND and pin 17 tied to +AVs
- 3 + AVs = +4.75 to +5.25V and +DVs = 3 to +5.5V, full operating tem. range.
- 4 V<sub>IL</sub> = 0V and V<sub>IH</sub> = +AVs, full operating temp. range
- VOH = +DVS-0.8V and VOL = +0.4V, full operating temp. range
- 6 +DVS = +3 to +5.5V, full operating temp. range

Weight

- ⑦ OE: +3 to 0V change
- ® <del>OE</del>: 0 to +3V change
- ③ 2.75µs clamp pulse width, 14.3MHz sampling, 15.75kHz clamping rate
- 10 The clamp pulse width given is for NTSC. For other processing systems adjust the rate to the clamp pulse cycle (1/15.75kHz for NTSC) to equal the value for NTSC.

0.007 ounces (0.2 grams)

- 1 NTSC 40IRE ramp, 14.3MHz sampling
- 50MHz sampling, +AVs = +5V



### **TECHNICAL NOTES**

- The ADC-321 is a monolithic CMOS device. It should be handled carefully to prevent static charge pickup.
- It has separate power supply terminals +AVs (pins 16, 19 and 20) and +DVs (pin 10) for the internal analog and digital circuits. It is recommended that both +AVs and +DVs be powered from a single source
  - Other external digital circuits must be powered with a separate +DVs. A time lag between the two power supplies could induce latch up when power is turned on if separate supplies are used. The operating range of +DVs is from +3.0V to +5.5V and it allows the use of a common power supply with 3.3V digital systems. The +3.3V power for +DVs in this case should be taken or derived from the +AVs supply to avoid latch up. No power supply terminal should be left open.
- 3. The ADC-321 has separate grounds, the analog GND (pins 22 and 23) and digital GND (pins 28 and 31). Separate and substantial AGND and DGND ground planes are required. These grounds have to be connected to one earth point underneath the device. Digital returns should not flow through analog grounds. Connect all ground lines to the power point.
- Bypass all power lines to GND with 0.1μF ceramic chip capacitors as close to the device as possible. This is very important.
- 5. Even though the analog input capacitance is a low 15pF, it is recommended that high frequency input be provided via a high-speed buffer amplifier. A parasitic oscillation may be generated when a high-speed amplifier is used. A 33 ohm resistor inserted between the output of an amplifier and the analog input of the ADC-321 will improve the situation. Kick back noise from A/D CLOCK pulses will be observed at the analog input terminal, but this has no influence on the ADC-321 performance.
- 6. Apply +2.5V to VRT (pin 18, reference top) and 0.5V to VRB (pin 24 reference bottom) to obtain an analog input range of +0.5V to +2.5V. Conversion accuracy is dependent on stable reference voltages. Provide reference inputs via amplifiers that have enough driving power to avoid noise problems. Keep to the following equations;

$$0V \le V_{RB} \le V_{RT} \le +2.7V$$
,  $|V_{RT} - V_{RB}| \ge 1.7V$ 

The ADC-321 has a self bias function which allows the device to work without external references. Connect VRTS (pin 17, self bias top) to +AVs and VRBS (pin 25, self bias bottom) to the analog GND to obtain an analog input range of +0.56 to +2.48V. Typical voltages at VRT (pin 18) and VRB (pin

- 24) will then be +2.48V and +0.56V respectively. Under an application where this self bias function is used, the effects of temperature changes are minimal. Voltage changes of the +5V supply have direct influence on the performance of the device. The use of external references is recommended for applications sensitive to gain error, no ac signals can be used as references for this device.
- A voltage up to +AVs + 0.5V can be applied to each digital input even when +3.3V is powered to +DVs, but the digital output voltage never exceeds +DVs.
- 8. Layout A/D CLOCK pulse input (pin 12) as short as possible for minimum influence on other signals. Use of a 100 ohm series resistor is recommended to protect the device as there may be some voltage difference and turn-on-time lag on the power supplies. Analog inputs signals are sampled at the falling edge of an A/D CLOCK pulse and digital data become available at the rising edge of an A/D CLOCK pulse that is delayed by 2.5 clock cycles. The A/D CLOCK are positive pulse that have 50% duty cycle. The minimum clock pulse width is 10 nsec for both high and low levels. Keep it low level while A/D conversions are on hold.
- Digital output is 3-state. To enable 3-state outputs connect the OUTPUT ENABLE (pin 30) to GND. To disable, connect it to +DVs. The output is recommended to be latched and buffered through output registers. The device may be damaged if a voltage higher than +DVs + 0.5V is given to digital output pins while at high impedance level.
- 10. The 50MHz sampling rate is guaranteed. It is not recommended to use this device at sampling rates slower than 500kHz because the droop characteristics of the internal sample and hold exceed the limit required to maintain the specified accuracy of the device. Also, burst mode sampling is not recommended.
- 11. The ADC-321 has a clamp function. This clamp is enabled when CLAMP ENABLE (pin 29) is tied to GND and is disabled when tied to +DVs or left open. Clamp pulse inputs (pin 15) are effective when this clamp function is enabled and signals are clamped whole, this clamp pulse is low. The clamp reference input (pin 26) is set by an external trim. The CCP terminal (pin 27) integrates the clamp control voltage across an external capacitor. Refer to Figure 4 for examples of various ways to use this clamp function.
- 12. The TEST 1 and 2 (pins 9 and 11) are not used. Always leave them open.

### THEORY OF OPERATION

(See Functional Block Diagram, Figure 1, and Timing Diagrams, Figure 2)

- 1. The DATEL ADC-321 is a 2-step parallel A/D converter featuring a 4-bit upper comparator group and two 4-bit lower comparator groups, each with built-in sample and hold. A reference voltage equal to the voltage between (VRT VRB)/16 is constantly applied to the 4-bit upper comparator block. A voltage corresponding to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins provde the self generation function for VRT (reference voltage top) and VRB (reference voltage bottom) voltages.
- This converter uses an offset cancelation type comparator and operates synchronously with the external clock. It features various operating modes which are shown in the Timing Diagram (Figure 2) by the symbols S, H and C. These characters stand for Input Sampling (Auto Zero) Mode, Input Hold Mode and Comparison Mode.
- 3. The operation of the respective parts is as indicated in Figure 2-3. For instance, input voltage N is sampled with the falling edge of the first clock by means of the upper

comparator block and the lower comparator A block. Input voltage N+1 is sampled with the falling edge of the second clock by means of the upper comparator block and lower comparator B block. The upper comparator block finalizes comparison data UD(N) with the rising edge of the second clock. The lower comparator block finalizes comparison data LD(N) with the rising edge of the third clock. UD(N) and LD(N) are combined and routed to the output as Output Data N with the rising edge of the fourth clock. Thus there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Table 2: Digital Output Coding

Vin	М	T CODE LSB			
0V +7.812mV	0 0 0 0	0 0 0	0 (	0 0	0
+0.9922V +1.000V	0 1 1 0	1 1 0 0	-	1 1	1 0
+1.500V	1 1	0 0	0 (	0 0	0
+1.9922V	1 1	1 1	1	1 1	1

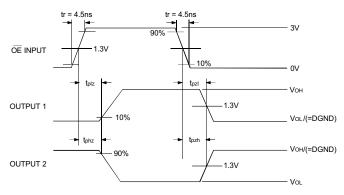


Figure 2-1. ADC-321 Timing Diagram

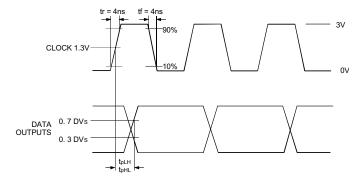


Figure 2-2. ADC-321 Timing Diagram



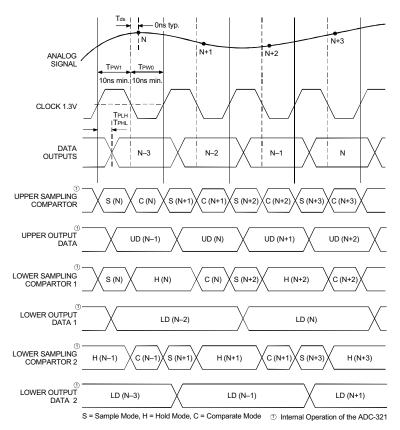


Figure 2-3. ADC-321 Timing Diagram

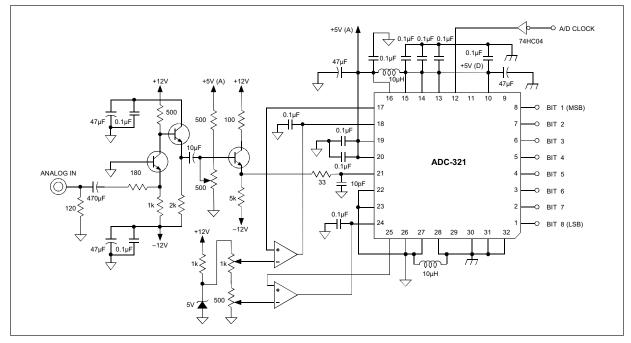


Figure 3. Typical Connection Diagram

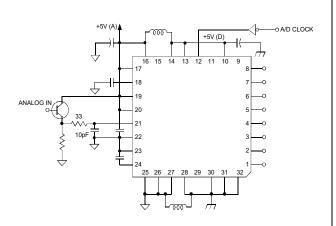


Figure 4-1. Clamp Not Used in Self Bias Mode

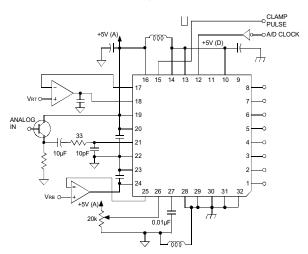


Figure 4-2. Clamp Used in External Reference Mode

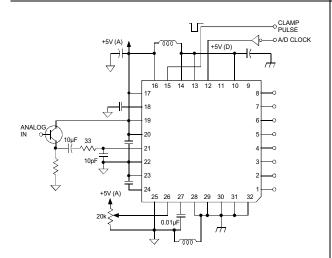


Figure 4-3. Clamp Used in Self Bias Mode

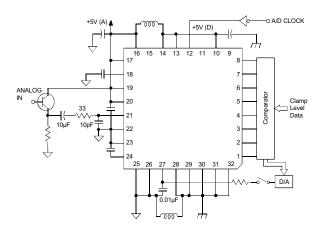


Figure 4-4. Digital Clamp Used in Self Bias Mode

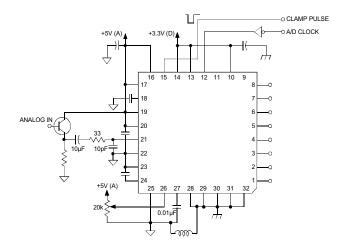


Figure 4-5. Clamp Used in Self Bias Mode With +5V/+3.3V Dual Power Supply



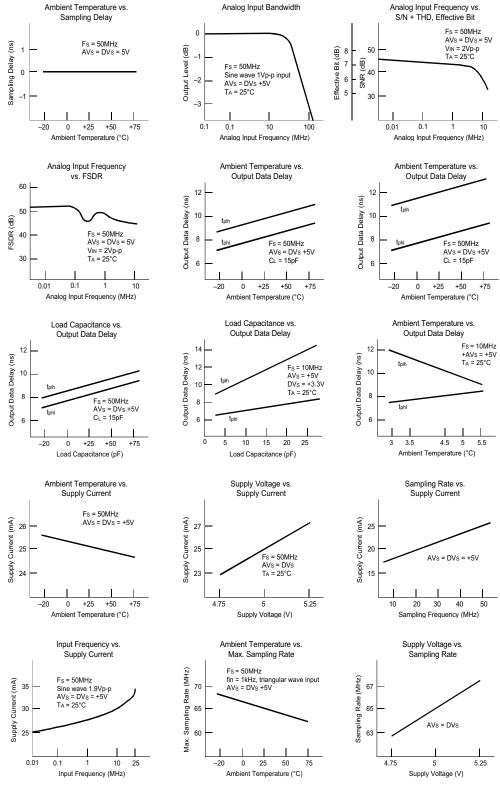


Figure 5: Typical Performance Curves

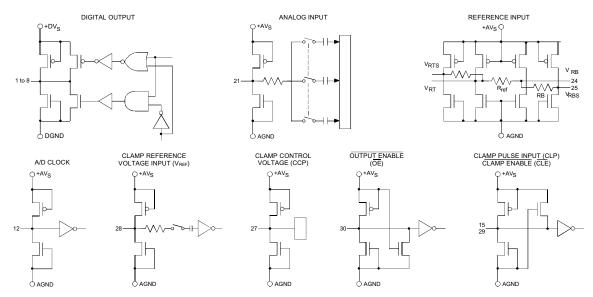
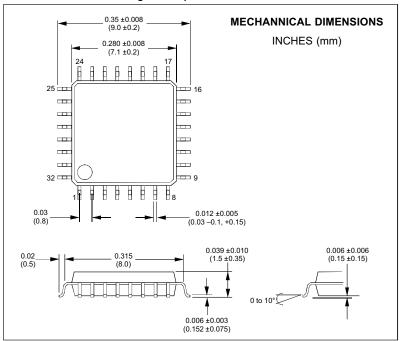


Figure 6: Equivalent Circuits



### ORDERING INFORMATION

ADC-321 8-bit, 50MHz A/D converter

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