# 72 Mb (2M x 36 & 4M x 18)
# DDR-II (Burst of 4) CIO Synchronous SRAMs

**MAY 2009**

## Features

- 2M x 36 or 4M x 18.
- On-chip delay-locked loop (DLL) for wide data valid window.
- Common I/O read and write ports.
- Synchronous pipeline read with late write operation.
- Double data rate (DDR-II) interface for read and write input ports.
- Fixed 4-bit burst for read and write operations.
- Clock stop support.
- Two input clocks (K and $\overline{K}$) for address and control registering at rising edges only.
- Two input clocks (C and $\overline{C}$) for data output control.
- Two echo clocks (CQ and $\overline{CQ}$) that are delivered simultaneously with data.
- +1.8V core power supply and 1.5, 1.8V $V_{DDQ}$, used with 0.75, 0.9V $V_{REF}$.
- HSTL input and output levels.
- Registered addresses, write and read controls, byte writes, and data outputs.
- Full data coherency.
- Boundary scan using limited set of JTAG 1149.1 functions.
- Byte write capability.
- Fine ball grid array (FBGA) package
  - 15mm x 17mm body size
  - 1mm pitch
  - 165-ball (11 x 15) array
- Programmable impedance output drivers via 5x user-supplied precision resistor.

## Description

The 72Mb IS61DDB42M36 and IS61DDB44M18 are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have a common I/O bus. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed. Refer to the *Timing Reference Diagram for Truth Table on p.8* for a description of the basic operations of these DDR-II (Burst of 4) CIO SRAMs.

Read and write addresses are registered on alternating rising edges of the K clock. Reads and writes are performed in double data rate. The following are registered internally on the rising edge of the K clock:

- Read and write addresses
- Address load
- Read/write enable
- Byte writes for burst addresses 1 and 3
- Data-in for burst addresses 1 and 3

The following are registered on the rising edge of the $\overline{K}$ clock:

- Byte writes for burst addresses 2 and 4
- Data-in for burst addresses 2 and 4

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered one cycle later than the write address. The first data-in burst is clocked one cycle later than the write command signal, and the second burst is timed to the following rising edge of the $\overline{K}$ clock. Two full clock cycles are required to complete a write operation.

During the burst read operation, at the first and third bursts the data-outs are updated from output registers off the second and fourth rising edges of the $\overline{C}$ clock (starting 1.5 cycles later). At the second and fourth bursts, the data-outs are updated with the third and fifth rising edges of the corresponding C clock (see page 9). The K and $\overline{K}$ clocks are used to time the data-outs whenever the C and $\overline{C}$ clocks are tied high. Two full clock cycles are required to complete a read operation

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

## x36 FBGA Pinout (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{CQ}$ | NC/SA* | SA | R/$\overline{W}$ | $\overline{BW}_2$ | $\overline{K}$ | $\overline{BW}_1$ | $\overline{LD}$ | SA | SA | CQ |
| B | NC | DQ27 | DQ18 | SA | $\overline{BW}_3$ | K | $\overline{BW}_0$ | SA | NC | NC | DQ8 |
| C | NC | NC | DQ28 | $V_{SS}$ | SA | $SA_0$ | $SA_1$ | $V_{SS}$ | NC | DQ17 | DQ7 |
| D | NC | DQ29 | DQ19 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | DQ16 |
| E | NC | NC | DQ20 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | DQ15 | DQ6 |
| F | NC | DQ30 | DQ21 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ5 |
| G | NC | DQ31 | DQ22 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ14 |
| H | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| J | NC | NC | DQ32 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ13 | DQ4 |
| K | NC | NC | DQ23 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ12 | DQ3 |
| L | NC | DQ33 | DQ24 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ2 |
| M | NC | NC | DQ34 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | DQ11 | DQ1 |
| N | NC | DQ35 | DQ25 | $V_{SS}$ | SA | SA | SA | $V_{SS}$ | NC | NC | DQ10 |
| P | NC | NC | DQ26 | SA | SA | C | SA | SA | NC | DQ9 | DQ0 |
| R | TDO | TCK | SA | SA | SA | $\overline{C}$ | SA | SA | SA | TMS | TDI |

* The following pins are reserved for higher densities: 2A for 144Mb

- $\overline{BW}_0$ controls writes to DQ0–DQ8; $\overline{BW}_1$ controls writes to DQ9–DQ17; $\overline{BW}_2$ controls writes to DQ18–DQ26; $\overline{BW}_3$ controls writes to DQ27–DQ35.

## x18 FBGA Pinout (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{CQ}$ | SA | SA | R/$\overline{W}$ | $\overline{BW}_1$ | $\overline{K}$ | NC/SA* | $\overline{LD}$ | SA | SA | CQ |
| B | NC | DQ9 | NC | SA | NC/SA* | K | $\overline{BW}_0$ | SA | NC | NC | DQ8 |
| C | NC | NC | NC | $V_{SS}$ | SA | $SA_0$ | $SA_1$ | $V_{SS}$ | NC | DQ7 | NC |
| D | NC | NC | DQ10 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| E | NC | NC | DQ11 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ6 |
| F | NC | DQ12 | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ5 |
| G | NC | NC | DQ13 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| H | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| J | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ4 | NC |
| K | NC | NC | DQ14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ3 |
| L | NC | DQ15 | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ2 |
| M | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | DQ1 | NC |
| N | NC | NC | DQ16 | $V_{SS}$ | SA | SA | SA | $V_{SS}$ | NC | NC | NC |
| P | NC | NC | DQ17 | SA | SA | C | SA | SA | NC | NC | DQ0 |
| R | TDO | TCK | SA | SA | SA | $\overline{C}$ | SA | SA | SA | TMS | TDI |

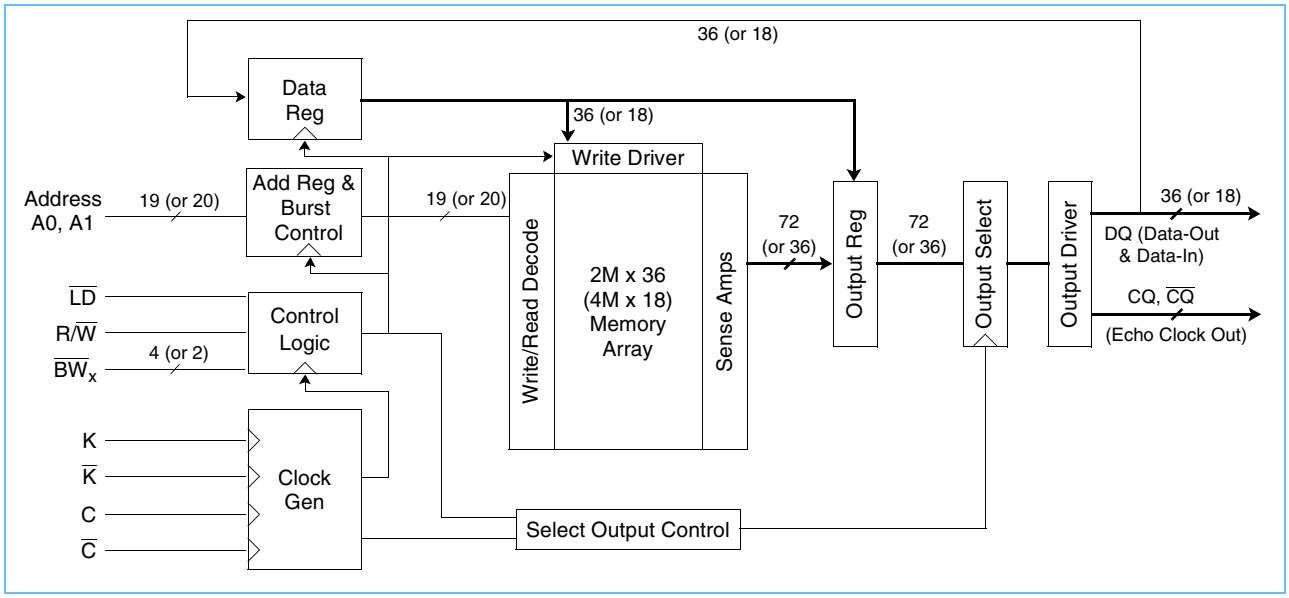
* The following pin is reserved for higher densities: 7A for 144Mb, 5B for 288Mb.

- $\overline{BW}_0$ controls writes to DQ0–DQ8; $\overline{BW}_1$ controls writes to DQ9–DQ17

## Pin Description

| Symbol | Pin Number | Description |
|---|---|---|
| K, $\overline{K}$ | 6B, 6A | Input clock. |
| C, $\overline{C}$ | 6P, 6R | Input clock for output data control. |
| CQ, $\overline{CQ}$ | 11A, 1A | Output echo clock. |
| $\overline{Doff}$ | 1H | DLL disable when low. |
| $SA_0$, $SA_1$ | 6C, 7C | Burst count address input. |
| SA | 3A, 9A, 10A, 4B, 8B, 5C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R,8R, 9R | 2M x 36 address inputs. |
| SA | 2A, 3A, 9A, 10A, 4B, 8B, 5C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R | 4M x 18 address inputs. |
| DQ0–DQ8<br>DQ9–DQ17<br>DQ18–DQ26<br>DQ27–DQ35 | 11P, 11M, 11L, 11K, 11J, 11F, 11E, 11C, 11B<br>10P, 11N, 10M, 10K, 10J, 11G, 10E, 11D, 10C<br>3B, 3D, 3E, 3F, 3G, 3K, 3L, 3N, 3P<br>2B, 3C, 2D, 2F, 2G, 3J, 2L, 3M, 2N | 2M x 36 DQ pins |
| DQ0–DQ8<br>DQ9–DQ17 | 11P, 10M, 11L, 11K, 10J, 11F, 11E, 10C, 11B<br>2B, 3D, 3E, 2F, 3G, 3K, 2L, 3N, 3P | 4M x 18 DQ pins |
| R/$\overline{W}$ | 4A | Read/write control. Read when active high. |
| $\overline{LD}$ | 8A | Synchronizes load. Loads new address when low. |
| $\overline{BW}_0$, $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$ | 7B, 7A, 5A,5B | 2M x 36 byte write control, active low. |
| $\overline{BW}_0$, $\overline{BW}_1$ | 7B, 5A | 4M x 18 byte write control, active low. |
| $V_{REF}$ | 2H, 10H | Input reference level. |
| $V_{DD}$ | 5F, 7F, 5G, 7G, 5H, 7H, 5J, 7J, 5K, 7K | Power supply. |
| $V_{DDQ}$ | 4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L | Output power supply. |
| $V_{SS}$ | 4C, 8C, 4D, 5D, 6D, 7D, 8D, 5E, 6E, 7E, 6F, 6G, 6H, 6J, 6K, 5L, 6L, 7L, 4M, 5M, 6M, 7M, 8M, 4N, 8N | Ground |
| ZQ | 11H | Output driver impedance control. |
| TMS, TDI, TCK | 10R, 11R, 2R | IEEE 1149.1 test inputs (1.8V LVTTL levels). |
| TDO | 1R | IEEE 1149.1 test output (1.8V LVTTL level). |
| NC | 2A, 1B, 9B, 10B, 1C, 2C, 9C, 1D, 9D, 10D, 1E, 2E, 9E, 1F, 9F, 10F, 1G, 9G, 10G, 1J, 2J, 9J, 1K, 2K, 9K, 1L, 9L, 10L, 1M, 2M, 9M, 1N, 9N, 10N, 1P, 2P, 9P | x36 Configuration |
| NC | 7A, 1B, 3B, 5B, 9B, 10B, 1C, 2C, 3C, 9C, 11C, 1D, 2D, 9D, 10D, 11D, 1E, 2E, 9E, 10E, 1F, 3F, 9F, 10F, 1G, 2G, 9G, 10G, 11G, 1J, 2J, 3J, 9J, 11J, 1K, 2K, 9K, 10K, 1L, 3L, 9L, 10L, 1M, 2M, 3M, 9M, 11M, 1N, 2N, 9N, 10N, 11N, 1P, 2P, 9P, 10P | x18 Configuration |

## Block Diagram




## SRAM Features

### Read Operations

The SRAM operates continuously in a burst-of-four mode. Read cycles are started by registering R/$\overline{W}$ in active high state at the rising edge of the K clock. R/$\overline{W}$ can be activated every other cycle because two full cycles are required to complete the burst-of-four read in DDR mode. A second set of clocks, C and $\overline{C}$, are used to control the timing to the outputs. A set of free-running echo clocks, CQ and $\overline{CQ}$, are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

When the C and $\overline{C}$ clocks are connected high, the K and $\overline{K}$ clocks assume the function of those clocks. In this case, the data corresponding to the first address is clocked 1.5 cycles later by the rising edge of the $\overline{K}$ clock. The data corresponding to the second burst is clocked 2 cycles later by the following rising edge of the K clock. The third data-out is clocked by the subsequent rising edge of the $\overline{K}$ clock, and the fourth data-out is clocked by the subsequent rising edge of the K clock.

Whenever $\overline{LD}$ is low, a new address is registered at the rising edge of the K clock. A NOP operation ($\overline{LD}$ is high) does not terminate the previous read. The output drivers disable automatically to a high state.

### Write Operations

Write operations can also be initiated at every other rising edge of the K clock whenever R/$\overline{W}$ is low. The write address is also registered at that time. When the address needs to change, $\overline{LD}$ needs to be low simultaneously to be registered by the rising edge of K. Again, the write always occurs in bursts of four.

The write data is provided in a 'late write' mode; that is, the data-in corresponding to the first address of the burst, is presented 1 cycle later or at the rising edge of the following K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of $\overline{K}$. The third data-out is clocked by the subsequent rising edge of the K clock, and the fourth data-out is clocked by the subsequent rising edge of the $\overline{K}$ clock.

The data-in provided for writing is initially kept in write buffers. The information on these buffers is written into the array on the third write cycle. A read cycle to the last two write address produces data from the write buffers. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the four burst addresses is written (see *X18/X36 Write Truth Tables* on page 9, 10 and *Timing Reference Diagram for Truth Table* on page 8).

Whenever a write is disabled (R/$\overline{W}$ is high at the rising edge of K), data is not written into the memory.

### RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and $V_{SS}$ to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For example, an RQ of 250Ω results in a driver impedance of 50Ω. The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω, with the tolerance described in *Programmable Impedance Output Driver DC Electrical Characteristics* on page 14. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than 3 pF.

The ZQ pin can also be directly connected to $V_{DDQ}$ to obtain a minimum impedance setting. ZQ must never be connected to $V_{SS}$.

### Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. At power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 1024 clock cycles.

### Single Clock Mode

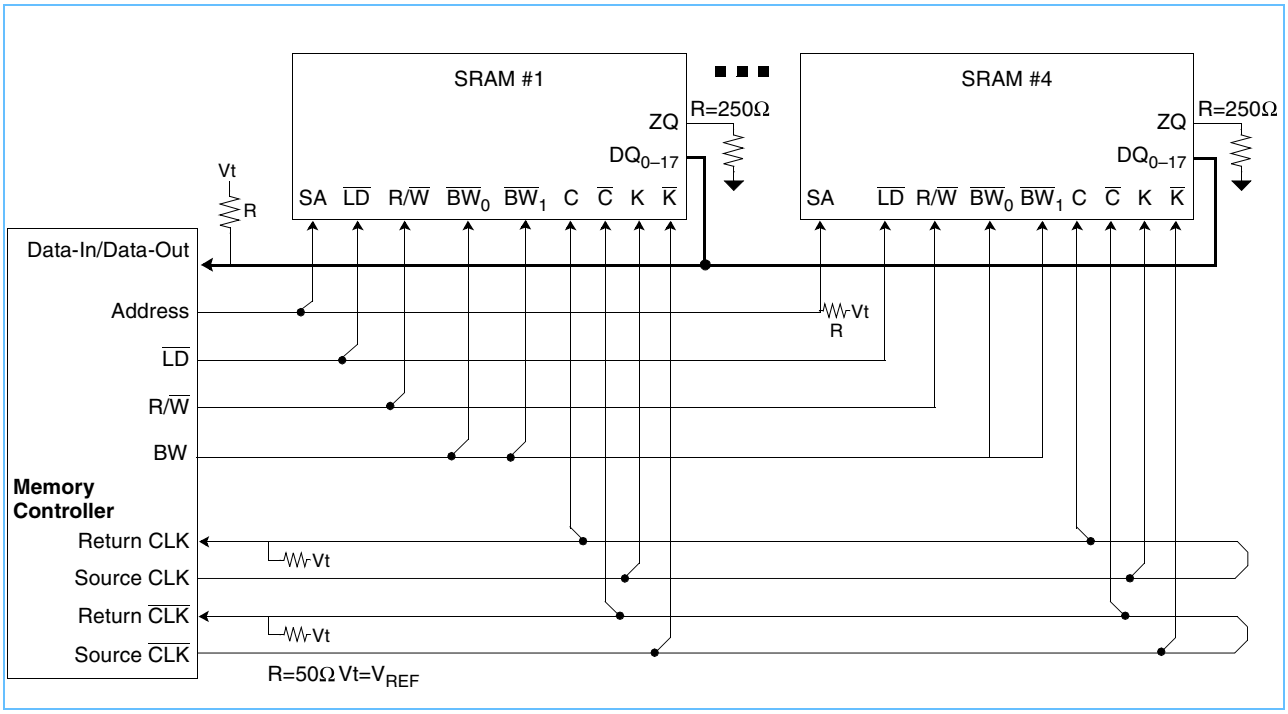
This device can be also operated in single-clock mode. In this case, C and $\overline{C}$ are both connected high at power-up and must never change. Under this condition, K and $\overline{K}$ control the output timings.

Either clock pair must have both polarities switching and must never connect to $V_{REF}$, as they are not differential clocks.

### Depth Expansion

The following figure depicts an implementation of four 4M x 18 DDR-II SRAMs with common I/Os. In this application example, the second pair of C and C clocks is delayed such that the return data meets the data setup and hold times at the memory controller.

## Application Example




## Power-Up and Power-Down Sequences

The following sequence is used for power-up:

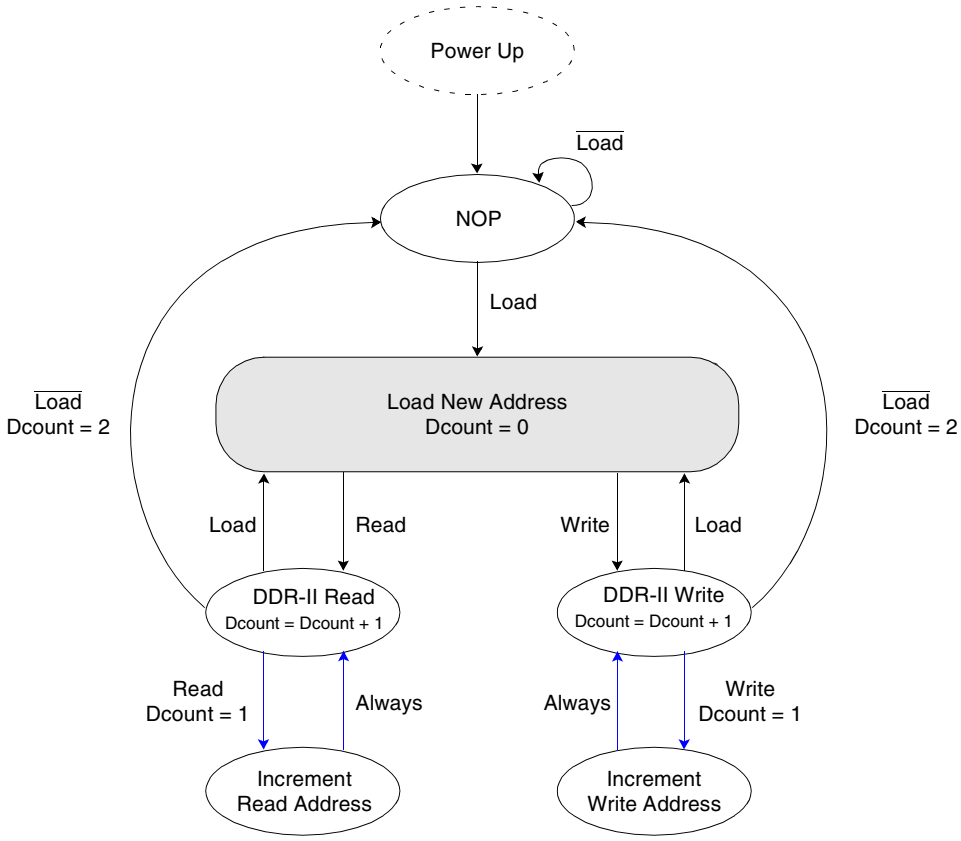
1. The power supply inputs must be applied in the following order while keeping $\overline{\text{Doff}}$ in LOW logic state:

    1) VDD
    2) VDDQ
    3) VREF

2. Start applying stable clock inputs (K, $\overline{\text{K}}$, C, and $\overline{\text{C}}$).
3. After clock signals have stabilized, change $\overline{\text{Doff}}$ to HIGH logic state.
4. Once the $\overline{\text{Doff}}$ is switched to HIGH logic state, wait an additional 1024 clock cycles to lock the DLL.

NOTES:
1. The power-down sequence must be done in reverse of the power-up sequence.
2. VDDQ can be allowed to exceed VDD by no more than 0.6V.
3. VREF can be applied concurrently with VDDQ.

## State Diagram



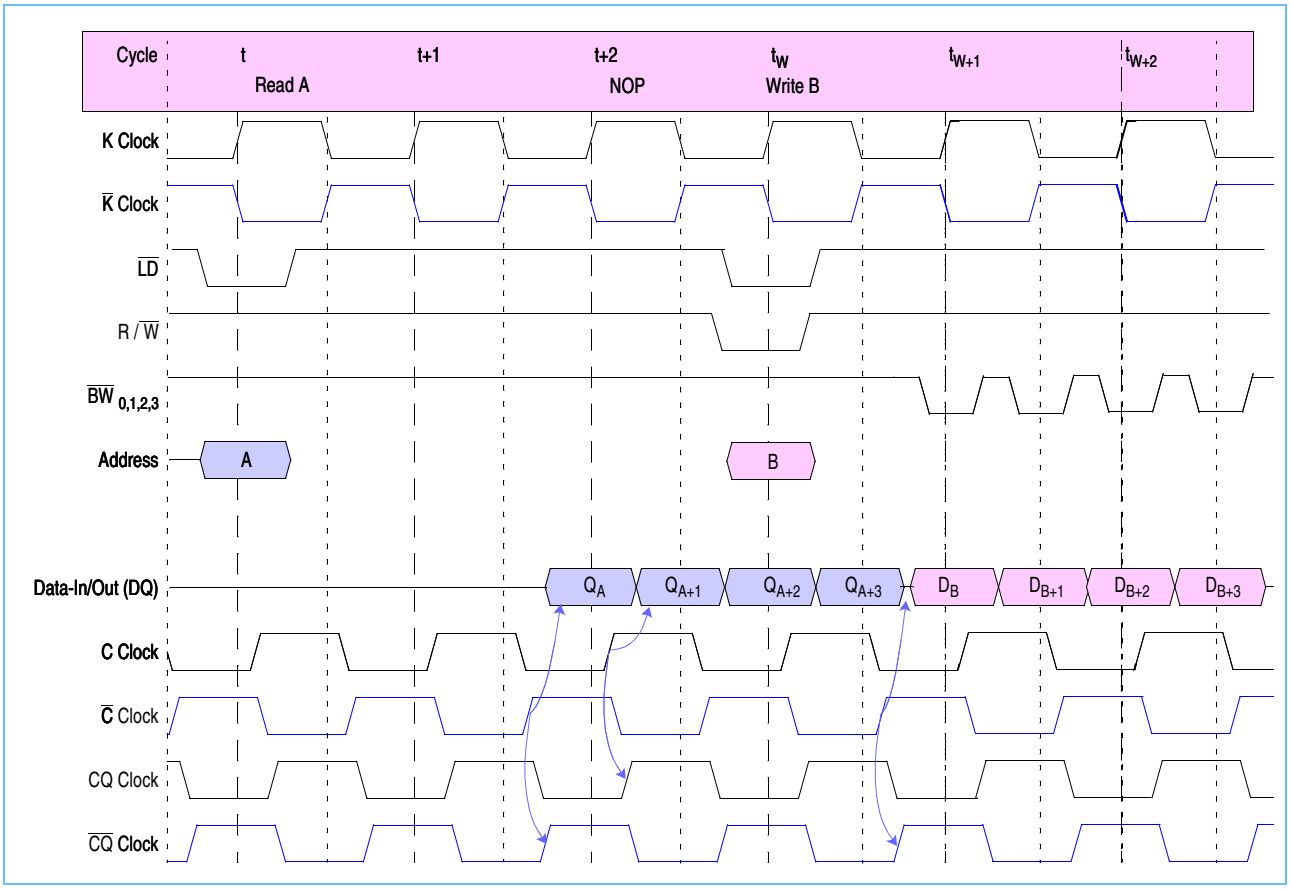

**Notes:** 1. Internal burst counter is fixed as four-bit linear; that is, when first address is A0+0, next internal burst address is A0+1.
2. *Read* refers to read active status with R/$\overline{W}$ = high.
3. *Write* refers to write active status with R/$\overline{W}$ = low.
4. *Load* refers to read new address active status with $\overline{LD}$ = low.
5. *Load* is read new address inactive status with $\overline{LD}$ = high.

The *Timing Reference Diagram for Truth Table* on page 8 is helpful in understanding the clock and write truth tables, as it shows the cycle relationship between clocks, address, data-in, data-out, and controls. All read and write commands are issued at the beginning of cycles t and $t_w$, respectively.

## Linear Burst Sequence Table

| Burst Sequence | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|
| | $SA_1$ | $SA_0$ | $SA_1$ | $SA_0$ | $SA_1$ | $SA_0$ | $SA_1$ | $SA_0$ |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

## Timing Reference Diagram for Truth Table




## Clock Truth Table (Use the following table with the *Timing Reference Diagram for Truth Table*.)

| Mode | Clock | Controls | | Data Out / Data In | | | |
|---|---|---|---|---|---|---|---|
| | K | LD̄ | R/W̄ | $Q_A$ / $D_B$ | $Q_{A+1}$ / $D_{B+1}$ | $Q_{A+2}$ / $D_{B+2}$ | $Q_{A+3}$ / $D_{B+3}$ |
| Stop Clock | Stop | X | X | Previous State | Previous State | Previous State | Previous State |
| No Operation (NOP) | L→H | H | H | High-Z | High-Z | High-Z | High-Z |
| Read B | L→H | L | H | Dout at C̄ (t + 1.5) | Dout at C (t + 2) | Dout at C̄ (t + 2.5) | Dout at C (t + 3) |
| Write A | L→H | L | L | $D_B$ ($t_W$ + 1) | $D_B$ ($t_W$ + 1.5) | $D_B$ ($t_W$ + 2) | $D_B$ ($t_W$ + 2.5) |

**Notes**:

1. The internal burst counter is always fixed as two-bit.
2. X = don't care; H = logic "1"; L = logic "0".
3. A read operation is started when control signal R/W̄ is active high.
4. A write operation is started when control signal R/W̄ is active low.
5. Before entering into the stop clock, all pending read and write commands must be completed.
6. For timing definitions, refer to the *AC Characteristics* on page 16. Signals must have AC specifications at timings indicated in parenthesis with respect to switching clocks K, K̄, C, and C̄.

**X36 Write Truth Table** Use the following table with the *Timing Reference Diagram for Truth Table* on page 8.

| Operation | K ($t_W$+1) | $\overline{K}$ ($t_W$+1.5) | K ($t_W$+2) | $\overline{K}$ ($t_W$+2.5) | $\overline{BW}_0$ | $\overline{BW}_1$ | $\overline{BW}_2$ | $\overline{BW}_3$ | $D_B$ | $D_{B+1}$ | $D_{B+2}$ | $D_{B+3}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write Byte 0 | L→H | | | | L | H | H | H | D0-8 ($t_W$+1) | | | |
| Write Byte 1 | L→H | | | | H | L | H | H | D9-17 ($t_W$+1) | | | |
| Write Byte 2 | L→H | | | | H | H | L | H | D18-26 ($t_W$+1) | | | |
| Write Byte 3 | L→H | | | | H | H | H | L | D27-35 ($t_W$+1) | | | |
| Write All Bytes | L→H | | | | L | L | L | L | D0-35 ($t_W$+1) | | | |
| Abort Write | L→H | | | | H | H | H | H | Don't care | | | |
| Write Byte 0 | | L →H | | | L | H | H | H | | D0-8 ($t_W$+1.5) | | |
| Write Byte 1 | | L→H | | | H | L | H | H | | D9-17 ($t_W$+1.5) | | |
| Write Byte 2 | | L→H | | | H | H | L | H | | D18-26 ($t_W$+1.5) | | |
| Write Byte 3 | | L→H | | | H | H | H | L | | D27-35 ($t_W$+1.5) | | |
| Write All Bytes | | L→H | | | L | L | L | L | | D0-35 ($t_W$+1.5) | | |
| Abort Write | | L→H | | | H | H | H | H | | Don't care | | |
| Write Byte 0 | | | L→H | | L | H | H | H | | | D0-8 ($t_W$+2) | |
| Write Byte 1 | | | L→H | | H | L | H | H | | | D9-17 ($t_W$+2) | |
| Write Byte 2 | | | L→H | | H | H | L | H | | | D18-26 ($t_W$+2) | |
| Write Byte 3 | | | L→H | | H | H | H | L | | | D27-35 ($t_W$+2) | |
| Write All Bytes | | | L→H | | L | L | L | L | | | D0-35 ($t_W$+2) | |
| Abort Write | | | L→H | | H | H | H | H | | | Don't care | |
| Write Byte 0 | | | | L→H | L | H | H | H | | | | D0-8 ($t_W$+2.5) |
| Write Byte 1 | | | | L→H | H | L | H | H | | | | D9-17 ($t_W$+2.5) |
| Write Byte 2 | | | | L→H | H | H | L | H | | | | D18-26 ($t_W$+2.5) |
| Write Byte 3 | | | | L→H | H | H | H | L | | | | D27-35 ($t_W$+2.5) |
| Write All Bytes | | | | L→H | L | L | L | L | | | | D0-35 ($t_W$+2.5) |
| Abort Write | | | | L→H | H | H | H | H | | | | Don't care |

**Notes**;

1. For all cases, R/$\overline{W}$ needs to be active low during the rising edge of K occurring at time $t_W$
2. For timing definitions refer to the *AC Characteristics* on page 16. Signals must have AC specifications with respect to switching clocks $\overline{K}$ and K.

**X18 Write Truth Table** Use the following table with the *Timing Reference Diagram for Truth Table* on page 8.

| Operation | K ($t_W$+1) | $\overline{K}$ ($t_W$+1.5) | K ($t_W$+2) | $\overline{K}$ ($t_W$+2.5) | $\overline{BW_0}$ | $\overline{BW_1}$ | $D_B$ | $D_{B+1}$ | $D_{B+2}$ | $D_{B+3}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Write Byte 0 | L→H | | | | L | H | D0-8 ($t_W$+1) | | | |
| Write Byte 1 | L→H | | | | H | L | D9-17 ($t_W$+1) | | | |
| Abort Write | L→H | | | | H | H | Don't care | | | |
| Write Byte 0 | | L→H | | | L | H | | D0-8 ($t_W$+1.5) | | |
| Write Byte 1 | | L→H | | | H | L | | D9-17 ($t_W$+1.5) | | |
| Write All Bytes | | L→H | | | L | L | | D0-17 ($t_W$+1.5) | | |
| Abort Write | | L→H | | | H | H | | Don't care | | |
| Write Byte 0 | | | L→H | | L | H | | | D0-8 ($t_W$+2) | |
| Write Byte 1 | | | L→H | | H | L | | | D9-17 ($t_W$+2) | |
| Write All Bytes | | | L→H | | L | L | | | D0-17 ($t_W$+2) | |
| Abort Write | | | L→H | | H | H | | | Don't care | |
| Write Byte 0 | | | | L→H | L | H | | | | D0-8 ($t_W$+2.5) |
| Write Byte 1 | | | | L→H | H | L | | | | D9-17 ($t_W$+2.5) |
| Write All Bytes | | | | L→H | L | L | | | | D0-17 ($t_W$+2.5) |
| Abort Write | | | | L→H | H | H | | | | Don't care |

**Notes**;
1. For all cases, R/$\overline{W}$ needs to be active low during the rising edge of K occurring at time $t_W$
2. For timing definitions refer to the *AC Characteristics* on page 16. Signals must have AC specifications with respect to switching clocks $\overline{K}$ and K.

## Absolute Maximum Ratings

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | -0.5 to 2.9 | V |
| Output power supply voltage | $V_{DDQ}$ | -0.5 to 2.9 | V |
| Input voltage | $V_{IN}$ | -0.5 to VDD+0.3 | V |
| Data out voltage | $V_{DOUT}$ | -0.5 to 2.6 | V |
| Operating temperature | $T_A$ | 0 to 70 | °C |
| Junction temperature | $T_J$ | 110 | °C |
| Storage temperature | $T_{STG}$ | -55 to +125 | °C |

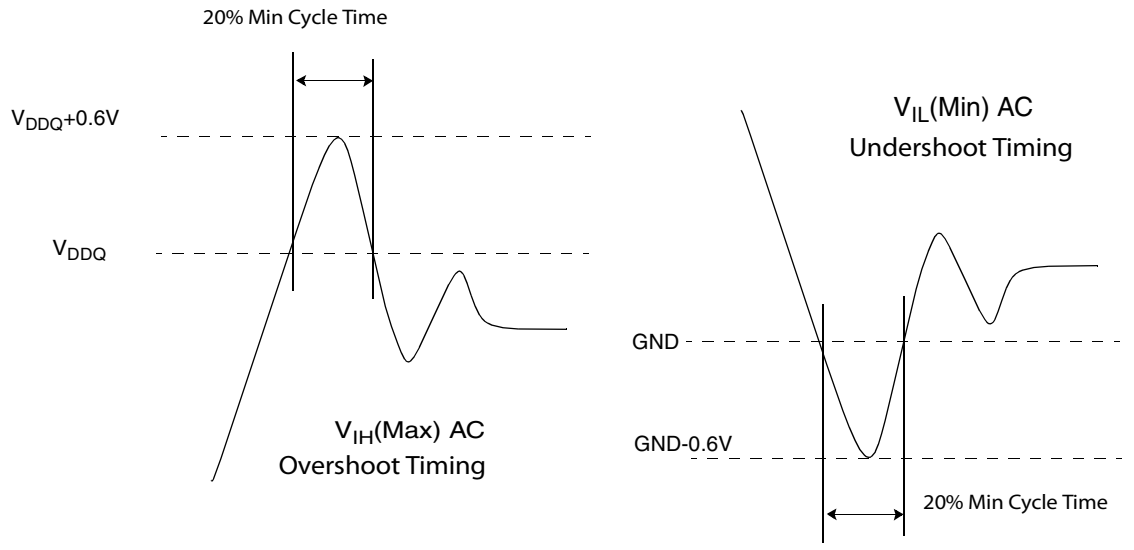
**Note:** Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions ($T_A$ = 0 to +70° C)

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 1.8 - 5% | | 1.8 + 5% | V | 1 |
| Output driver supply voltage | $V_{DDQ}$ | 1.4 | | 1.9 | V | 1 |
| Input high voltage | $V_{IH}$ | $V_{REF}$ +0.1 | | $V_{DDQ}$ + 0.3 | V | 1, 2 |
| Input low voltage | $V_{IL}$ | -0.3 | | $V_{REF}$ - 0.1 | V | 1, 3 |
| Input reference voltage | $V_{REF}$ | 0.68 | | 0.95 | V | 1, 5 |
| Clocks signal voltage | $V_{IN - CLK}$ | -0.3 | | $V_{DDQ}$ + 0.3 | V | 1, 4 |

1. All voltages are referenced to $V_{SS}$. All $V_{DD}$, $V_{DDQ}$, and $V_{SS}$ pins must be connected.
2. $V_{IH}$(Max) AC = See *0vershoot and Undershoot Timings*.
3. $V_{IL}$(Min) AC = See *0vershoot and Undershoot Timings*.
4. $V_{IN-CLK}$ specifies the maximum allowable DC excursions of each clock (K, $\overline{K}$, C, and $\overline{C}$).
5. Peak-to-peak AC component superimposed on $V_{REF}$ may not exceed 5% of $V_{REF}$.

## 0vershoot and Undershoot Timings




## PBGA Thermal Characteristics

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Thermal resistance junction to ambient (airflow = 1m/s) | RΘJA | 18.6 | °C/W |
| Thermal resistance junction to case | RΘJC | 4.3 | °C/W |
| Thermal resistance junction to pins | RΘJB | 1.77 | °C/W |

## Capacitance ($T_A$ = 0 to +70° C, $V_{DD}$ = 1.8V -5%, +5%, f = 1MHz)

| Parameter | Symbol | Test Condition | Maximum | Units |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0V | 4 | pF |
| Data-in/Out capacitance (DQ0–DQ35) | $C_{DQ}$ | $V_{DIN}$ = 0V | 4 | pF |
| Clocks Capacitance (K, $\overline{K}$, C, $\overline{C}$) | $C_{CLK}$ | $V_{CLK}$ = 0V | 4 | pF |

## DC Electrical Characteristics ($T_A$ = 0 to + 70 C, $V_{DD}$ = 1.8V -5%, +5%)

| Parameter | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| x36 average power supply operating current ($I_{OUT}$ = 0, $V_{IN}$ = $V_{IH}$ or $V_{IL}$) | $I_{DD33}$<br>$I_{DD40}$<br>$I_{DD50}$ | —<br>—<br>— | 600<br>550<br>500 | mA | 1, 3 |
| x18 average power supply operating current ($I_{OUT}$ = 0, $V_{IN}$ = $V_{IH}$ or $V_{IL}$) | $I_{DD33}$<br>$I_{DD40}$<br>$I_{DD50}$ | —<br>—<br>— | 600<br>550<br>500 | mA | 1, 3 |
| Power supply standby current ($\overline{R}$ = $V_{IH}$, $\overline{W}$ = $V_{IH}$. All other inputs = $V_{IH}$ or $V_{IH}$, $I_{IH}$ = 0) | $I_{SBSS}$ | — | 200 | mA | 1 |
| Input leakage current, any input (except JTAG) ($V_{IN}$ = $V_{SS}$ or $V_{DD}$) | $I_{LI}$ | -2 | +2 | uA | |
| Output leakage current ($V_{OUT}$ = $V_{SS}$ or $V_{DDQ}$, Q in High-Z) | $I_{LO}$ | -2 | +2 | uA | |
| Output “high” level voltage ($I_{OH}$ = -6mA) | $V_{OH}$ | $V_{DDQ}$ -.4 | $V_{DDQ}$ | V | 2, 4 |
| Output “low” level voltage ($I_{OL}$ = +6mA) | $V_{OL}$ | $V_{SS}$ | $V_{SS}$+.4 | V | 2, 4 |
| JTAG leakage current ($V_{IN}$ = $V_{SS}$ or $V_{DD}$) | $I_{LIJTAG}$ | -100 | +100 | uA | 5 |

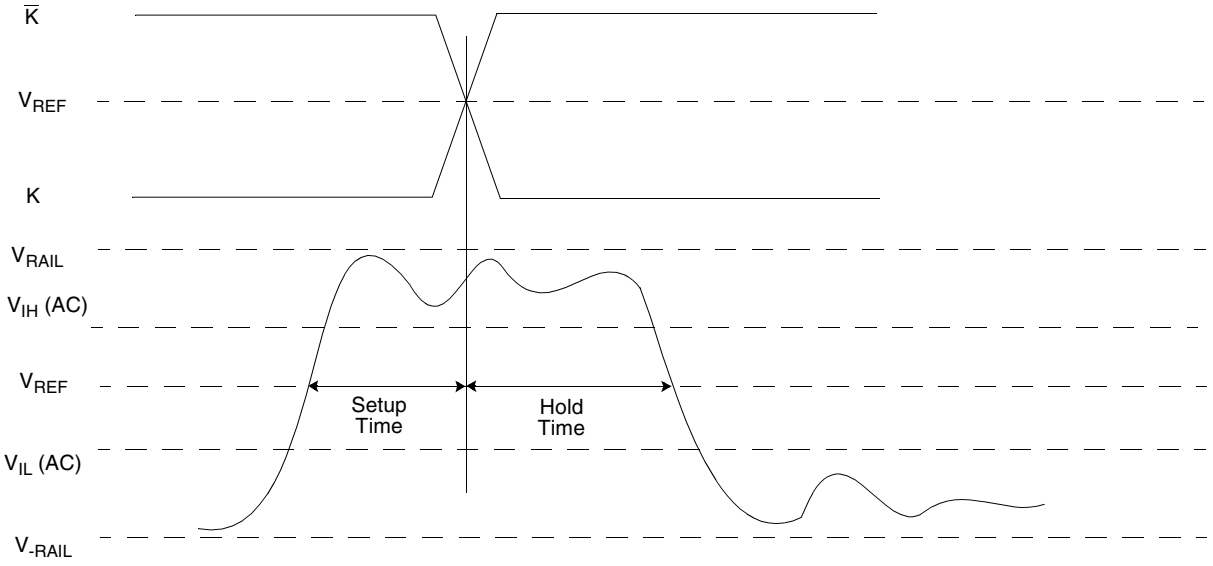
1. $I_{OUT}$ = chip output current.
2. Minimum impedance output driver.
3. The numeric suffix indicates the part operating at speed, as indicated in *AC Characteristics* on page 16.
4. JEDEC Standard JESD8-6 Class 1 compatible.
5. For JTAG inputs only.
6. Currents are estimates only and need to be verified.

## Typical AC Input Characteristics

| Item | Symbol | Minimum | Maximum | Notes |
|---|---|---|---|---|
| AC input logic high | $V_{IH}$ (ac) | $V_{REF}$ + 0.2 | | 1, 2, 3, 4 |
| AC input logic low | $V_{IL}$ (ac) | | $V_{REF}$ - 0.2 | 1, 2, 3, 4 |
| Clock input logic high (K, $\overline{K}$, C, $\overline{C}$) | $V_{IH-CLK}$ (ac) | $V_{REF}$ + 0.2 | | 1, 2, 3 |
| Clock input logic low (K, $\overline{K}$, C, $\overline{C}$) | $V_{IL-CLK}$ (ac) | | $V_{REF}$ - 0.2 | 1, 2, 3 |

1. The peak-to-peak AC component superimposed on $V_{REF}$ may not exceed 5% of the DC component of $V_{REF}$.
2. Performance is a function of $V_{IH}$ and $V_{IL}$ levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past VIH (AC) and VIL (AC) during the input setup and input hold window. VIH (AC) and VIL (AC) are used for timing purposes only.

## AC Input Definition




## Programmable Impedance Output Driver DC Electrical Characteristics

($T_A$ = 0 to +70° C, $V_{DD}$ = 1.8V -5%, +5%, $V_{DDQ}$ = 1.5, 1.8V)

| Parameter | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Output “high” level voltage | $V_{OH}$ | $V_{DDQ}$ / 2 | $V_{DDQ}$ | V | 1, 3 |
| Output “low” level voltage | $V_{OL}$ | $V_{SS}$ | $V_{DDQ}$ / 2 | V | 2, 3 |

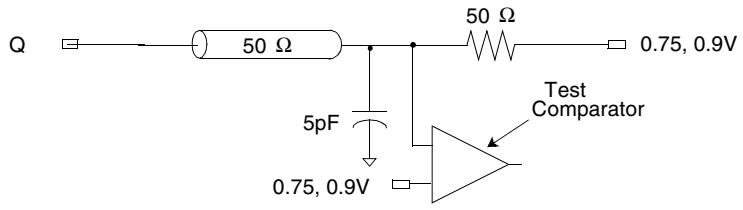
1. $I_{OH} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
2. $I_{OL} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right) \pm 15\%$ @ $V_{OL} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
3. Parameter tested with RQ = 250Ω and $V_{DDQ}$ = 1.5V.

## AC Test Conditions ($T_A$ = 0 to +70° C, $V_{DD}$ = 1.8V -5%, +5%, $V_{DDQ}$ = 1.5, 1.8V)

| Parameter | Symbol | Conditions | Units | Notes |
|---|---|---|---|---|
| Output driver supply voltage | $V_{DDQ}$ | 1.5, 1.8 | V | |
| Input high level | $V_{IH}$ | $V_{REF}$+0.5 | V | |
| Input Low Level | $V_{IL}$ | $V_{REF}$-0.5 | V | |
| Input reference voltage | $V_{REF}$ | 0.75, 0.9 | V | |
| Input rise time | $T_R$ | 0.35 | ns | |
| Input fall time | $T_F$ | 0.35 | ns | |
| Output timing reference level | | $V_{REF}$ | V | |
| Clocks reference level | | $V_{REF}$ | V | |
| Output load conditions | | | | 1, 2 |

1. See *AC Test Loading*.
2. Parameter tested with RQ = 250Ω and $V_{DDQ}$ = 1.5V.

## AC Test Loading



## AC Characteristics ($T_A$ = 0 to + 70 C, $V_{DD}$ = 1.8V -5%, +5%)

| Parameter | Symbol | 33 (300MHz) | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| **Clock** | | | | | |
| Cycle time (K, $\overline{K}$, C, $\overline{C}$) | $t_{KHKH}$ | 3.3 | 7.5 | ns | |
| Clock phase jitter (K, $\overline{K}$, C, $\overline{C}$) | $t_{KC\text{-}VAR}$ | | 0.2 | ns | |
| Clock high pulse (K, $\overline{K}$, C, $\overline{C}$) | $t_{KHKL}$ | 1.32 | | ns | |
| Clock low pulse (K, $\overline{K}$, C, $\overline{C}$) | $t_{KLKH}$ | 1.32 | | ns | |
| Clock to $\overline{clock}$ ($K_H$>$\overline{K}_H$, $C_H$>$\overline{C}_H$) | $t_{KH\overline{K}H}$ | 1.49 | | ns | |
| Clock to data clock ($K_H$>$C_H$, $\overline{K}_H$>$\overline{C}_H$) | $t_{KHCH}$ | 0.0 | 0.8 | ns | |
| DLL lock (K, C) | $t_{KC\text{-}lock}$ | 1024 | | cycle | |
| Doff Low period to DLL reset | tDoffLowToReset | 5 | | ns | |
| **Output Times** | | | | | |
| C, $\overline{C}$ high to output valid | $t_{CHQV}$ | | 0.35 | ns | 1, 3 |
| C, $\overline{C}$ high to output hold | $t_{CHQX}$ | -0.35 | | ns | 1, 3 |
| C, $\overline{C}$ high to echo clock valid | $t_{CHCQV}$ | | 0.33 | ns | 3 |
| C, $\overline{C}$ high to echo clock hold | $t_{CHCQX}$ | -0.33 | | ns | 3 |
| CQ, $\overline{CQ}$ high to output valid | $t_{CQHQV}$ | | 0.35 | ns | 1, 3 |
| CQ, $\overline{CQ}$ high to output hold | $t_{CQHQX}$ | -0.33 | | ns | 1, 3 |
| C high to output high-Z | $t_{CHQZ}$ | | 0.35 | ns | 1, 3 |
| C high to output low-Z | $t_{CHQX1}$ | -0.33 | | ns | 1, 3 |
| **Setup Times** | | | | | |
| Address valid to K, $\overline{K}$ rising edge | $t_{AVKH}$ | 0.4 | — | ns | 2 |
| Control inputs valid to K rising edge | $t_{IVKH}$ | 0.4 | — | ns | 2 |
| Data-in valid to K, $\overline{K}$ rising edge | $t_{DVKH}$ | 0.30 | — | ns | 2 |
| **Hold Times** | | | | | |
| K rising edge to address hold | $t_{KHAX}$ | 0.4 | — | ns | 2 |
| K rising edge to control inputs hold | $t_{KHIX}$ | 0.4 | — | ns | 2 |
| K, $\overline{K}$ rising edge to data-in hold | $t_{KHDX}$ | 0.30 | — | ns | 2 |

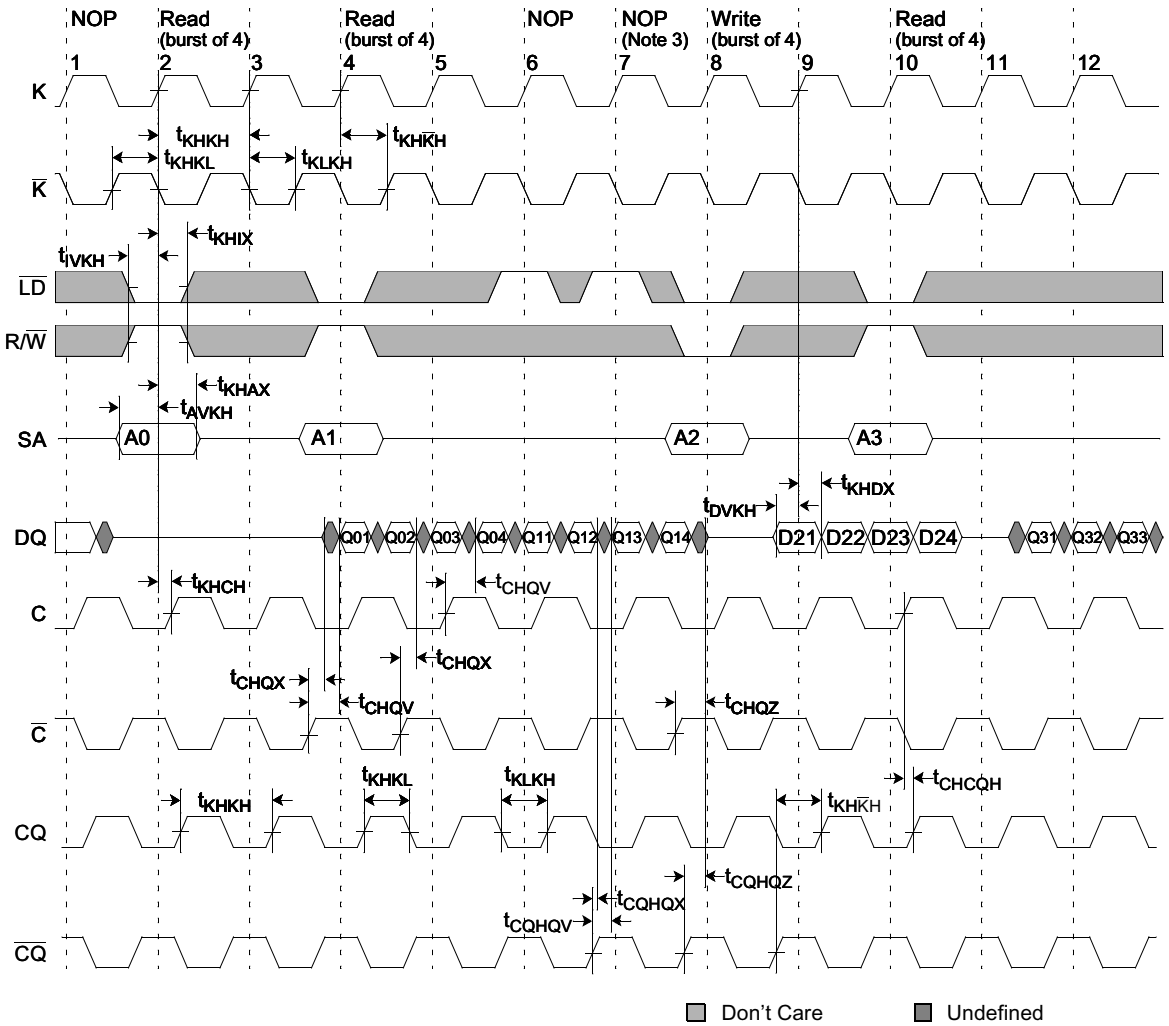
1. See *AC Test Loading* on page 15.
2. During normal operation, $V_{IH}$, $V_{IL}$, $T_{RISE}$, and $T_{FALL}$ of inputs must be within 20% of $V_{IH}$, $V_{IL}$, $T_{RISE}$, and $T_{FALL}$ of clock.
3. If C, $\overline{C}$ are tied high, then K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters.

## AC Characteristics ($T_A$ = 0 to +70 C, $V_{DD}$ = 1.8V -5%, +5%)

| Parameter | Symbol | 40 (250MHz) | | 50 (200MHz) | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| **Clock** | | | | | | | |
| Cycle time (K, $\overline{K}$, C, $\overline{C}$) | $t_{KHKH}$ | 4.0 | 7.5 | 5.0 | 7.5 | ns | |
| Clock phase jitter (K, $\overline{K}$, C, $\overline{C}$) | $t_{KC\text{-}VAR}$ | | 0.2 | | 0.2 | ns | |
| Clock high pulse (K, $\overline{K}$, C, $\overline{C}$) | $t_{KHKL}$ | 1.6 | | 2.0 | | ns | |
| Clock low pulse (K, $\overline{K}$, C, $\overline{C}$) | $t_{KLKH}$ | 1.6 | | 2.0 | | ns | |
| Clock to $\overline{clock}$ ($K_H$>$\overline{K}_H$, $C_H$>$\overline{C}_H$) | $t_{KH\overline{K}H}$ | 1.8 | | 2.2 | | ns | |
| Clock to data clock ($K_H$>$C_H$, $\overline{K}_H$>$\overline{C}_H$) | $t_{KHCH}$ | 0.0 | 0.8 | 0.0 | 0.8 | ns | |
| DLL lock (K, C) | $t_{KC\text{-}lock}$ | 1024 | | 1024 | | cycle | |
| Doff Low period to DLL reset | tDoffLowToReset | 5 | | 5 | | ns | |
| **Output Times** | | | | | | | |
| C, $\overline{C}$ high to output valid | $t_{CHQV}$ | | 0.35 | | 0.38 | ns | 1, 3 |
| C, $\overline{C}$ high to output hold | $t_{CHQX}$ | -0.35 | | -0.38 | | ns | 1, 3 |
| C, $\overline{C}$ high to echo clock valid | $t_{CHCQV}$ | | 0.33 | | 0.36 | ns | 3 |
| C, $\overline{C}$ high to echo clock hold | $t_{CHCQX}$ | -0.33 | | -0.36 | | ns | 3 |
| CQ, $\overline{CQ}$ High to output valid | $t_{CQHQV}$ | | 0.35 | | 0.36 | ns | 1, 3 |
| CQ, $\overline{CQ}$ high to output hold | $t_{CQHQX}$ | -0.35 | | -0.36 | | ns | 1, 3 |
| C High to output high-Z | $t_{CHQZ}$ | | 0.35 | | 0.38 | ns | 1, 3 |
| C High to output low-Z | $t_{CHQX1}$ | -0.35 | | -0.38 | | ns | 1, 3 |
| **Setup Times** | | | | | | | |
| Address valid to K, $\overline{K}$ rising edge | $t_{AVKH}$ | 0.4 | — | 0.5 | — | ns | 2 |
| Control inputs valid to K rising edge | $t_{IVKH}$ | 0.4 | — | 0.5 | — | ns | 2 |
| Data-in valid to K, $\overline{K}$ rising edge | $t_{DVKH}$ | 0.35 | — | 0.4 | — | ns | 2 |
| **Hold Times** | | | | | | | |
| K rising edge to address hold | $t_{KHAX}$ | 0.4 | — | 0.5 | — | ns | 2 |
| K rising edge to Control Inputs Hold | $t_{KHIX}$ | 0.4 | — | 0.5 | — | ns | 2 |
| K, $\overline{K}$ rising edge to data-in hold | $t_{KHDX}$ | 0.35 | — | 0.4 | — | ns | 2 |

1. See *AC Test Loading* on page 14.
2. During normal operation, $V_{IH}$, $V_{IL}$, $T_{RISE}$, and $T_{FALL}$ of inputs must be within 20% of $V_{IH}$, $V_{IL}$, $T_{RISE}$, and $T_{FALL}$ of clock.
3. If C, $\overline{C}$ are tied high, then K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters.

## Read, Write, and NOP Timing Diagram




**Notes:**
1. Q01 refers to the output from address A. Q02 refers to the output from the next internal burst address following A.
2. Outputs are disabled (high impedance) one clock cycle after a NOP.
3. The second NOP cycle is not necessary for correct device operation, however, at high clock frequencies, it might be required to prevent bus contention.

### IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required.

#### *Signal List*

- TCK: test clock
- TMS: test mode select
- TDI: test data-in
- TDO: test data-out

## JTAG DC Operating Characteristics ($T_A$ = 0 to +70° C)

Operates with JEDEC Standard 8-5 (1.8V) logic signal levels

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| JTAG input high voltage | $V_{IH1}$ | 1.3 | — | $V_{DD}$+0.3 | V | 1 |
| JTAG input low voltage | $V_{IL1}$ | -0.3 | — | 0.5 | V | 1 |
| JTAG output high level | $V_{OH1}$ | $V_{DD}$-0.4 | — | $V_{DD}$ | V | 1, 2 |
| JTAG output low level | $V_{OL1}$ | $V_{SS}$ | — | 0.4 | V | 1, 3 |

1. All JTAG inputs and outputs are LVTTL-compatible.
2. $I_{OH1} \geq$ -|2mA|
3. $I_{OL1} \geq$ +|2mA|.

## JTAG AC Test Conditions ($T_A$ = 0 to +70° C, $V_{DD}$ = 1.8V -5%, +5%)

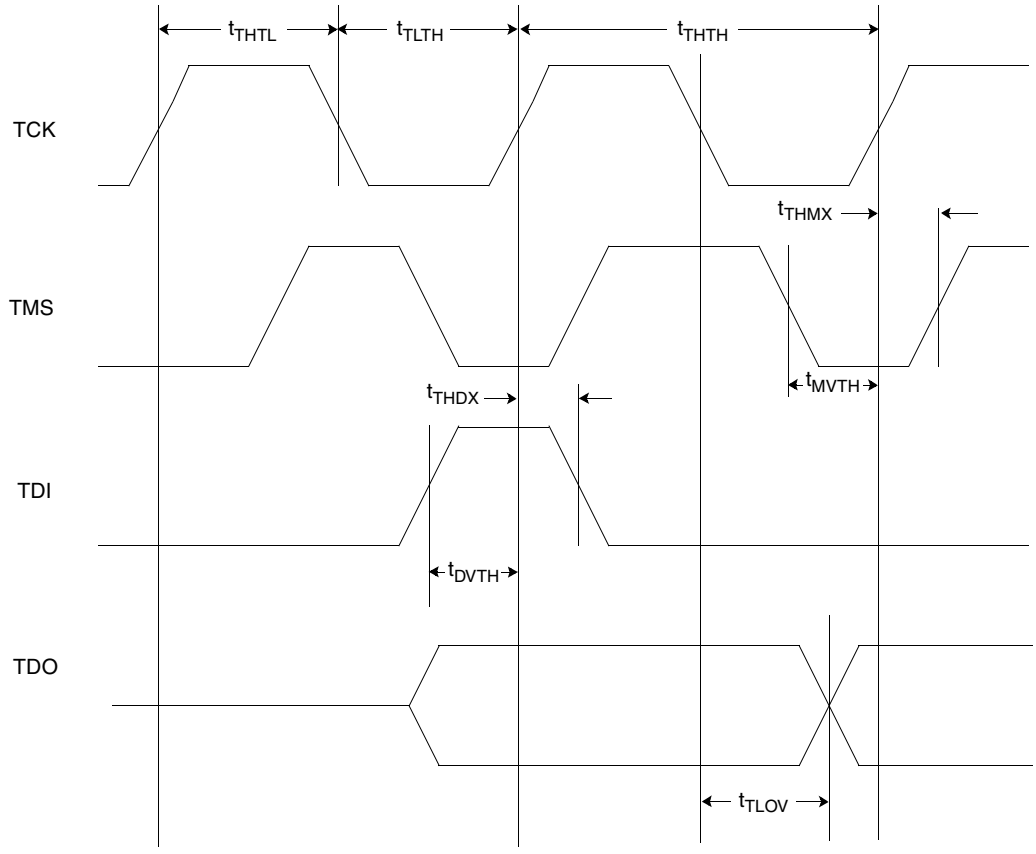
| Parameter | Symbol | Conditions | Units |
|---|---|---|---|
| Input pulse high level | $V_{IH1}$ | 1.3 | V |
| Input pulse low level | $V_{IL1}$ | 0.5 | V |
| Input rise time | $T_{R1}$ | 1.0 | ns |
| Input fall time | $T_{F1}$ | 1.0 | ns |
| Input and output timing reference level | | 0.9 | V |

## JTAG AC Characteristics ($T_A$ = 0 to +70° C, $V_{DD}$ = 1.8V -5%, +5%)

| Parameter | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| TCK cycle time | $t_{THTH}$ | 20 | — | ns | |
| TCK high pulse width | $t_{THTL}$ | 7 | — | ns | |
| TCk low pulse width | $t_{TLTH}$ | 7 | — | ns | |
| TMS setup | $t_{MVTH}$ | 4 | — | ns | |
| TMS hold | $t_{THMX}$ | 4 | — | ns | |
| TDI setup | $t_{DVTH}$ | 4 | — | ns | |
| TDI hold | $t_{THDX}$ | 4 | — | ns | |
| TCK low to valid data | $t_{TLOV}$ | — | 7 | ns | 1 |

1. See *AC Test Loading* on page 15.

## JTAG Timing Diagram



## Scan Register Definition

| Register Name | Bit Size x18 or x36 |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 109 |

## ID Register Definition

| Part | Field Bit Number and Description | | | |
|---|---|---|---|---|
| | Revision Number (31:29) | Part Configuration (28:12) | JEDEC Code (11:1) | Start Bit (0) |
| 4M x 18 | 000 | 00def0wx0t0q0b0s0 | 000 101 001 00 | 1 |
| 2M x 36 | 000 | 00def0wx0t0q0b0s0 | 000 101 001 00 | 1 |

**Part Configuration Definition**:
def = 011 for 72Mb
wx = 11 for x36, 10 for x18
t = 1 for DLL, 0 for non-DLL
q = 1 for QUADB4, 0 for DDR-II
b = 1 for burst of 4, 0 for burst of 2
s = 1 for separate I/0, 0 for common I/O

## Instruction Set

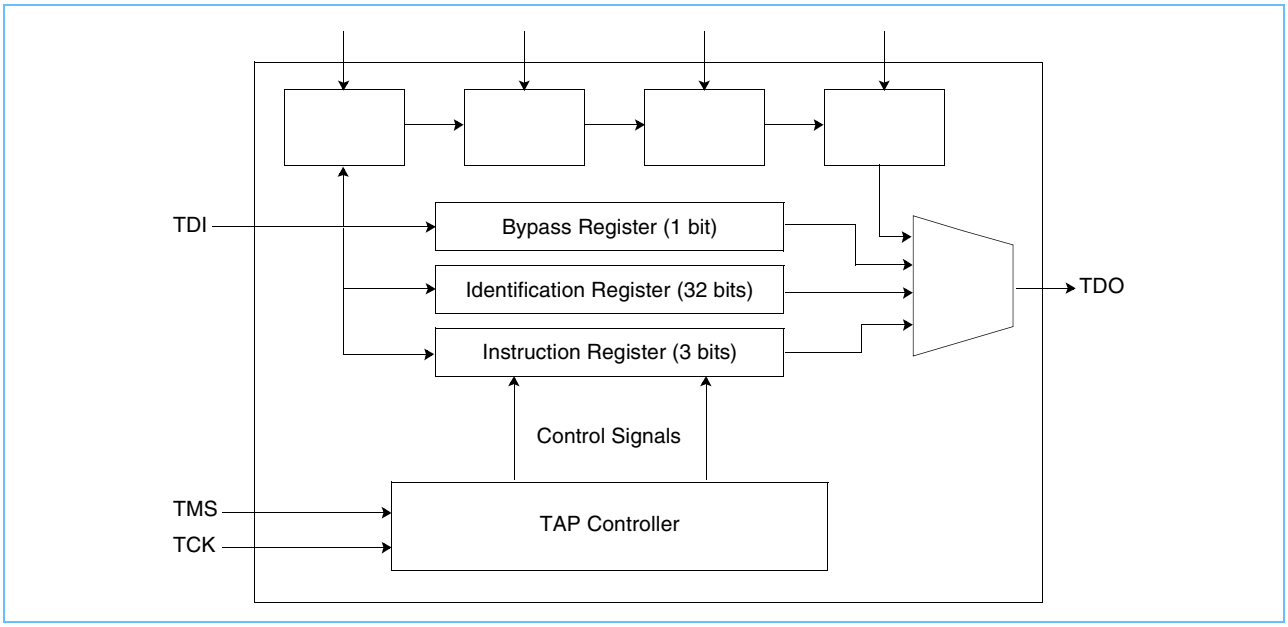
| Code | Instruction | TDO Output | Notes |
|---|---|---|---|
| 000 | EXTEST | Boundary Scan Register | 2,6 |
| 001 | IDCODE | 32-bit Identification Register | |
| 010 | SAMPLE-Z | Boundary Scan Register | 1, 2 |
| 011 | PRIVATE | Do not use | 5 |
| 100 | SAMPLE | Boundary Scan Register | 4 |
| 101 | PRIVATE | Do not use | 5 |
| 110 | PRIVATE | Do not use | 5 |
| 111 | BYPASS | Bypass Register | 3 |

1. Places Qs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to $V_{SS}$ when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place DQs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places Q in high-Z. If the internal register on the scan chain is set high, Q will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

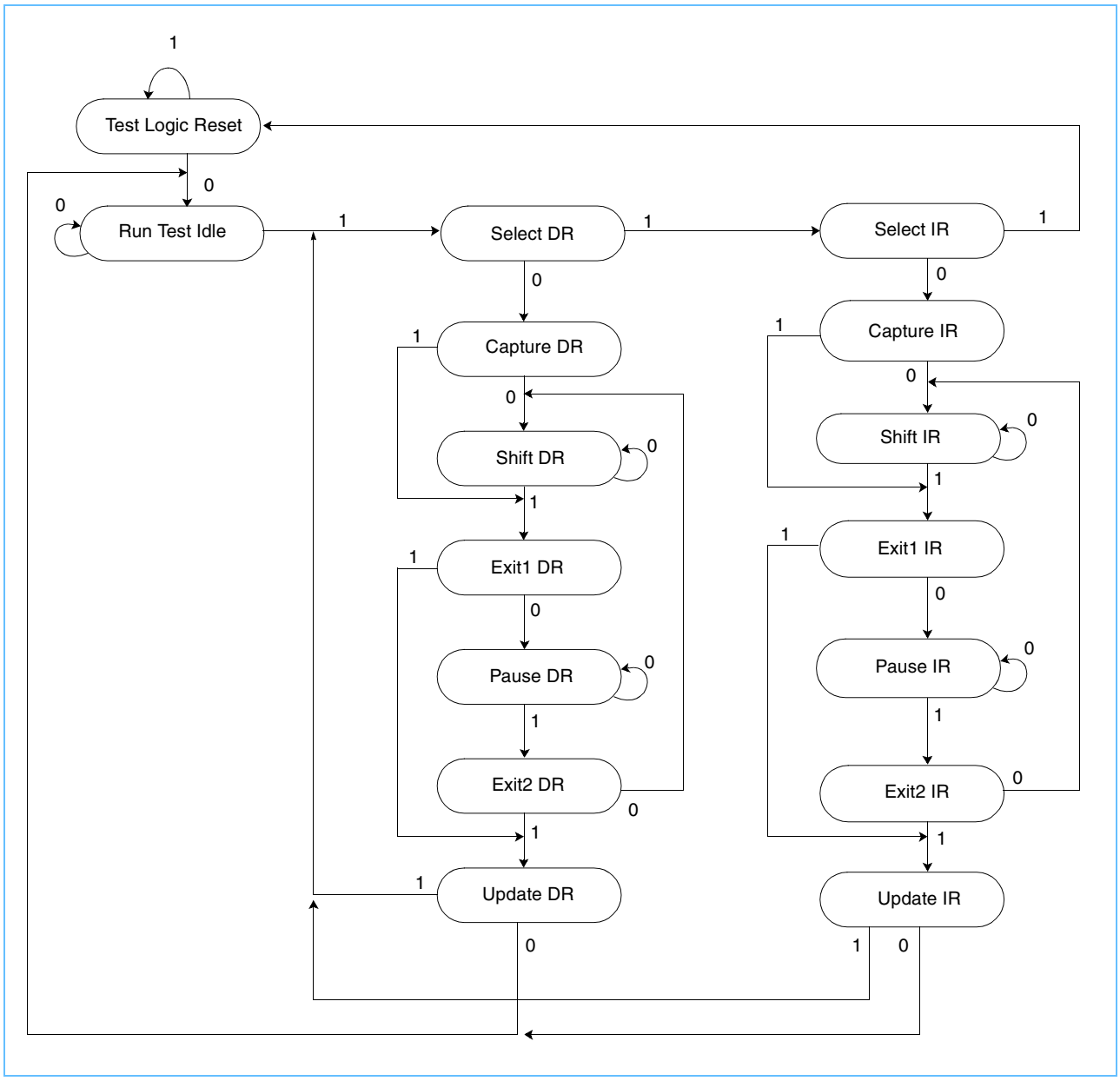
### List of IEEE 1149.1 Standard Violations

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

## JTAG Block Diagram



## TAP Controller State Machine



**Boundary Scan Exit Order** The same length is used for x18 and x36 I/O configuration.

| Order | Pin ID |
|---|---|
| 1 | 6R |
| 2 | 6P |
| 3 | 6N |
| 4 | 7P |
| 5 | 7N |
| 6 | 7R |
| 7 | 8R |
| 8 | 8P |
| 9 | 9R |
| 10 | 11P |
| 11 | 10P |
| 12 | 10N |
| 13 | 9P |
| 14 | 10M |
| 15 | 11N |
| 16 | 9M |
| 17 | 9N |
| 18 | 11L |
| 19 | 11M |
| 20 | 9L |
| 21 | 10L |
| 22 | 11K |
| 23 | 10K |
| 24 | 9J |
| 25 | 9K |
| 26 | 10J |
| 27 | 11J |
| 28 | 11H |
| 29 | 10G |
| 30 | 9G |
| 31 | 11F |
| 32 | 11G |
| 33 | 9F |
| 34 | 10F |
| 35 | 11E |
| 36 | 10E |

| Order | Pin ID |
|---|---|
| 37 | 10D |
| 37 | 9E |
| 39 | 10C |
| 40 | 11D |
| 41 | 9C |
| 42 | 9D |
| 43 | 11B |
| 44 | 11C |
| 45 | 9B |
| 46 | 10B |
| 47 | 11A |
| 48 | 10A |
| 49 | 9A |
| 50 | 8B |
| 51 | 7C |
| 52 | 6C |
| 53 | 8A |
| 54 | 7A |
| 55 | 7B |
| 56 | 6B |
| 57 | 6A |
| 58 | 5B |
| 59 | 5A |
| 60 | 4A |
| 61 | 5C |
| 62 | 4B |
| 63 | 3A |
| 64 | 2A |
| 65 | 1A |
| 66 | 2B |
| 67 | 3B |
| 68 | 1C |
| 69 | 1B |
| 70 | 3D |
| 71 | 3C |
| 72 | 1D |

| Order | Pin ID |
|---|---|
| 73 | 2C |
| 74 | 3E |
| 75 | 2D |
| 76 | 2E |
| 77 | 1E |
| 78 | 2F |
| 79 | 3F |
| 80 | 1G |
| 81 | 1F |
| 82 | 3G |
| 83 | 2G |
| 84 | 1H |
| 85 | 1J |
| 86 | 2J |
| 87 | 3K |
| 88 | 3J |
| 89 | 2K |
| 90 | 1K |
| 91 | 2L |
| 92 | 3L |
| 93 | 1M |
| 94 | 1L |
| 95 | 3N |
| 96 | 3M |
| 97 | 1N |
| 98 | 2M |
| 99 | 3P |
| 100 | 2N |
| 101 | 2P |
| 102 | 1P |
| 103 | 3R |
| 104 | 4R |
| 105 | 4P |
| 106 | 5P |
| 107 | 5N |
| 108 | 5R |
| 109 | Internal |

1) NC pins as defined on *FBGA pinouts* on page 2 are read as “don’t cares”.
2) State of Internal pin (#109) is loaded via JTAG.

| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MAX. | NOM. | MIN. |
| A | — | — | 1.40 | — | — | 0.055 |
| A1 | 0.27 | — | 0.46 | 0.011 | — | 0.018 |
| b | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| D | 16.90 | 17.00 | 17.10 | 0.665 | 0.669 | 0.673 |
| D1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 14.90 | 15.00 | 15.10 | 0.587 | 0.591 | 0.594 |
| E1 | 9.90 | 10.00 | 10.10 | 0.390 | 0.394 | 0.398 |
| e | 1.00 BSC | | | 0.039 BSC | | |

NOTE :

1. Controlling dimension : mm

| | | | | |
|---|---|---|---|---|
| TITLE | 165L 15x17mm LF-BGA Package Outline | REV. | B | DATE 12/10/2007 |

## ORDERING INFORMATION

### Commercial Range: 0°C to +70°C

| Speed | Order Part No. | Organization | Package |
|---|---|---|---|
| 300 MHz | IS61DDB42M36-300M3 | 2Mx36 | 165 BGA |
| | IS61DDB42M36-300M3L | 2Mx36 | 165 BGA, Lead-free |
| | IS61DDB44M18-300M3 | 4Mx18 | 165 BGA |
| | IS61DDB44M18-300M3L | 4Mx18 | 165 BGA, Lead-free |
| 250 MHz | IS61DDB42M36-250M3 | 2Mx36 | 165 BGA |
| | IS61DDB42M36-250M3L | 2Mx36 | 165 BGA, Lead-free |
| | IS61DDB44M18-250M3 | 4Mx18 | 165 BGA |
| | IS61DDB44M18-250M3L | 4Mx18 | 165 BGA, Lead-free |