

HD74HC299

8-bit Universal Shift/Storage Register (with 3-state outputs)

REJ03D0609-0200
(Previous ADE-205-488)
Rev.2.00
Jan 31, 2006

Description

The HD74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and 3-state feature, this device is ideally suited for interfacing with bus lines in a bus oriented system. Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S_0 and S_1 high. This places the 3-state outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding clear input is provided to clear the register whether the outputs are enabled or disabled.

Features

- High Speed Operation
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC299FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HC299RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

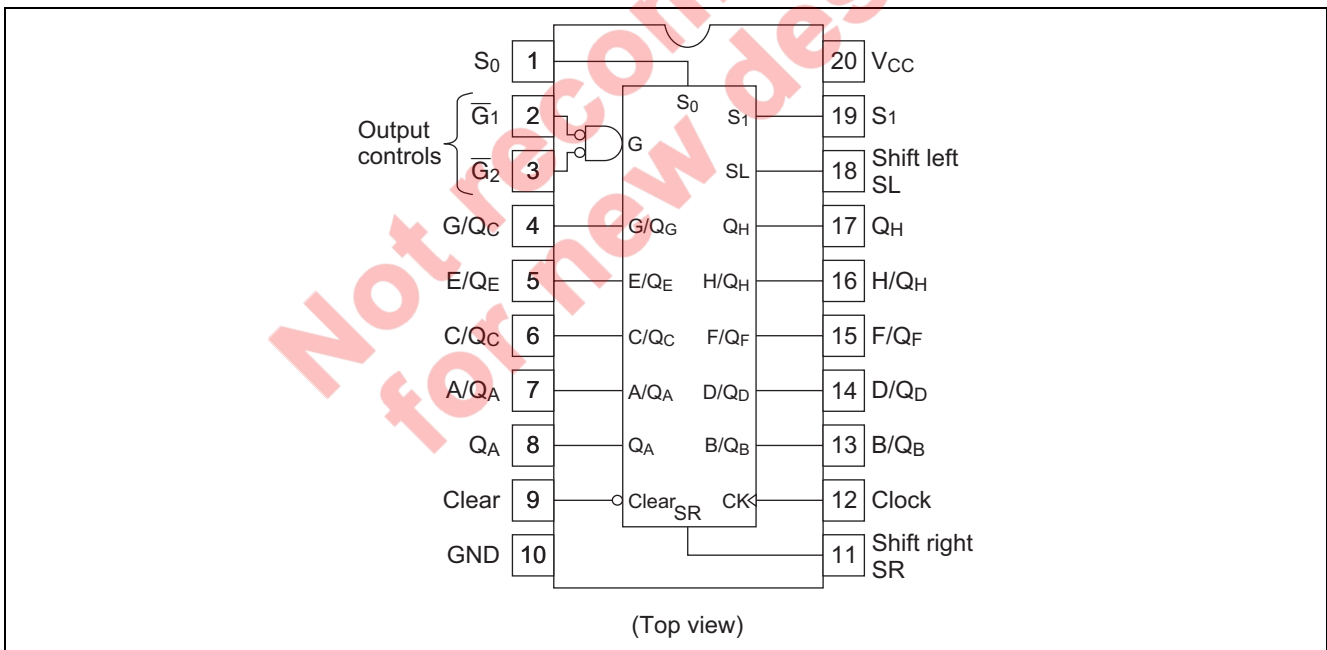
Note: Please consult the sales office for the above package availability.

Function Table

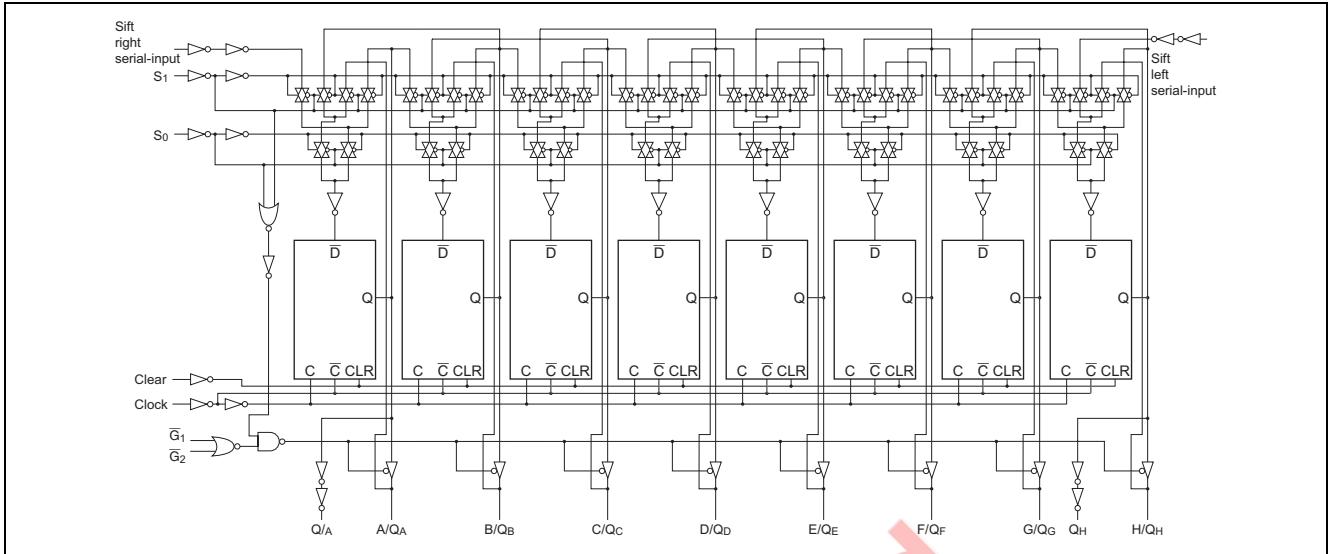
Mode	Inputs								Inputs/Outputs								Outputs		
	Clear	Function Select		Output Control		Clock	Serial										Q _A '	Q _H '	
		S ₁	S ₀	$\overline{G}_1 \uparrow$	$\overline{G}_2 \uparrow$		S _L	S _R	A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H			
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}	
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}	
Shift Right	H	L	H	L	L	\downarrow	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}	
	H	L	H	L	L	\downarrow	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}	
Shift Left	H	H	L	L	L	\downarrow	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H	
	H	H	L	L	L	\downarrow	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L	
Load	H	H	H	X	X	\downarrow	X	X	a	b	c	d	e	f	g	h	a	h	

- Notes:
1. a to h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.
 2. Q_{A0} to Q_{H0}; the level of Q_A through Q_H, respectively, before the indicated steady-state input conditions were established.
 3. Q_{An} to Q_{Hn}; the level of Q_A through Q_H, respectively, before the most-recent \downarrow transition of the clock.
 4. \uparrow ; When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.
 5. When clear is low, outputs of Q_A' and Q_H' are low, in spite of other inputs.

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	$^{\circ}C$	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions			
			Min	Typ	Max	Min	Max					
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V				
		4.5	3.15	—	—	3.15	—					
		6.0	4.2	—	—	4.2	—					
	V _{IL}	2.0	—	—	0.5	—	0.5	V				
		4.5	—	—	1.35	—	1.35					
		6.0	—	—	1.8	—	1.8					
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA		
		4.5	4.4	4.5	—	4.4	—					
		6.0	5.9	6.0	—	5.9	—					
		4.5	4.18	—	—	4.13	—		Q _A ' & Q _H ' Outputs	I _{OH} = -4 mA		
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA		
		4.5	4.18	—	—	4.13	—		A/Q _A thru H/Q _H Outputs	I _{OH} = -6 mA		
		6.0	5.68	—	—	5.63	—			I _{OH} = -7.8 mA		
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA		
		4.5	—	0.0	0.1	—	0.1					
		6.0	—	0.0	0.1	—	0.1					
		4.5	—	—	0.26	—	0.33				Q _A ' & Q _H ' Outputs	I _{OH} = 4 mA
		6.0	—	—	0.26	—	0.33					I _{OH} = 5.2 mA
		4.5	—	—	0.26	—	0.33				A/Q _A thru H/Q _H Outputs	I _{OH} = 6 mA
		6.0	—	—	0.26	—	0.33					I _{OH} = 7.8 mA
Off-state output current	I _{oz}	6.0	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND			
Quiescent supply current	I _{cc}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA			

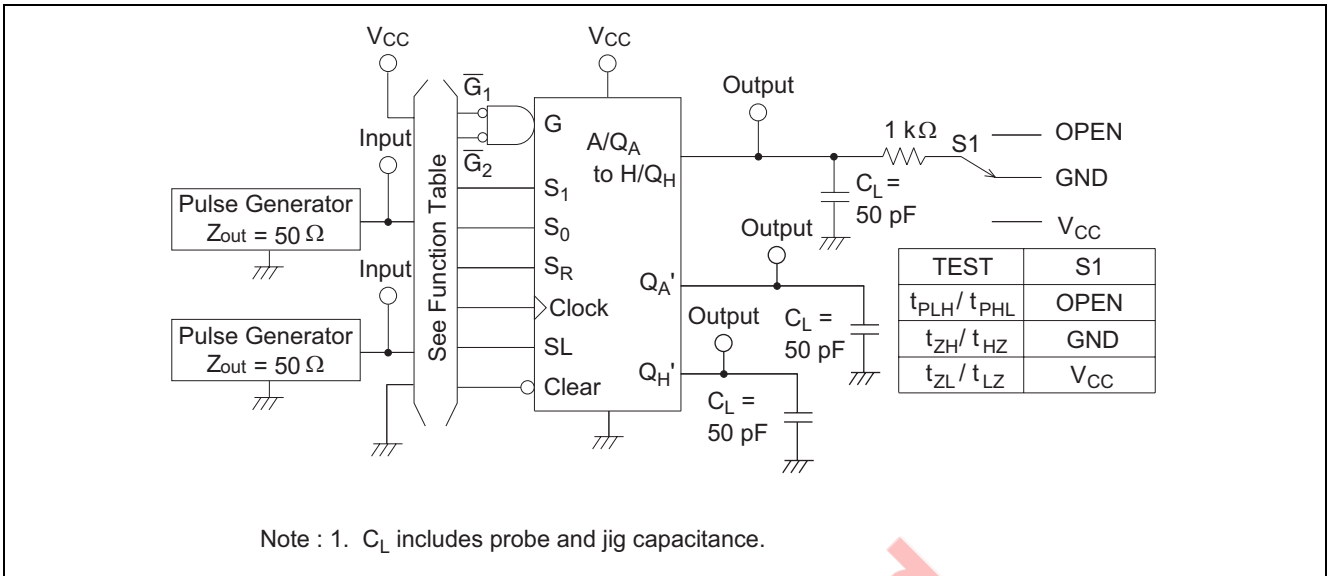
Not recommended for new designs

Switching Characteristics

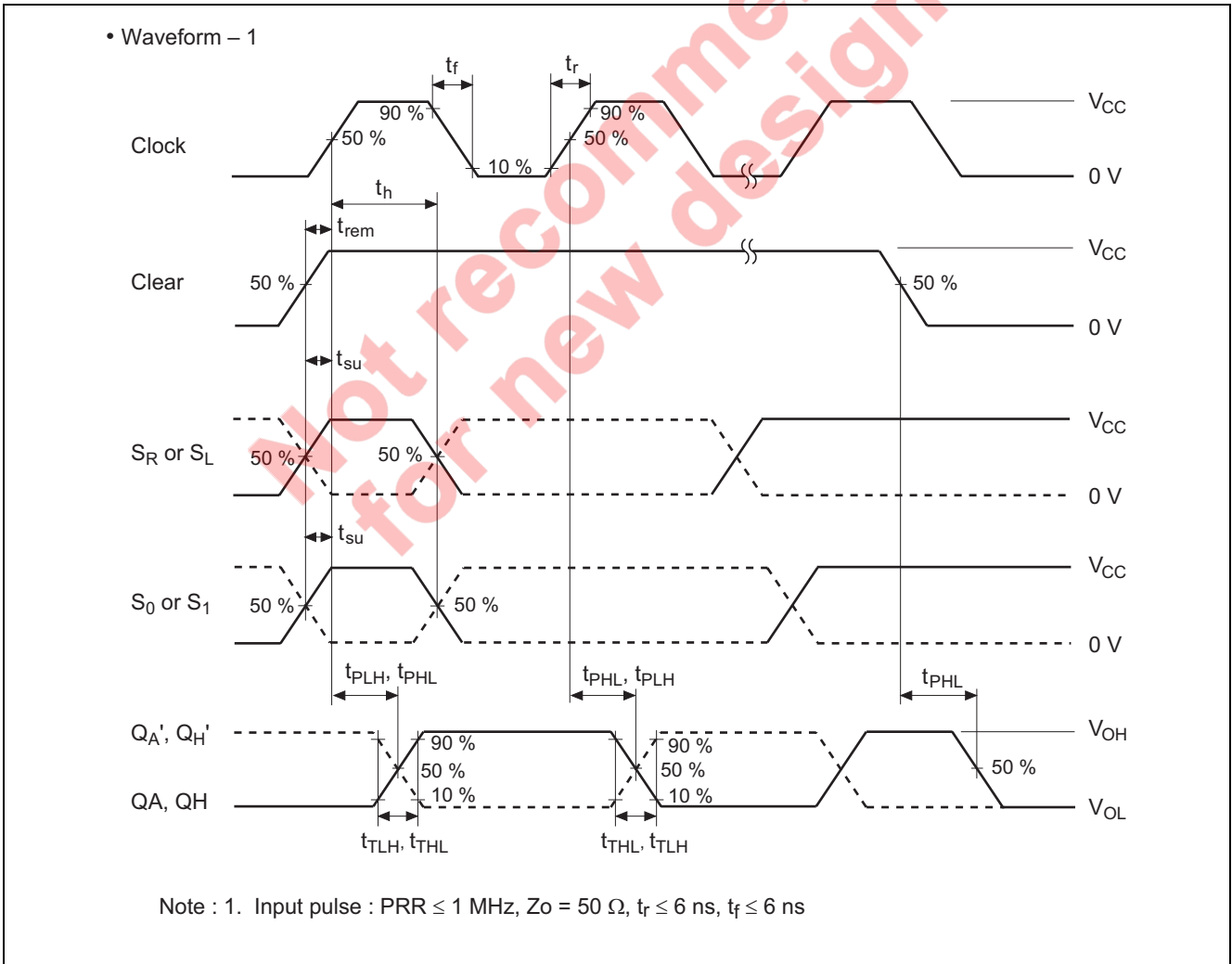
($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	23		
Propagation delay time	t _{PLH}	2.0	—	—	190	—	240	ns	Clock to Q _A ' or Q _H '
		4.5	—	—	38	—	48		
		6.0	—	—	32	—	41		
	t _{PHL}	2.0	—	—	220	—	275	ns	Clear to Q _A ' or Q _H '
		4.5	—	—	44	—	55		
		6.0	—	—	37	—	47		
	t _{PLH}	2.0	—	—	190	—	240	ns	Clock to Q _A – Q _H
		4.5	—	—	38	—	48		
		6.0	—	—	32	—	41		
	t _{PHL}	2.0	—	—	220	—	275	ns	Clear to Q _A – Q _H
		4.5	—	—	44	—	55		
		6.0	—	—	37	—	47		
Output enable time	t _{ZH}	2.0	—	—	160	—	200	ns	
		4.5	—	—	32	—	40		
		6.0	—	—	27	—	34		
Output disable time	t _{LZ}	2.0	—	—	160	—	200	ns	
		4.5	—	—	32	—	40		
		6.0	—	—	27	—	34		
Setup time	t _{su}	2.0	100	—	—	125	—	ns	Select
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t _h	2.0	5	—	—	5	—	ns	Select
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t _{rem}	2.0	50	—	—	65	—	ns	Clear
		4.5	10	—	—	13	—		
		6.0	9	—	—	11	—		
Pulse width	t _w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t _{TLH}	2.0	—	—	60	—	75	ns	A/Q _A thru H/Q _H outputs
		4.5	—	—	12	—	15		
		6.0	—	—	10	—	13		
	t _{THL}	2.0	—	—	75	—	95	ns	Q _A ' & Q _H ' outputs
		4.5	—	—	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

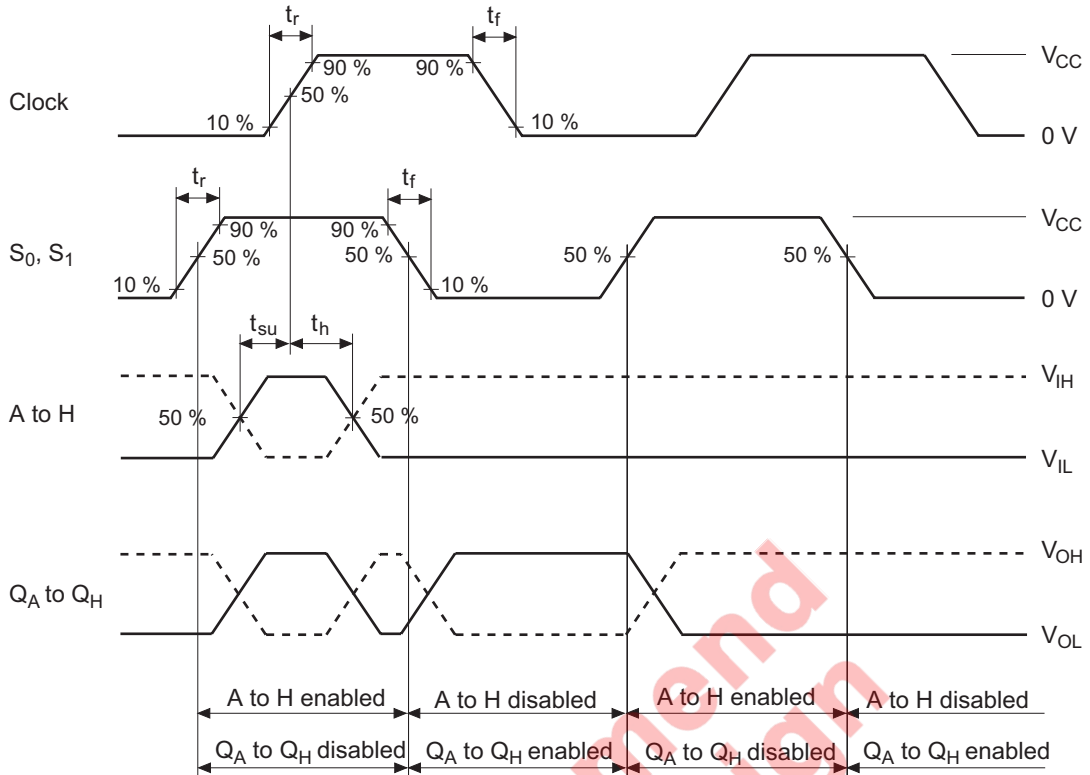
Test Circuit



Waveforms

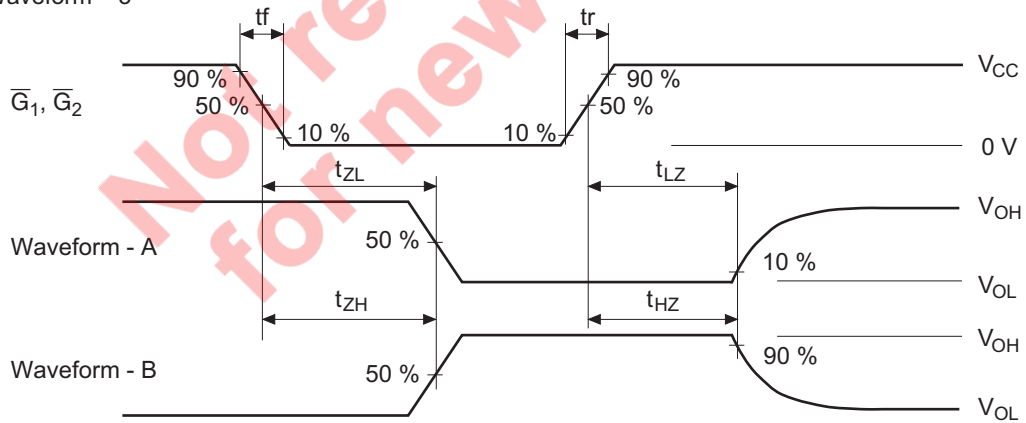


• Waveform – 2



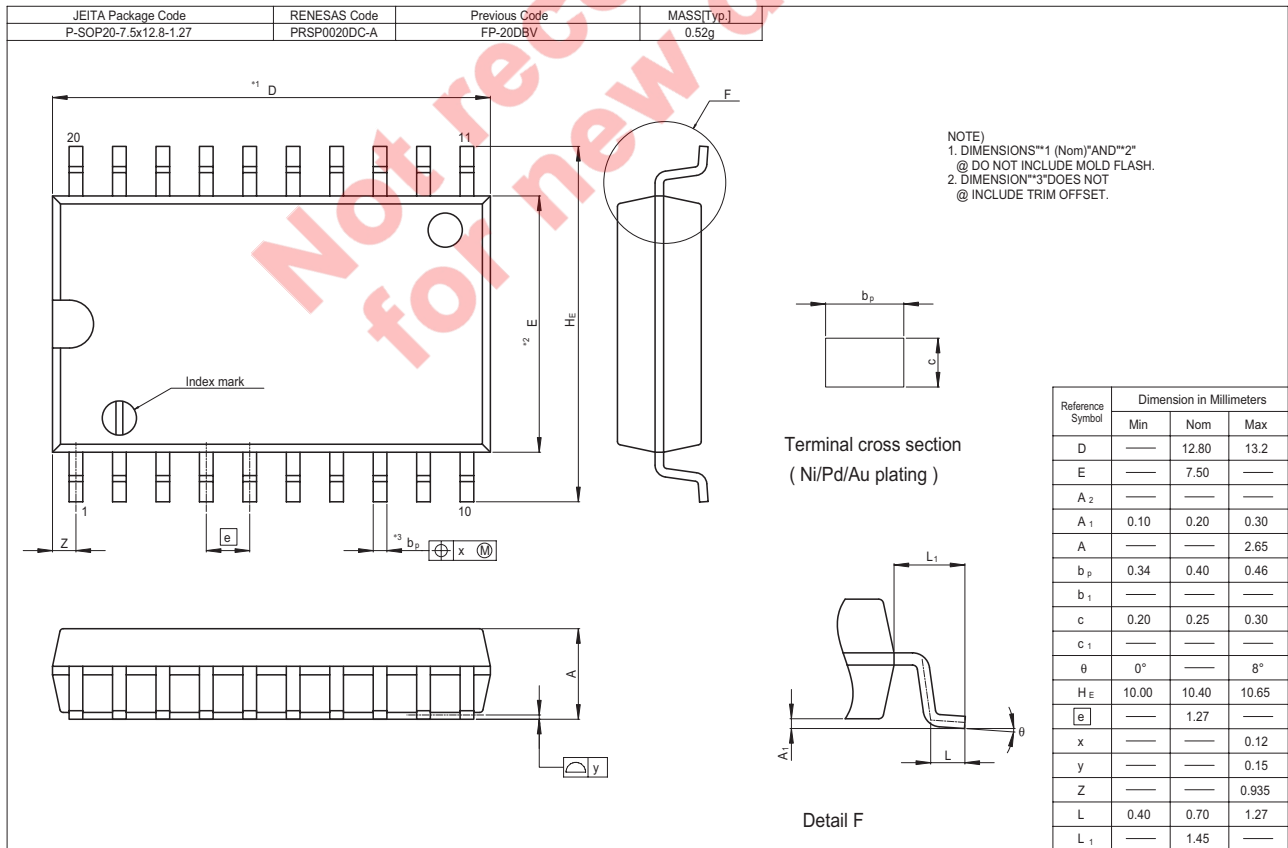
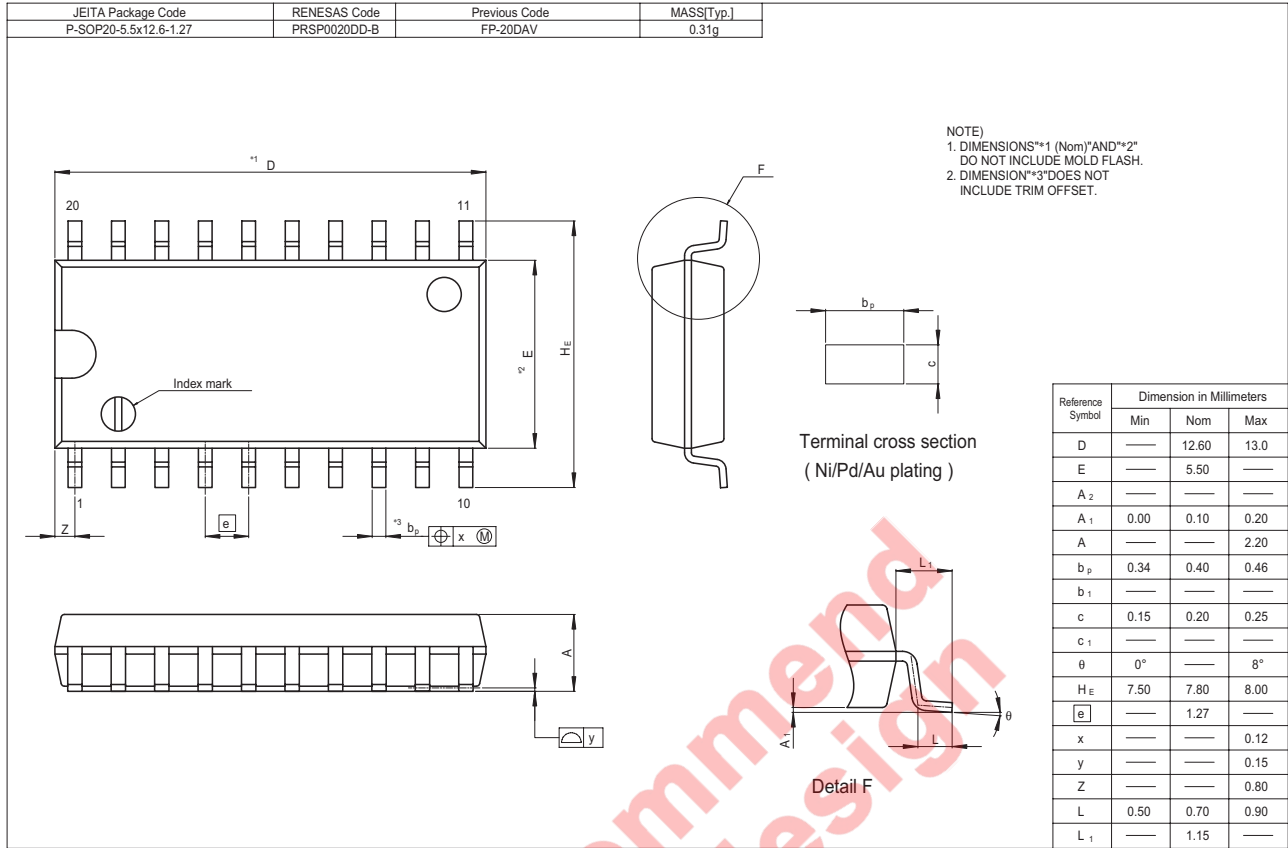
Note : 1. Input pulse : PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns

• Waveform – 3



- Notes : 1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns
- 2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
- 3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
- 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510