

Silicon NPN Power Transistors

2SC2307

DESCRIPTION

- With TO-3PN package
- High voltage ,high speed

APPLICATIONS

- For power switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

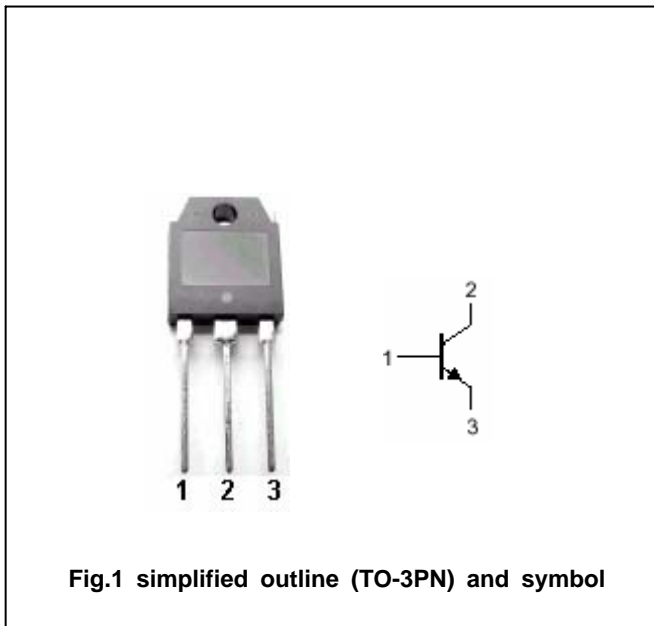


Fig.1 simplified outline (TO-3PN) and symbol

Absolute maximum ratings(Ta=25)

SYMBOL	PARAMETER	CONDITIONS	MAX	UNIT
V_{CBO}	Collector-base voltage	Open emitter	500	V
V_{CEO}	Collector-emitter voltage	Open base	400	V
V_{EBO}	Emitter-base voltage	Open collector	7	V
I_C	Collector current (DC)		12	A
P_C	Collector power dissipation	$T_C=25$	100	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =25mA ; I _B =0	400			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =1mA ; I _E =0	500			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	7			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =7A; I _B =1.4A			0.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =7A; I _B =1.4A			1.3	V
I _{CBO}	Collector cut-off current	V _{CB} =500V; I _E =0			100	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =7V; I _C =0			100	μ A
h _{FE}	DC current gain	I _C =7A ; V _{CE} =4V	10			
f _T	Transition frequency	I _C =1A ; V _{CE} =12V		18		MHz

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PACKAGE OUTLINE

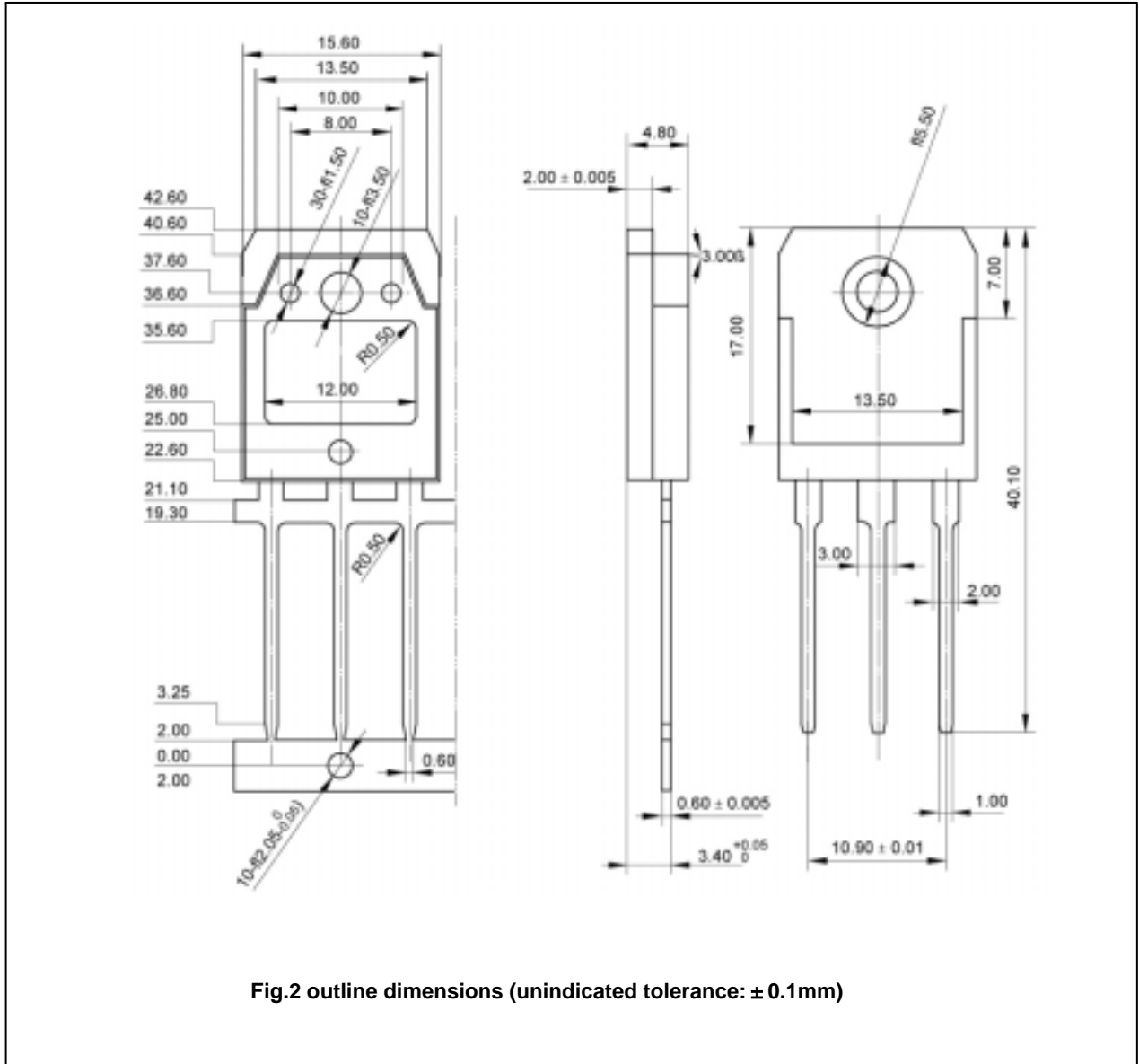


Fig.2 outline dimensions (unindicated tolerance: ± 0.1 mm)