3.3V ‘SpreadTrak’ Zero Delay Buffer

Features

- Zero input - output propagation delay, adjustable by capacitive load on FBK input.
- Multiple configurations - Refer “ASM5P23S04A Configurations Table”.
- Input frequency range: 15 MHz to 133 MHz
- Multiple low-skew outputs.
- Output-output skew less than 200 pS.
- Device-device skew less than 500 pS.
- Two banks of two outputs each.
- Less than 200 pS cycle-to-cycle jitter
  - (-1, -1H, -2, -2H).
- Available in space saving, 8-pin 150-mil SOIC package.
- 3.3V operation.
- Advanced 0.35μ CMOS technology.
- Industrial temperature available.
- ‘SpreadTrak’.

Functional Description

ASM5P23S04A is a versatile, 3.3V zero-delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. It is available in a 8-pin package. The part has an on-chip PLL, which locks to an input clock, presented on the REF pin. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input-to-output propagation delay is guaranteed to be less than 250 pS, and the output-to-output skew is guaranteed to be less than 200 pS.

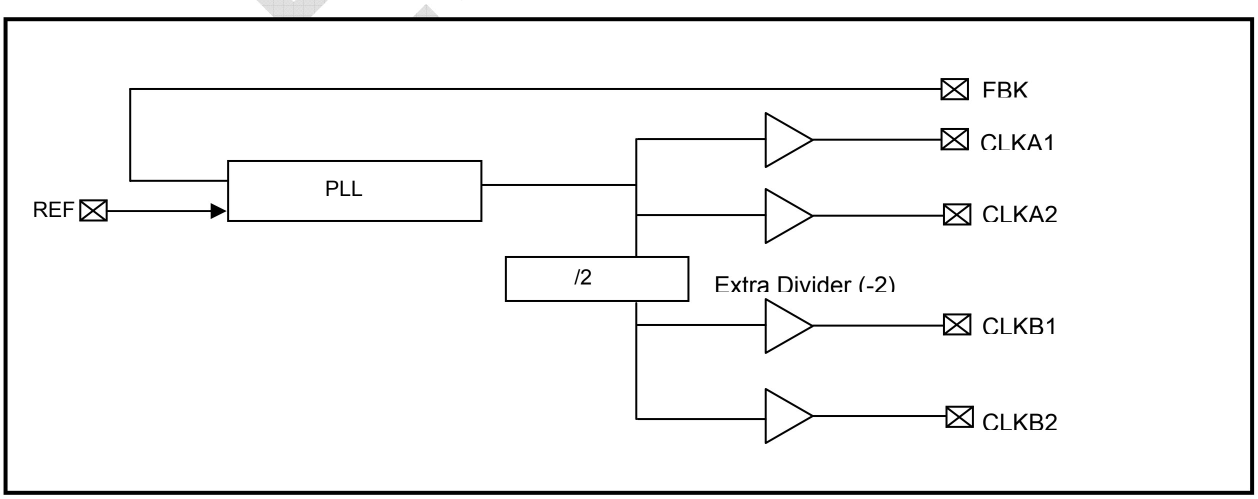
The ASM5P23S04A has two banks of two outputs each. Multiple ASM5P23S04A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 500 pS.

The ASM5P23S04A is available in two different configurations (Refer “ASM5P23S04A Configurations Table). The ASM5P23S04A-1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The ASM5P23S04A-1H is the high-drive version of the -1 and the rise and fall times on this device are much faster.

The ASM5P23S04A-2 allows the user to obtain Ref and 1/2X frequencies on each output bank. The exact configuration and output frequencies depend on which output drives the feedback pin.

The ASM5P23S04A-2H is a high-drive version with REF/2 on both banks.

Block Diagram



PRELIMINARY

PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200, Campbell, CA 95008 • Tel: 408-879-9077 • Fax: 408-879-9018
www.pulsecoresemi.com

Notice: The information in this document is subject to change without notice.

ASM5P23S04A Configurations

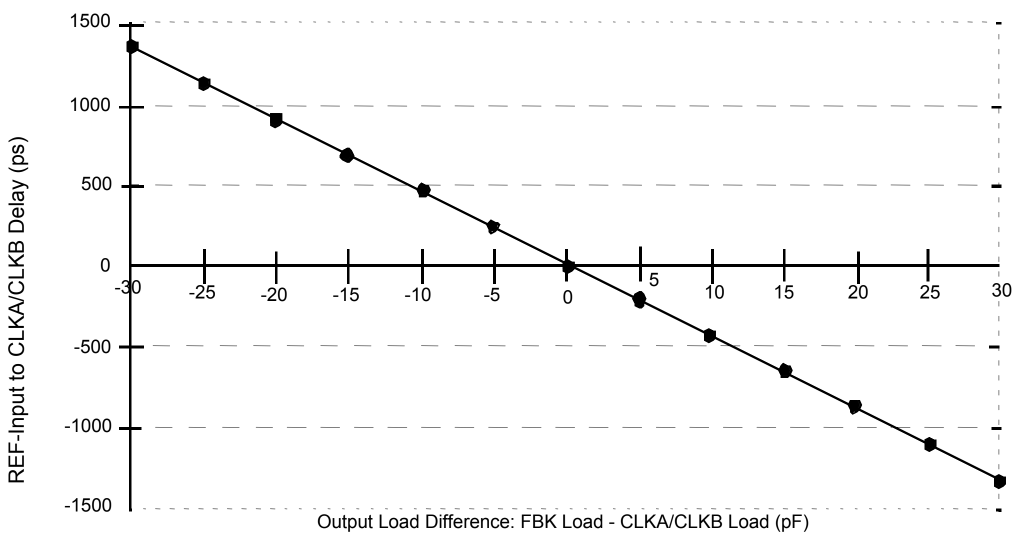
Device	Feedback From	Bank A Frequency	Bank B Frequency
ASM5P23S04A-1	Bank A or Bank B	Reference	Reference
ASM5P23S04A-1H	Bank A or Bank B	Reference	Reference
ASM5P23S04A-2	Bank A or Bank B	Reference	Reference /2
ASM5P23S04A-2H	Bank A or Bank B	Reference	Reference /2

'SpreadTrak'

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. ASM5P23S04A is designed so as not to filter off the Spread Spectrum feature of the Reference Input, assuming it exists. When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

Zero Delay and Skew Control

For applications requiring zero input-output delay, all outputs must be equally loaded.



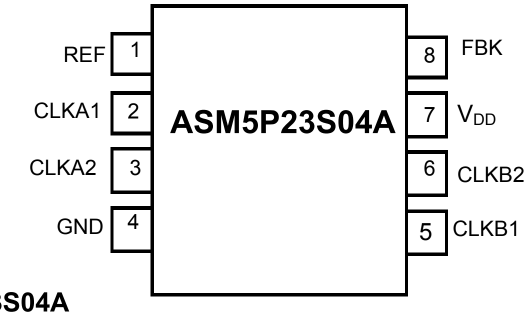
REF Input to CLKA/CLKB Delay Vs Difference in Loading between FBK pin and CLKA/CLKB pins

To close the feedback loop of the ASM5P23S04A, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs. For zero output-output skew, be sure to load outputs equally.

Notice: The information in this document is subject to change without notice.

Pin Configuration



Pin Description for ASM5P23S04A

Pin #	Pin Name	Description
1	REF[1]	Input reference frequency, 5V tolerant input
2	CLKA1[2]	Buffered clock output, bank A
3	CLKA2[2]	Buffered clock output, bank A
4	GND	Ground
5	CLKB1[2]	Buffered clock output, bank B
6	CLKB2[2]	Buffered clock output, bank B
7	V_{DD}	3.3V supply
8	FBK	PLL feedback input

Notes:

1. Weak pull-down.
2. Weak pull-down on all outputs.

Notice: The information in this document is subject to change without notice.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	+7.0	V
DC Input Voltage (Except REF)	-0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	-0.5	7	V
Storage Temperature	-65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)		>2000	V
Note: These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.			

Operating Conditions for ASM5P23S04A Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[3]		7	pF

Note:
3. Applies to both Ref Clock and FBK.

Notice: The information in this document is subject to change without notice.

Electrical Characteristics for ASM5P23S04A Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	µA
V_{OL}	Output LOW Voltage [4]	I_{OL} = 8mA (-1, -2) I_{OH} = 12mA (-1H, -2H)		0.4	V
V_{OH}	Output HIGH Voltage [4]	I_{OL} = -8mA (-1, -2) I_{OH} = -12mA (-1H, -2H)	2.4		V
I_{DD}	Supply Current	Unloaded outputs 100MHz REF, Select inputs at V_{DD} or GND		TBD	mA
				TBD	
		Unloaded outputs, 66MHz REF (-1, -2)		TBD	
		Unloaded outputs, 33MHz REF (-1, -2)		TBD	

Note:
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Notice: The information in this document is subject to change without notice.

Switching Characteristics for ASM5P23S04A Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30 pF load, All devices	15		100	MHz
$1/t_1$	Output Frequency	20 pF load, -1H, -2H devices	15		133	MHz
$1/t_1$	Output Frequency	15 pF load, -1, -2 devices	15		133	MHz
	Duty Cycle [5]= (t_2 / t_1) * 100 (-1, -2, -1H, -2H)	Measured at 1.4V, F_{OUT} = 66.66 MHz 30 pF load	40.0	50.0	60.0	%
	Duty Cycle [5] = (t_2 / t_1) * 100 (-1, -2,-1H, -2H)	Measured at 1.4V, F_{OUT} = <50 MHz 15 pF load	45.0	50.0	55.0	%
t_3	Output Rise Time [5] (-1, -2)	Measured between 0.8V and 2.0V 30 pF load			2.20	nS
t_3	Output Rise Time [5] (-1, -2)	Measured between 0.8V and 2.0V 15 pF load			1.50	nS
t_3	Output Rise Time [5] (-1H, -2H)	Measured between 0.8V and 2.0V 30 pF load			1.50	nS
t_4	Output Fall Time [5] (-1, -2)	Measured between 2.0V and 0.8V 30 pF load			2.20	nS
t_4	Output Fall Time [5] (-1, -2)	Measured between 2.0V and 0.8V 15 pF load			1.50	nS
t_4	Output Fall Time [5] (-1H, -2H)	Measured between 2.0V and 0.8V 30 pF load			1.25	nS
t_5	Output-to-output skew on same bank (-1, -2) [5]	All outputs equally loaded			200	pS
	Output-to-output skew (-1H, -2H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-1, -2H)	All outputs equally loaded			200	
	Output bank A to output bank B skew (-2)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge [5]	Measured at V_{DD} /2		0	±250	pS
t_7	Device-to-Device Skew [5]	Measured at V_{DD}/2 on the FBK pins of the device		0	500	pS
t_8	Output Slew Rate[5]	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/nS
t_J	Cycle-to-cycle jitter [5] (-1, -1H, -2H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			175	pS
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133 MHz, loaded outputs, 15 pF load			100	
t_J	Cycle-to-cycle jitter [5] (-2)	Measured at 66.67 MHz, loaded outputs, 30 pF load			400	pS
		Measured at 66.67 MHz, loaded outputs, 15 pF load			375	
t_{LOCK}	PLL Lock Time [5]	Stable power supply, valid clock presented on REF and FBK pins			1.0	mS

Note:
5. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Notice: The information in this document is subject to change without notice.

Operating Conditions for ASM5I23S04A Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[6]		7	pF

Note:
6. Applies to both Ref Clock and FBK.

Electrical Characteristics for ASM5I23S04A Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage [7]	I_{OL} = 8mA (-1, -2) I_{OH} = 12mA (-1H, -2H)		0.4	V
V_{OH}	Output HIGH Voltage [7]	I_{OL} = -8mA (-1, -2) I_{OH} = -12mA (-1H, -2H)	2.4		V
I_{DD}	Supply Current	Unloaded outputs 100MHz REF, Select inputs at V_{DD} or GND		TBD	mA
				TBD	
		Unloaded outputs, 66MHz REF (-1, -2)		TBD	
		Unloaded outputs, 33MHz REF (-1, -2)		TBD	

Note:
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Notice: The information in this document is subject to change without notice.

Switching Characteristics for ASM5I23S04A Industrial Temperature Devices

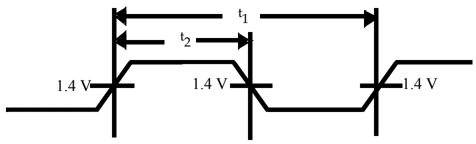
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30 pF load, All devices	15		100	MHz
t_1	Output Frequency	20 pF load, -1H, -2H devices	15		133	MHz
t_1	Output Frequency	15 pF load, -1 and -2 devices	15		133	MHz
	Duty Cycle [8] = (t_2 / t_1) * 100 (-1, -2, -1H, -2H)	Measured at 1.4V, F_{OUT} = <66.66 MHz 30 pF load	40.0	50.0	60.0	%
	Duty Cycle [8]= (t_2 / t_1) * 100 (-1, -2, -1H, -2H)	Measured at 1.4V, F_{OUT} = <50 MHz 15 pF load	45.0	50.0	55.0	%
t_3	Output Rise Time [8] (-1, -2)	Measured between 0.8V and 2.0V 30 pF load			2.50	nS
t_3	Output Rise Time [8] (-1, -2)	Measured between 0.8V and 2.0V 15 pF load			1.50	nS
t_3	Output Rise Time [8] (-1H, -2H)	Measured between 0.8V and 2.0V 30 pF load			1.50	nS
t_4	Output Fall Time [8] (-1, -2)	Measured between 2.0V and 0.8V 30 pF load			2.50	nS
t_4	Output Fall Time [8] (-1, -2)	Measured between 2.0V and 0.8V 15 pF load			1.50	nS
t_4	Output Fall Time [8] (-1H, -2H)	Measured between 2.0V and 0.8V 30 pF load			1.25	nS
t_5	Output-to-output skew on same bank (-1, -2) [8]	All outputs equally loaded			200	pS
	Output-to-output skew (-1H, -2H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-1, -2H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-2)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge [8]	Measured at V_{DD} /2		0	±250	pS
t_7	Device-to-Device Skew [8]	Measured at V_{DD}/2 on the FBK pins of the device		0	500	pS
t_8	Output Slew Rate[8]	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/nS
t_J	Cycle-to-cycle jitter [8] (-1, -1H, -2H)	Measured at 66.67 MHz, loaded outputs,15 pF load			180	pS
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133 MHz, loaded outputs, 15 pF load			100	
t_J	Cycle-to-cycle jitter [8] (-2)	Measured at 66.67 MHz, loaded outputs, 30 pF load			400	pS
		Measured at 66.67 MHz, loaded outputs, 15 pF load			380	
t_{LOCK}	PLL Lock Time [8]	Stable power supply, valid clock presented on REF and FBK pins			1.0	mS

Note:
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

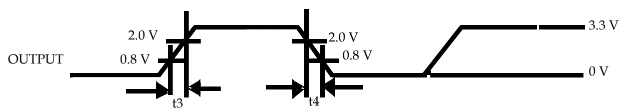
Notice: The information in this document is subject to change without notice.

Switching Waveforms

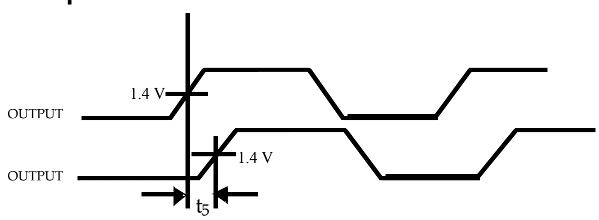
Duty Cycle Timing



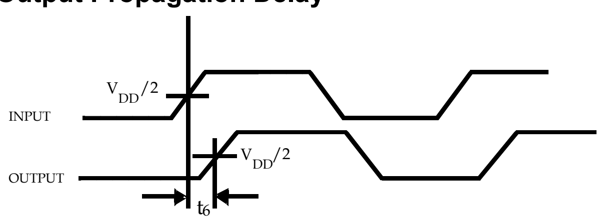
All Outputs Rise/Fall Time



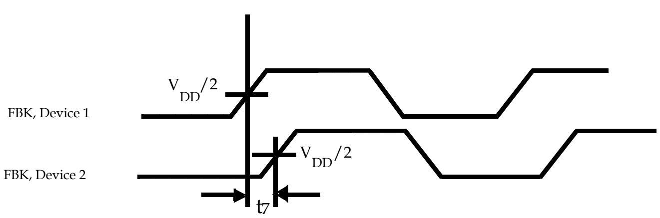
Output - Output Skew



Input - Output Propagation Delay

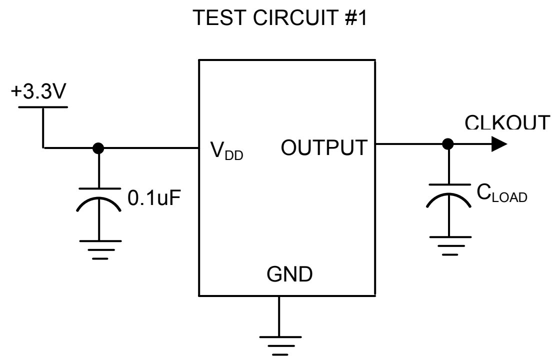


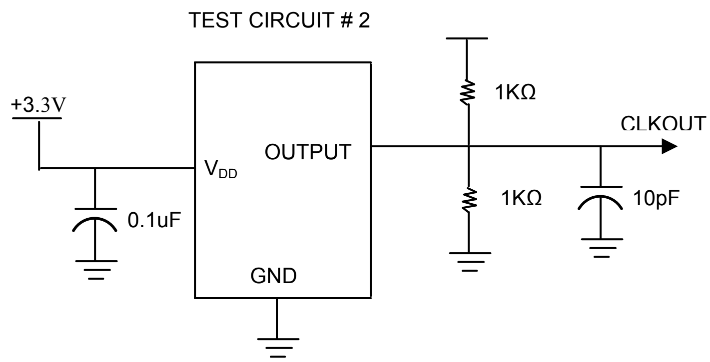
Device - Device Skew



Notice: The information in this document is subject to change without notice.

Test Circuits

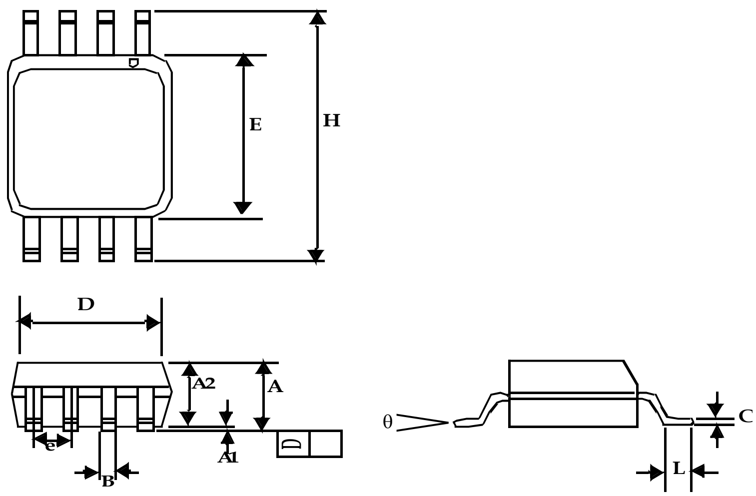




For parameter t_8 (output skew rate) on -1H devices

Notice: The information in this document is subject to change without notice.

Package Information: **8-lead (150 Mil) Molded SOIC**



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Notice: The information in this document is subject to change without notice.

Ordering Codes

Ordering Code	Marking	Package Type	Temperature
ASM5P23S04AF-1-08-SR	5P23S04AF-1	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Commercial
ASM5P23S04AF-1-08-ST	5I23S04AF-1	8-pin 150-mil SOIC-TUBE, Pb free	Commercial
ASM5I23S04AF-1-08-SR	5P23S04AF-1	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Industrial
ASM5I23S04AF-1-08-ST	5I23S04AF-1	8-pin 150-mil SOIC-TUBE, Pb free	Industrial
ASM5P23S04AF-1H-08-SR	5P23S04AF-1H	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Commercial
ASM5P23S04AF-1H-08-ST	5I23S04AF-1H	8-pin 150-mil SOIC-TUBE, Pb free	Commercial
ASM5I23S04AF-1H-08-SR	5P23S04AF-1H	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Industrial
ASM5I23S04AF-1H-08-ST	5I23S04AF-1H	8-pin 150-mil SOIC-TUBE, Pb free	Industrial
ASM5P23S04AF-2-08-SR	5P23S04AF-2	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Commercial
ASM5P23S04AF-2-08-ST	5I23S04AF-2	8-pin 150-mil SOIC-TUBE, Pb free	Commercial
ASM5I23S04AF-2-08-SR	5P23S04AF-2	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Industrial
ASM5I23S04AF-2-08-ST	5I23S04AF-2	8-pin 150-mil SOIC-TUBE, Pb free	Industrial
ASM5P23S04AF-2H-08-SR	5P23S04AF-2H	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Commercial
ASM5P23S04AF-2H-08-ST	5I23S04AF-2H	8-pin 150-mil SOIC-TUBE, Pb free	Commercial
ASM5I23S04AF-2H-08-SR	5P23S04AF2H	8-pin 150-mil SOIC-TAPE & REEL, Pb free	Industrial
ASM5I23S04AF-2H-08-ST	5I23S04AFH	8-pin 150-mil SOIC-TUBE, Pb free	Industrial

Notice: The information in this document is subject to change without notice.

Ordering Codes (Contd…)

Ordering Code	Marking	Package Type	Temperature
ASM5P23S04AG-1-08-SR	5P23S04AG-1	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM5P23S04AG-1-08-ST	5I23S04AG-1	8-pin 150-mil SOIC-TUBE, Green	Commercial
ASM5I23S04AG-1-08-SR	5P23S04AG-1	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM5I23S04AG-1-08-ST	5I23S04AG-1	8-pin 150-mil SOIC-TUBE, Green	Industrial
ASM5P23S04AG-1H-08-SR	5P23S04AG-1H	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM5P23S04AG-1H-08-ST	5I23S04AG-1H	8-pin 150-mil SOIC-TUBE, Green	Commercial
ASM5I23S04AG-1H-08-SR	5P23S04AG-1H	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM5I23S04AG-1H-08-ST	5I23S04AG-1H	8-pin 150-mil SOIC-TUBE, Green	Industrial
ASM5P23S04AG-2-08-SR	5P23S04AG-2	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM5P23S04AG-2-08-ST	5I23S04AG-2	8-pin 150-mil SOIC-TUBE, Green	Commercial
ASM5I23S04AG-2-08-SR	5P23S04AG-2	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM5I23S04AG-2-08-ST	5I23S04AG-2	8-pin 150-mil SOIC-TUBE, Green	Industrial
ASM5P23S04AG-2H-08-SR	5P23S04AG-2H	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM5P23S04AG-2H-08-ST	5I23S04AG-2H	8-pin 150-mil SOIC-TUBE, Green	Commercial
ASM5I23S04AG-2H-08-SR	5P23S04AG2H	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM5I23S04AG-2H-08-ST	5I23S04AGH	8-pin 150-mil SOIC-TUBE, Green	Industrial

Notice: The information in this document is subject to change without notice.

Device Ordering Information

A S M 5 P 2 3 S 0 4 A F - 0 8 T R

R = Tape & Reel, T = Tube or Tray

O = SOT	U = MSOP
S = SOIC	E = TQFP
T = TSSOP	L = LQFP
A = SSOP	U = MSOP
V = TVSOP	P = PDIP
B = BGA	D = QSOP
Q = QFN	X = SC-70

DEVICE PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE, LEAD FREE, and RoHS

PART NUMBER

X= Automotive (-40C to +125C)	I= Industrial (-40C to +85C)	P or n/c = Commercial (0C to +70C)

1 = Reserved	6 = Power Management
2 = Non PLL based	7 = Power Management
3 = EMI Reduction	8 = Power Management
4 = DDR support products	9 = Hi Performance
5 = STD Zero Delay Buffer	0 = Reserved

PulseCore Semiconductor Mixed Signal Product

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

Notice: The information in this document is subject to change without notice.

PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

Copyright © PulseCore Semiconductor
All Rights Reserved
Part Number: ASM5P23S04A
Document Version: 1.4

Note: This product utilizes US# 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

© Copyright 2006 PulseCore Semiconductor Corporation. All rights reserved. Our logo and name are trademarks or registered trademarks of PulseCore Semiconductor. All other brand and product names may be the trademarks of their respective companies. PulseCore reserves the right to make changes to this document and its products at any time without notice. PulseCore assumes no responsibility for any errors that may appear in this document. The data contained herein represents PulseCore's best data and/or estimates at the time of issuance. PulseCore reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. PulseCore does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of PulseCore products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in PulseCore's Terms and Conditions of Sale (which are available from PulseCore). All sales of PulseCore products are made exclusively according to PulseCore's Terms and Conditions of Sale. The purchase of products from PulseCore does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of PulseCore or third parties. PulseCore does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of PulseCore products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify PulseCore against all claims arising from such use.