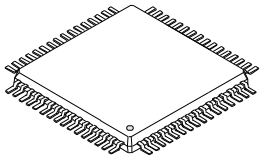
CD DIGITAL SERVO SIGNAL PROCESSOR(SLAVE MODE)

DESCRIPTION

The SC9641 is a single-chip CD processor for digital servo and ASIC circuit. This LSI incorporates CD servo controller, CD signal processor, digital audio DAC and built-in CPU interface.



QFP-64-14 x 14-0.8

FEATURES

* Supports 1X to 2X speed playback
* Command and sub code transmission adopts tri-line communication or parallel communication
* Built-in MCU controls the CD and state feedback by communication instructions of the communication bus.* Supports format of CD-A/V, CD-R, CD-R/W and CD-ROM

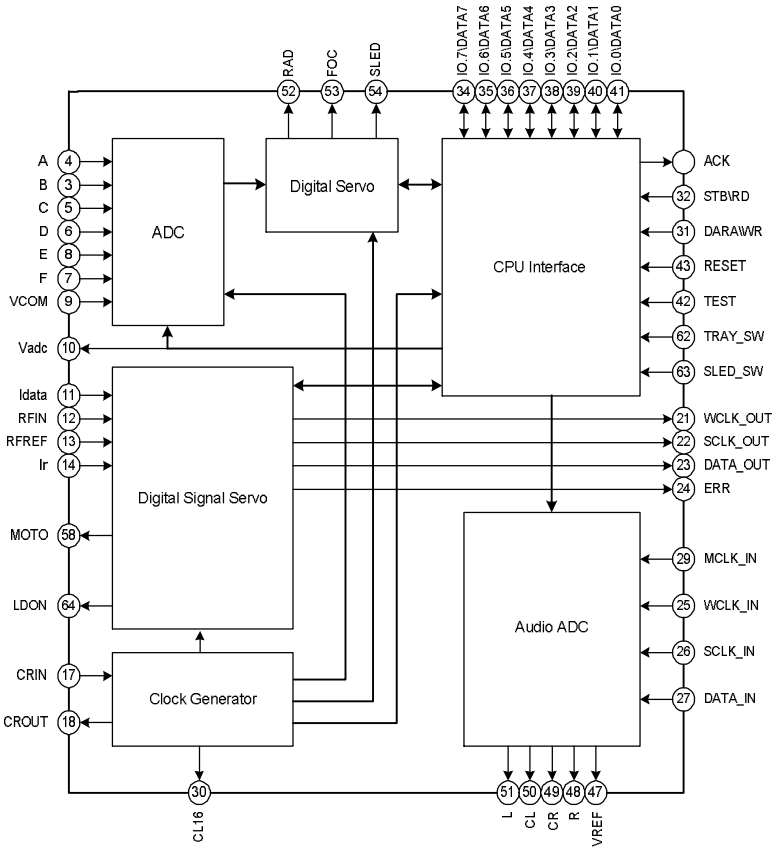
APPLICATIONS

* CD, VCD and MP3 player
* Desk audio system

ORDERING INFORMATION

Device	Package
SC9641	QFP-64-14X14-0.8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 ~ +5.5	V
Input Voltage On Pins	V_{IN}	-0.5 ~ V_{DD} + 0.5	V
Operating Temperature	Tmax	-20 ~ +75	°C

ELECTRICAL CHARACTERISTICS(V_{DD}=3.4~5.5V;V_{SS}=0V;Tamb=-10~+60°C)

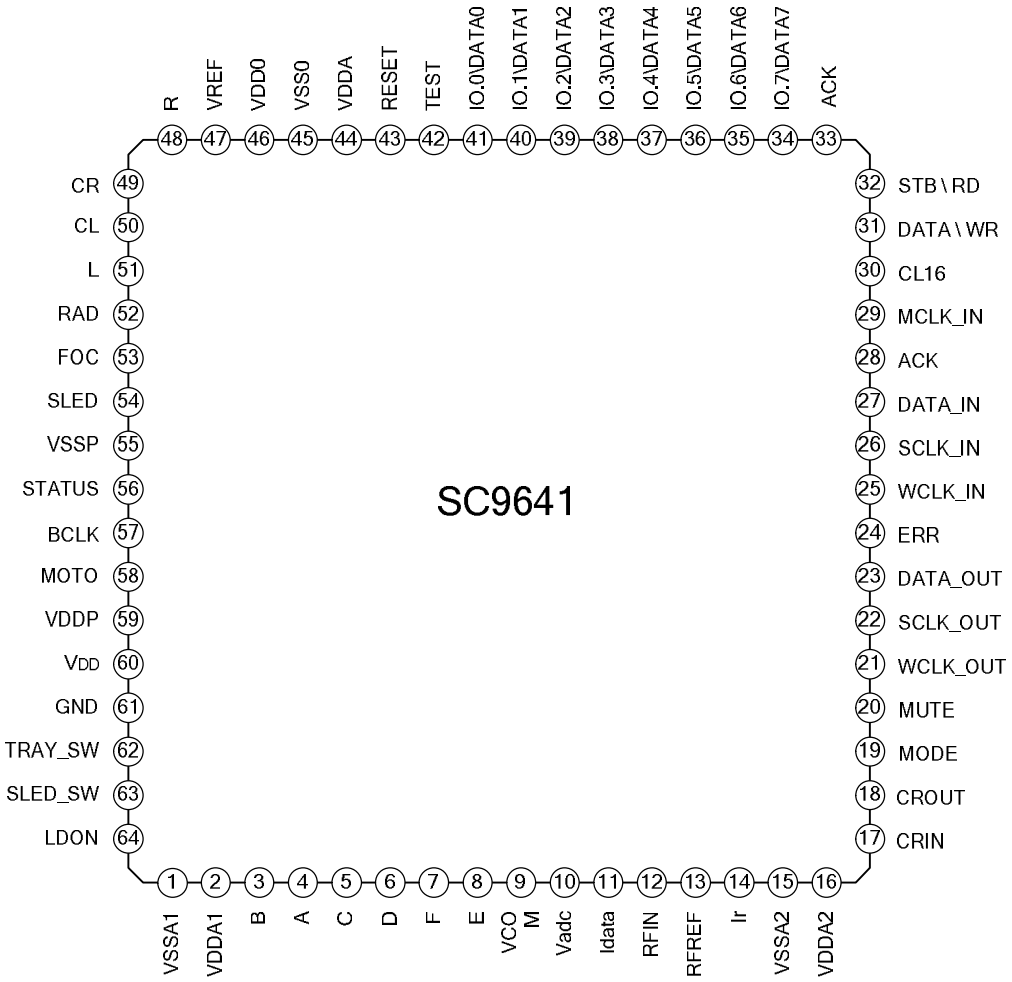
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}	5V; 1X Speed	—	45	—	mA
RFIN Input Signal	V_{RFIN}		—	1.0	—	V
Reference Voltage	V_{Ir}		—	0.5V_{DD}	—	V
Common Mode DC	V_{VCOM}		2.0	2.5	—	V
Output ADC Reference Voltage	V_{Vadc}		V_{VCOM}+ 0.462	—	V_{VCOM}+ 2.313	V
Input Current Of Central Diode B	I_B		0	—	10	μA
Input Current Of Central Diode A	I_A		0	—	10	μA
Input Current Of Central Diode C	I_C		0	—	10	μA
Input Current Of Central Diode D	I_D		0	—	10	μA
Input Current Of Satellite Diode F	I_F		0	—	5	μA
Input Current Of Satellite Diode F	I_E		0	—	5	μA
Data Slicer Feed-back Current Output	I_{Idata}		1.9	—	5.5	μA
LDON Low Level Output Current	I_{LDON}		0	—	2	mA
ERR Output Current	I_{ERR}		0	1	—	mA
DATA_OUT WCLK_OUT SCLK_OUT Output Current	I_{OH1} I_{OL1}		0	1	—	mA
DATA_OUT WCLK_OUT SCLK_OUT Low Level Output Voltage	V_{OL1}	IOL1=1mA	0	—	0.4	V
DATA_OUT WCLK_OUT SCLK_OUT High Level Output Voltage	V_{OH1}	IOH1=-1mA	V_{DD}-0.4	—	V_{DD}	V
RAD Output Current	I_{RAD}		0	1	—	mA
FOC Output Current	I_{FOC}		0	1	—	mA
SLED Output Current	I_{SLED}		0	1	—	mA

(To be continued)

(Continued)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
MOTO Output Current	IMOTO		0	10	—	mA
RAD, FOC, SLED Low Level Output Voltage	VOL	IOL=1mA	0	—	0.4	V
RAD, FOC, SLED High Level Output Voltage	VOH	IOH=-1mA	VDD-0.4	—	VDD	V
Moto Low Level Output Voltage	VOLmoto	IOLmoto=10mA	0	—	1.0	V
Moto high Level Output Voltage	VOHmoto	IOHmoto=-10mA	VDD-1	—	VDD	V
RAD, FOC, SLED, MOTO Output 3-state Leakage Current	IZO		-10	0	+10	μA
ACK, WR, RD, DATA0～7, High Level Input Voltage	VILH		2.8	3.0	-	V
ACK, WR, RD, DATA0～7, Low Level Input Voltage	VIHL		0.6	—	0.7	V
DATA_IN, WCLK_IN, SCLK_IN, High Level Input Voltage	VOHda		0.7VDD	—	VDD+0.5	V
DATA_IN, WCLK_IN, SCLK_IN, Low Level Input Voltage	VOLda		-0.5	—	0.3VDD	V
DAC Total Harmonic Distortion Plus Noise	(THD+N)/S		60	65	70	dB
DA Filter Attenuation	Filter_DA	0~19 kHz	-	-	0.001	dB
		19~20 kHz	-	-	0.03	dB
		24KHz	25	-	-	dB
		25 ~ 35 KHz	40	-	-	dB
		35 ~ 64 KHz	50	-	-	dB
		64 ~68 KHz	31	-	-	dB
		68KHz	35	-	-	dB
		69~ 88KHz	40	-	-	dB
Crystal Frequency	Fsystem		—	16.9344	—	MHz
SCLK Frequency	FSCLK_IN		—	2.8224	—	MHz
WCLK Frequency	FWCLK_IN		—	44.1	—	KHz

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin name	Descriptions
1	VSSA1	Analog Ground 1
2	VDDA1	Analog Supply 1
3	B	Central diode current signal input
4	A	Central diode current signal input
5	C	Central diode current signal input
6	D	Central diode current signal input
7	F	Satellite diode current signal input
8	E	Satellite diode current signal input
9	VCOM	DC voltage input
10	Vadc	ADC reference voltage output
11	Idata	Data signal feed-back current output

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Pin No.	Pin name	Descriptions
12	RFIN	EFM signal input
13	RFREF	Comparator common mode input
14	Ir	Reference current output
15	VSSA2	Analog ground 2
16	VDDA2	Analog supply 2
17	CRIN	Crystal oscillation circuit input. When the master clock is input externally, input it from this pin.
18	CROUT	Crystal oscillation circuit output.
19	MODE	Connect ground.
20	MOT_CTRL	Control the spindle motor (during focusing and jumping, if MOT_CTRL output high level signal, it can control the MOT control port of SA9529 after through 3 voltage drop diodes, then prevent the spindle reverse; in other condition, the MOT-CTRL output low level).
21	WCLK_OUT	D/A interface. LR clock output.
22	SCLK_OUT	D/A interface. Bit clock output.
23	DATA_OUT	D/A interface. Serial data output
24	ERR	C2 error flag
25	WCLK_IN	D/A interface. LR clock input.
26	SCLK_IN	D/A interface. Bit clock input.
27	DATA_IN	D/A interface. Serial data input
28	ACK	Acknowledge Signal output pin (drain open, with pull up resistor).
29	MCLK_IN	DAC system clock input (16.9344MHz)
30	CL16	16.9344MHZ clock output
31	DATA \ WR	Data I/O port, it is shared with write port of parallel communication.
32	STB \ RD	Control I/O port, it is shared with read port of parallel communication.(drain open, with internal pull-up resistor).
33	ACK	Acknowledge signal port (drain open, with internal pull-up resistor).
34	IO.7 \ DATA7	General I/O port, it is shared with data bit 7 (drain open, with internal pull up resistor).
35	IO.6 \ DATA6	General I/O port, it is shared with data bit 6 (drain open, with internal pull up resistor).
36	IO.5 \ DATA5	General I/O port, it is shared with data bit 5 (drain open, with internal pull up resistor).
37	IO.4 \ DATA4	General I/O port, it is shared with data bit 4 (drain open, with internal pull up resistor).
38	IO.3 \ DATA3	General I/O port, it is shared with data bit 3 (drain open, with internal pull up resistor).
39	IO.2 \ DATA2	General I/O port, it is shared with data bit 2 (drain open, with internal pull up resistor).
40	IO.1 \ DATA1	General I/O port, it is shared with data bit 1 (drain open, with internal pull up resistor).
41	IO.0 \ DATA0	General I/O port, it is shared with data bit 0 (drain open, with internal pull up resistor).
42	TEST	Test pin.
43	RESET	Reset pin (active low)
44	VDDA	Analog Supply
45	VSSO	Analog Ground
46	VDD0	Analog Supply

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Pin No.	Pin name	Descriptions
47	VREF	Internal reference voltage for output channels
48	R	Digital audio right channel output pin.
49	CR	Digital audio right channel filter pin.
50	CL	Digital audio left channel filter pin.
51	L	Digital audio left channel output pin.
52	RAD	Tracking drive output
53	FOC	Focus drive output
54	SLED	Sled drive output
55	VSSP	Ground
56	STATUS	Shake signal output (high active, used for anti-seismic system)
57	BCLK	75Hz frame sync signal output pin.
58	MOTO	Spindle drive output.
59	VDDP	Digital power supply.
60	VDD	Digital power supply.
61	GND	Digital ground.
62	TRAY_SW	Tray loading position monitor signal input
63	SLED_SW	Sled motor position monitor signal input
64	LDON	Laser control signal output (active high)

FUNCTION DESCRIPTION

The system controller sets the mode and readout the status of signal processor and digital servo by the standard CPU interface. The detail of command and interface timing is explained in the following tables.

1. SYSTEM WRITE COMMAND TABLE:

COMMAND (HEX)	PARAMETER (BIN)	FUNCTION DESCRIPTIONS
01	XXXXXXXX	Set up 8 general I/O ports, one bit control one I/O port, when the bit is 1, the corresponding port is set input, and it was set output port when it is 0. IO.7~IO.0 corresponding the high bit to least bit. All ports set input status when power on.
03	XXXXXXXX	Set the data of output port. If it is input port, the data is IO.7~IO.0.
08	XXXXXXXX	Set motor speed standard (the initial value is EFH); Motor rotate speed when stable playing: 10000B The low 5 bits set motor rotate speed lower limit: range (00000B~10000B) The high 3 bits set motor rotate upper limit : (10000B~10111B) According to the initial value, if the motor speed is in the range of 01111B~100111B , it consider the motor is stable, and can carry the next operation.

(To be continued)

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COMMAND (HEX)	PARAMETER (BIN)	FUNCTION DESCRIPTIONS
0C	XXXXXXXX	Set shield time of the motor error signal (the initial value is 40H), the parameter is 00H~FFH, the internal reference is 8ms, so the shield time is 0~2 seconds; if the motor rotate speed is detected in the set range, and detect the shield time of motor error signal is exceed, the system consider the servo is abnormally and need restart.
0F	00000010	Start play, if not read TOC, then store the TOC data; when play at the export section, if the sub-controller at normal play state, the system will receive the command of master controller.
	00000011	read and save TOC information again, and stay in the lay in section.
	00000100	Pause.
	00000101	Fast play, at this time, playing at FAST_STEP, and FAST_TIME interval, after fast forward to export section, it entry pause mode, wait for the next command.
	00000110	Fast backward, playing at FAST_STEP, and FAST_TIME interval. After fast backward to import section, it enter pause mode and wait for the command of master controller.
	00000111	Stop play, and switch bare head to inside track.
	00010000	If it is in the lay in section, then jump out the lay in section, and play at the target track. The target track set command: 0X11
	00010001	If it is in the lay in section, then jump out the lay in section, and play at the target track. The target track set command: 0X12, 0X13, 0X14
	00010010	If it is in the lay in section, then jump out the lay in section, and play at the relative time of target track. Set command: 0X11, 0X12, 0X13, 0X14
	00010011	Initialize the servo
	00010100	Closed CD data output.
	00010101	Open CD data output
	00100000	Jump to the next session; if there are a next session, then store the start address of program to the NEXT_AMIN, NEXT_ASEC, NEXT_AFRM; If there are no next session, then the NEXT_AMIN, NEXT_ASEC, NEXT_AFRM remain original value or is 0XFF.
	00100001	Stop at the former play point, the sled motor will not return.
	00100010	This command used for control sled motor in or out after servo stop: 5FH + 81H, 0FH + 21H→ Sled motor sled inside. 5FH + 7FH, 0FH + 21H→Sled motor sled outside. 5FH + 00H, 0FH + 21H→Sled motor stop.

(To be continued)

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COMMAND (HEX)	PARAMETER (BIN)	FUNCTION DESCRIPTIONS
60	XXXXXXXX	Set the high 8 bits (0FFH~00H, it need complement code and the default code is 0FDH) of TRACK when the import section (TOC) jump to normal play section.
61	XXXXXXXX	Set the time of jump to the next session; if it is not jump to the next session in the set time, the sub controller will set the NEXT_AMIN, NEXT_ASEC, NEXT_AFRM is 0XFF; this command is treat with the copy disc.(he unit of the time is 100ms).
63	XXXXXXXX	BIT2, BIT1, BIT0------set SC9641 internal DAC data input format, the default is B110; BIT2: 1----single data input. 0----double data input. BIT1, BIT0: 00---I2S-BUS 10---LSB FIXED 16 BITS 01---LSB FIXED 18 BITS 11---LSB FIXED 20 BITS BIT7, BIT6: Improve play capability of difficult read disk. 00---normal (default) 01--- one step higher than 00 10--- one step higher than 01 11--- one step higher than 11 (this setting is the easiest read disk, if the disk is not readable in one time in the normal setting, this two bits can set to 11 to read the disk easily) BIT5: IMPROVE PLAY CAPABILITY OF difficult readable disk, can set with BIT6, BIT7. 0--- normal(default) 1--- read disk more easy (the setting is the same as BIT6, BIT7)
0D	10110011	Set 1x speed play
	10111011	Set 2X speed play
	1010XXXX	Set voltage Vadc
	00111010	Set data output format: I^2S-BUS CD-ROM mode
	00111011	Set data output format: EIAJ CD-ROM mode
	00111110	Set data output format: I^2S-BUS 16-BIT FS mode
	00110010	Set data output format: EIAJ 16-BITS FS MODE
11	XXXXXXXX	set TARGET TNO
12	XXXXXXXX	set TARGET minute
13	XXXXXXXX	set TARGET second
14	XXXXXXXX	set TARGET frame
15	XXXXXXXX	Set jump frame range.
16	XXXXXXXX	Set fast forward and fast backward steps (TRACK).
17	XXXXXXXX	Set step time (10ms)
18	XXXXXXXX	Set NEG FRAME of jump target (0~255)

2. SYSTEM READ COMMAND TABLE:

COMMAND (HEX)	PARAMETER (BIN)	FUNCTION DESCRIPTIONS
02	XXXXXXXX	Read the value of IO.7~IO.0D, if it as output port, it read the output data.
81	MINTNO	The minimum target(HEX)
82	MAXTNO	The maximum track no (HEX)
83	NEXT_AMIN	The absolute time (minute) of the next session (BCD).
84	NEXT_ASEC	The absolute time (second) of the next session (BCD).
85	NEXT_AFRM	The absolute time (frame) of the next session (BCD).
86	MAXMIN	Maximum play time- min(HEX)
87	MAXSEC	Maximum play time- sec(HEX)
89	MAXFRM	Maximum play time- frame(HEX)
8A	XXXXXX0X	Not store TOC information
	XXXXXX1X	Store TOC information
	XXXXX0XX	Not enter play status
	XXXXX1XX	Enter play status
	XXXX0XXX	Not enter pause status
	XXXX1XXX	Enter pause status
	XXX0XXXX	Not enter pause status
	XXX1XXXX	Enter fast forward status
	XX0XXXXX	Not enter fast backward status
	XX1XXXXX	Enter fast backward status
	X0XXXXXX	Not enter stop status
	X1XXXXXX	Enter stop status
	0XXXXXXX	Not initialize servo parameter
	1XXXXXXX	Initialize servo parameter
8B	XXXXXXX0	1x, 2x speed switch over.
	XXXXXXX1	1x, 2x speeds not switch over.
	XXXXXX0X	Not find the set target and playing.
	XXXXXX1X	Find the set target and playing.
	XXXXX0XX	Servo normal.
	XXXXX1XX	Servo stop, resuming.
	XXXX0XXX	Not detect no disc
	XXXX1XXX	Detect no disc+
	XXX0XXXX	Play not at the target track.
	XXX1XXXX	Playing at the target track.
	XX0XXXXX	Open CD output.
	XX1XXXXX	Close CD output.
	X0XXXXXX	1x speed play status.
	X1XXXXXX	2x speed play status.
	0XXXXXXX	Not fast forward the export section or not fast backward the import section.
	1XXXXXXX	It is have been fast forward the export section or fast backward to the lay in section or play to the export section.

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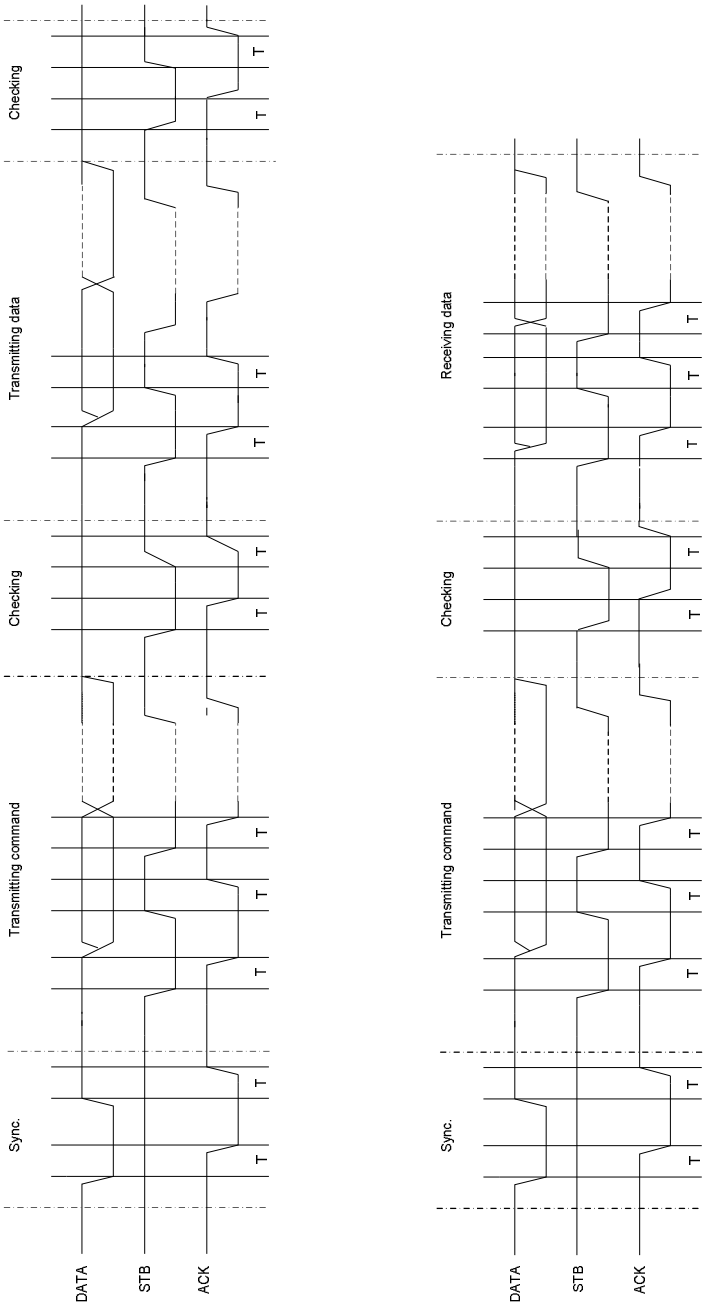
COMMAND (HEX)	PARAMETER (BIN)	FUNCTION DESCRIPTIONS
9A	XXXXX0XX	TRAY_SW=0
	XXXXX1XX	TRAY_SW=1
A0	QCODE0	CTRLADR (BCD)disc mode code.
A1	QCODE1	TNO (BCD) Tone no.
A2	QCODE2	IX (BCD) index no.
A3	QCODE3	RMIN (BCD) relative time-minute
A4	QCODE4	RSEC (BCD) relative time-second
A5	QCODE5	RSEC (BCD) relative time- frame
A6	QCODE6	ZERO (BCD)
A7	QCODE7	AMIN (BCD) absolute time-minute
A8	QCODE8	ASEC (BCD) absolute time-second
A9	QCODE9	AFRAME (BCD) absolute time-frame
AA	QCODE0~9	Continue read ten Q sub-code (BCD code), this command is active in the parallel mode.
DD	000XXXXX	Read motor speed information, normal play: b00010000, stop : b00000000，when the motor is accelerated from 0 to stable play, if it is exceed the b00010000, it will stabilization at b00010000.

3. CPU INTERFACE TIMING



Note:

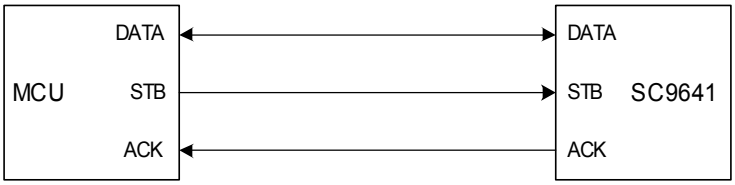
The interface protocol adopt fixed communication format. Every frame includes 24 bits, where 16 bits data code, and 8 bits verify code.

COMMAND (8bits) + CHECK(4bits) + DATA(8bits) + CHECK(4bits)

4 bits verify code is obtained from high 4 bits XOR low 4 bits of the former 8 bits code.

The 8 bits DATA code is the master controller send to SC9641, or the SC9641 request read code. If the COMMAND not set value, then the DATA after COMMAND is invalid, but the DATA cannot omit. COMMAND and DATA send code from MSB to LSB. SC9641 operation according the master controller command and it is single initiative communication.

4. INTERFACE DESCRIPTION



DATA (pin 31): synchronization and data transmission.

STB (pin 32): low level active.

ACK (pin 33): acknowledge signal

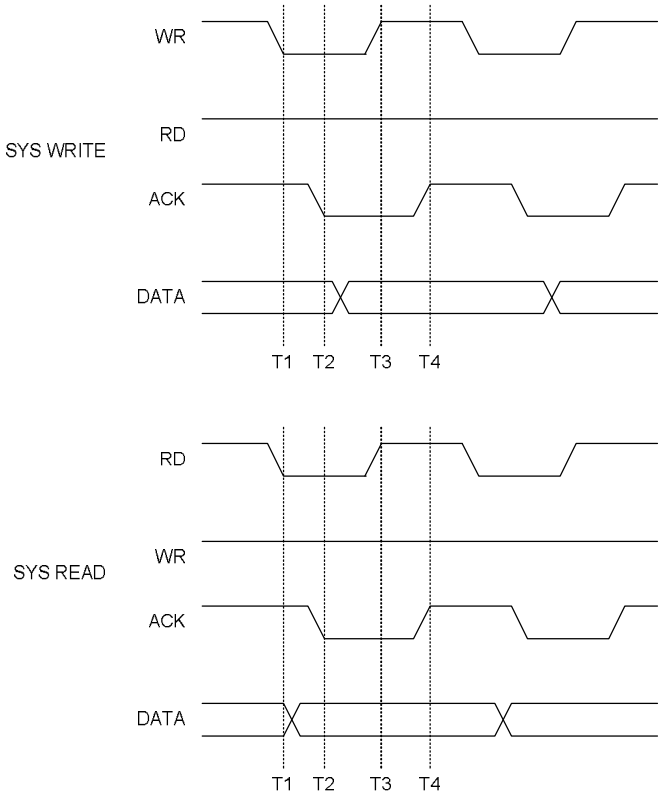
1. Master controller transmit data

1) The master controller transmitted data is COMMAND or PARAMETER. Every frame of data transmit, the master controller start to synchronize, transmit the 8 bits command, then transmit the 4 bits check data, if sub-controller pass the check data, following transmit continuance or read the command.
2) The ACK send out acknowledge signal, if the sub-controller received data is match to CHECK data, ACK signal become low indicate the check passed; if it is not match, ACK signal keep high level, then exit this communicate. The master controller will operating with the ACK station, the data line keep high when checking the data.
3) In the transmitting, if the master controller or sub-controller not response the request in some time (T<1000us), the system regard this transmit error. The master controller will exit and repeat again or produce other errors.
4) In the transmitting, the master controller transmits the DATA when the ACK is low, and the transmitted DATA is available at STB is high, SC9641 complete write 1 bit after ACK become high.

2. Master controller receive data

1) After master controller transmitted the data code, the sub-controller check the 8 bits command, if it is match the check data, then send the request data to master controller. The STB of master controller complete this process.
2) After transmit the 12 bits data, the sub-controller complete this communication. The master controller check the 12 bits data, if it is match the check data, this communication complete, the receive data available. And if it is not match, the receive data invalid, the master controller transmit the read again command, but it won't transmit check data.
3) In the receiving, if the master controller or sub-controller not response the request in some time (T<1000us), the system regard this receive error. The master controller will exit and repeat again or produce other error.
4) In the receiving, the sub-controller receive the DATA when the ACK is low, and the DATA is read out at STB is high, SC9641 complete read 1 bit after ACK become high.

5. PARALLEL COMMUNICATION TIMING WAVEFORM



Note: WR (pin 31), RD (pin 32) is controlled by system (master controller), and ACK (pin 28) is controlled by SC9641 (sub-controller), normal state is high level, and DATA is controlled by all above.

1) Write mode: ACK_H
   a. The system set WR: begin to write operation: MSB (T1).
   b. The system wait SC9641 acknowledge: MSB (T2)
   c. After the system write data to the DATA port, set the WR: LSB (T3).
   d. The system wait for the response of SC9641: LSB (T4)
   (After SC9641 read the data, set ACK: LSB)
   e. After write one byte, according to the a→ b → c → d order write the next byte.
2) Read mode: ACK_H
   a. The system set RD: MSB (T1), and begin to read operation.
   b. The system wait for SC9461 response ACK: MSB (T2) (SC9641 set ACK after data ready: MSB)
   c. After the system read out the data, set the RD: LSB (T3).
   d. The system wait for the response of SC9641: LSB (T4).
   e. After read one byte, according to the a→ b → c → d order perform the next byte read operation.
3) Time of communication protocol:
   a. system read (SYS READ):
      T2-T1: >=7us
      T3-T2: =5us (TYP.), related with the execute speed of master controller.
      T4-T3: >=6us

b. system write (SYS WRITE):

T2-T1: >=6us

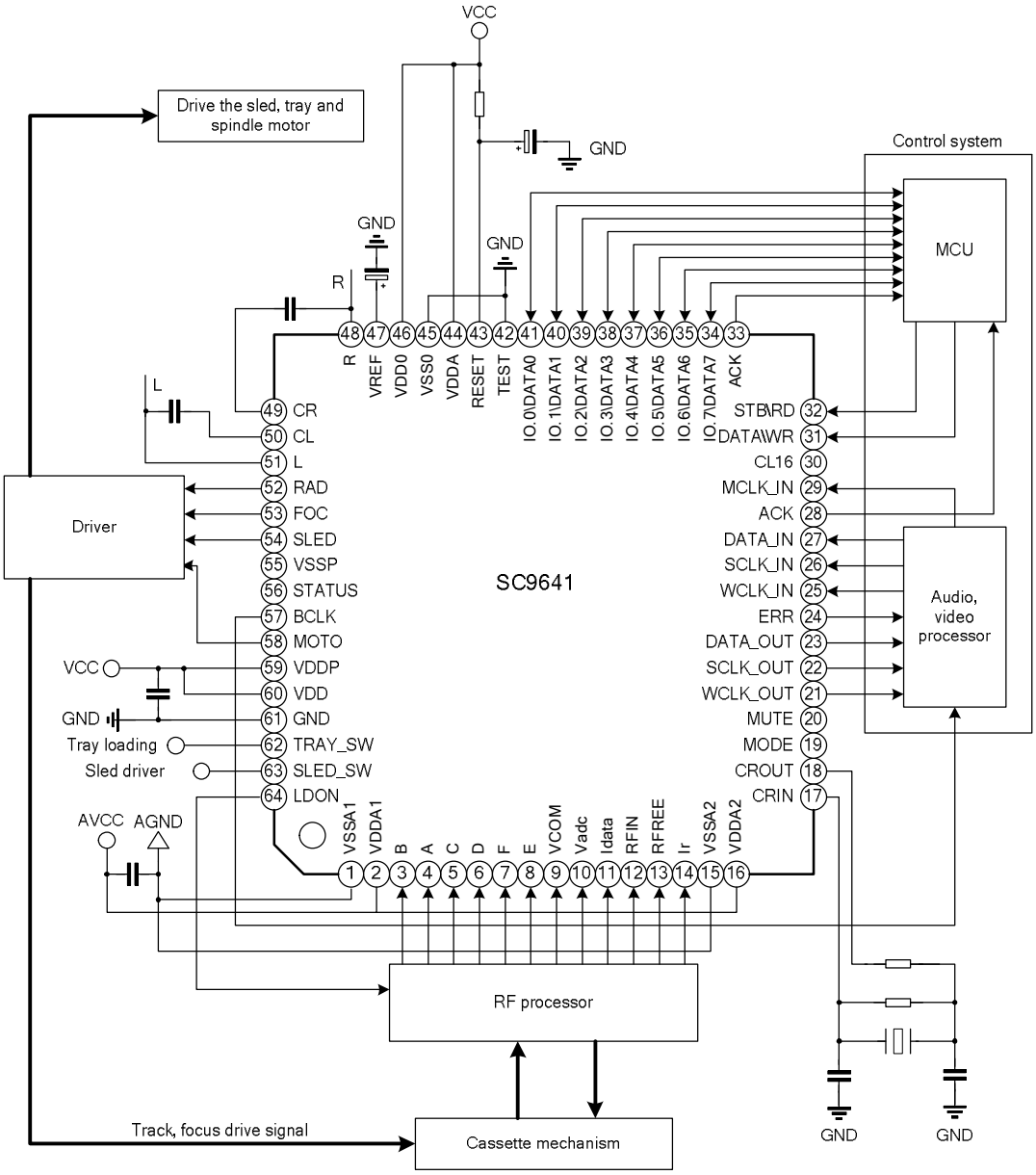
T3-T2: =5us (TYP.), related with the execute speed of master controller.

T4-T3: >=4us

4) Processor of communication error.

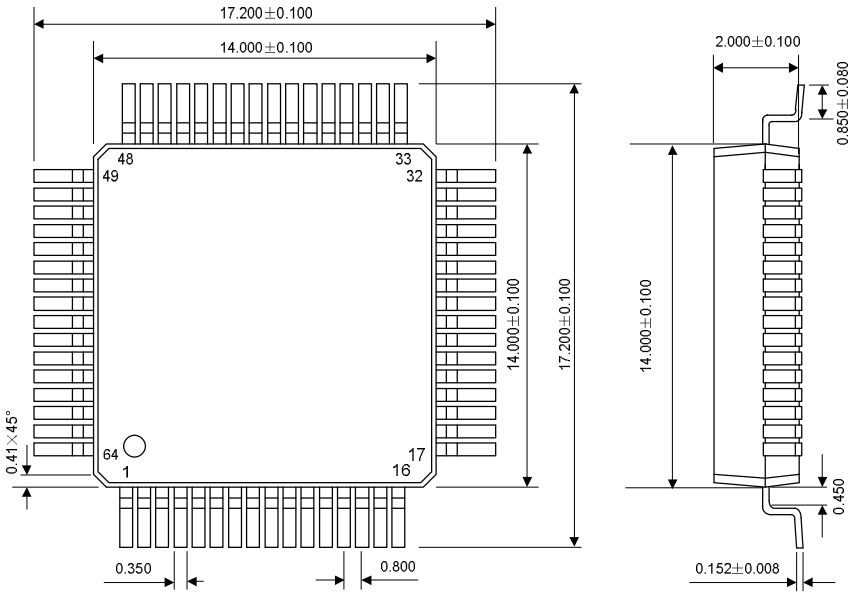
In order to keep the communication normally, SC9641 design the error process in the program communicate protocol. During the communication, the max time of SC9641 wait system command (WR, RD) is 130us, if the wait time is more than 130us, SC9641 regard this communication error, and end this operation, wait the next communication.

TYPICAL APPLICATIONS CIRCUIT



PACKAGE OUTLINE

QFP-64-14x14-0.8 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note: Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.