

EPF8101S

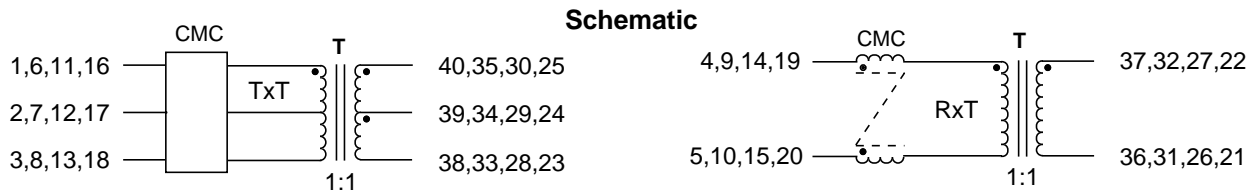


- For National Semiconductor Chips •
- 40 Pin SOIC Package •
- Guaranteed to operate with 8 mA DC bias at 70°C •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

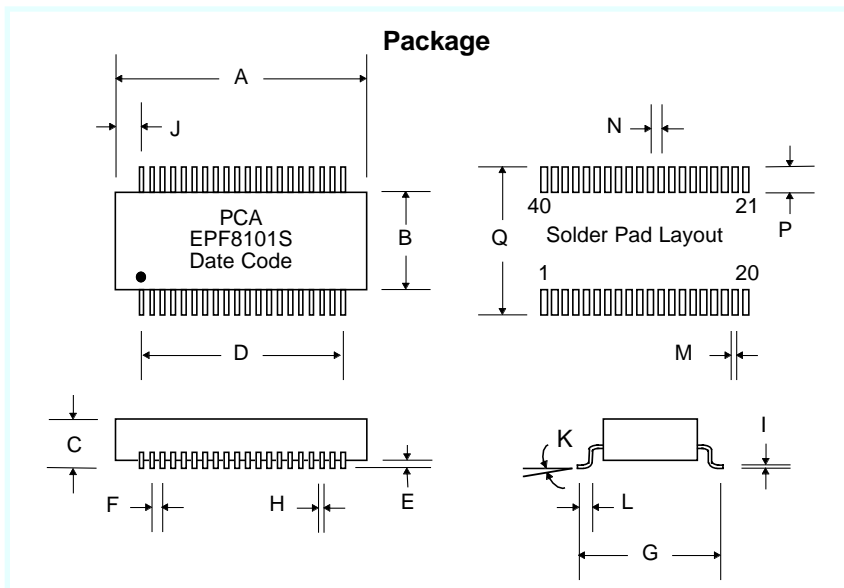
Electrical Parameters @ 25° C

OCL @ 70°C	Insertion Loss (dB Max.)		Return Loss (dB Min.)						Common Mode Rejection (dB Min.)		Crosstalk (dB Min.)
	1-100 MHz		1-30 MHz	30-60 MHz	60-80 MHz				1-80 MHz	80-100 MHz	
100 KHz, 0.1 Vrms 8 mA DC Bias											
Media Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Xmit	
350µH	-1	-1	-18	-18	-12	-12	-10	-10	-35	-30	-38

- Isolation : 1500 Vrms • Impedance : 100 ohms • Rise Time : 3.0 nS Max. •



Version G



Dimensions

Dim.	(Inches)			(Millimeters)		
	Min.	Max.	Nom.	Min.	Max.	Nom.
A	1.110	1.130		28.19	28.70	
B	.470	.490		11.94	12.45	
C	.235	.255		6.10	6.35	
D	.950	Typ.		24.13	Typ.	
E	.010	.015		.254	.381	
F	.050	Typ.		1.27	Typ.	
G	.590	.610		14.99	15.49	
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.085	Typ.		2.16	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.030			.762
N			.050			1.27
P			.090			2.29
Q			.670			17.02