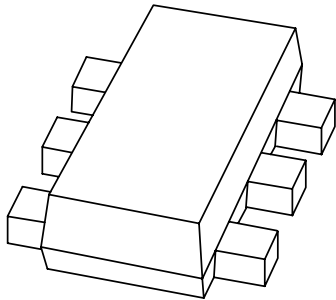


DATA SHEET



PBSS4140V 40 V low V_{CEsat} NPN transistor

Product data sheet
Supersedes data of 2001 Nov 05

2002 Jun 20

40 V low V_{CEsat} NPN transistor

PBSS4140V

FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm x 1.2 mm x 0.55 mm ultra thin package
- Improved thermal behaviour due to flat leads
- Excellent coplanarity due to straight leads
- Low collector-emitter saturation voltage
- High current capabilities
- Reduced required PCB area.

APPLICATIONS

- General purpose switching and muting
- LCD backlighting
- Supply line switching circuits
- Battery driven equipment (mobile phones, video cameras and hand-held devices).

DESCRIPTION

NPN low V_{CEsat} transistor with high current capability in a SOT666 plastic package. PNP complement: PBSS5140V.

MARKING

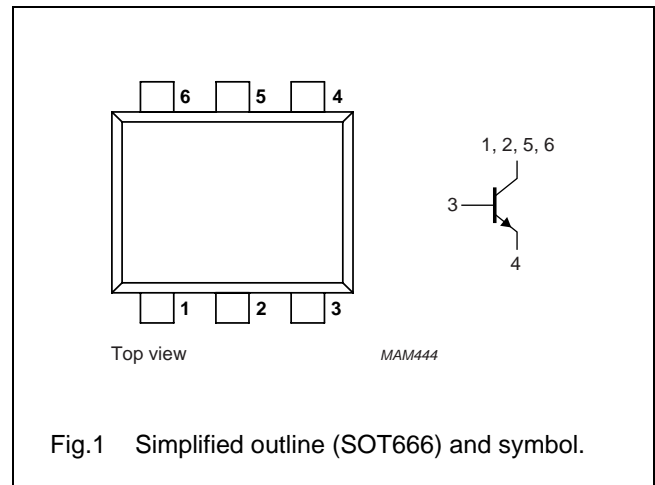
TYPE NUMBER	MARKING CODE
PBSS4140V	22

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	40	V
I_C	collector current (DC)	1	A
I_{CRP}	peak collector current	2	A
R_{CEsat}	equivalent on-resistance	<190	m Ω

PINNING

PIN	DESCRIPTION
1	collector
2	collector
3	base
4	emitter
5	collector
6	collector



40 V low V_{CEsat} NPN transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	1	A
I_{CM}	peak collector current		–	3	A
I_{CRP}	repetitive peak collector current	note 1	–	2	A
I_B	base current (DC)		–	300	mA
I_{BM}	peak base current		–	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 2	–	300	mW
		$T_{amb} \leq 25\text{ °C}$; note 3	–	500	mW
		$T_{amb} \leq 25\text{ °C}$; notes 1 and 2	–	1.2	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions: $t_p \leq 30\text{ ms}$; $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
3. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm^2 .

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	410	K/W
		note 2	215	K/W
		notes 1 and 3	110	K/W

Notes

1. Device mounted on a printed circuit board; single sided copper; tinplated; standard footprint.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm^2 .
3. Operated under pulsed conditions: $t_p \leq 30\text{ ms}$; $\delta \leq 0.2$.

Soldering

The only recommended soldering method is reflow soldering.

40 V low V_{CEsat} NPN transistor

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CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

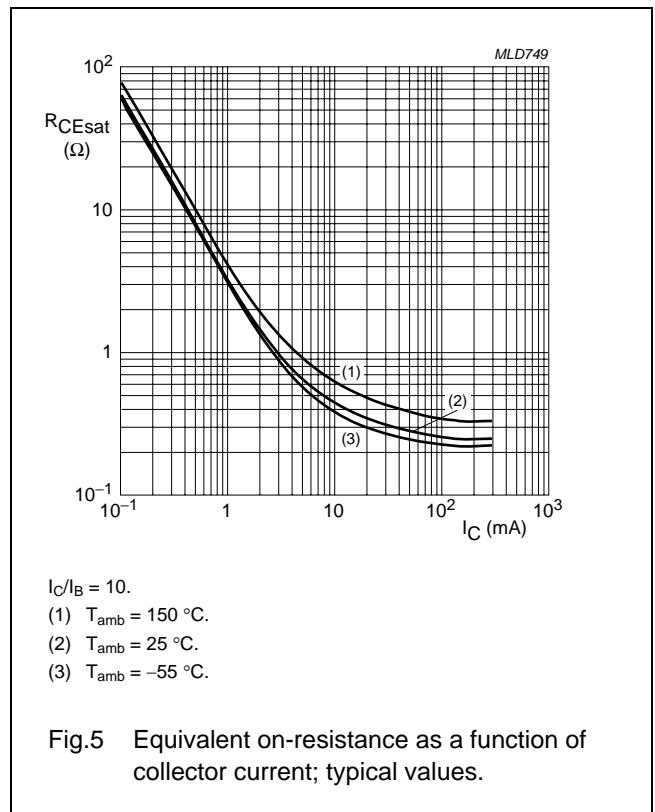
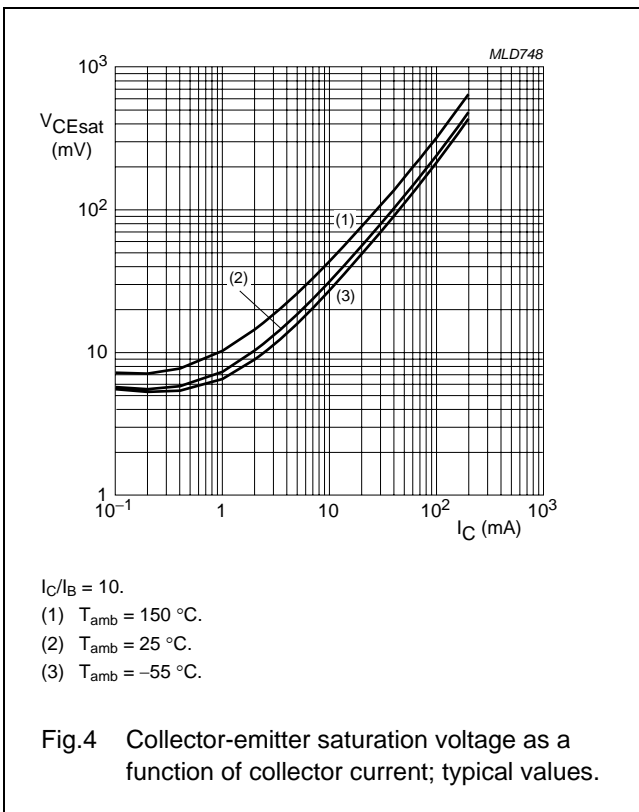
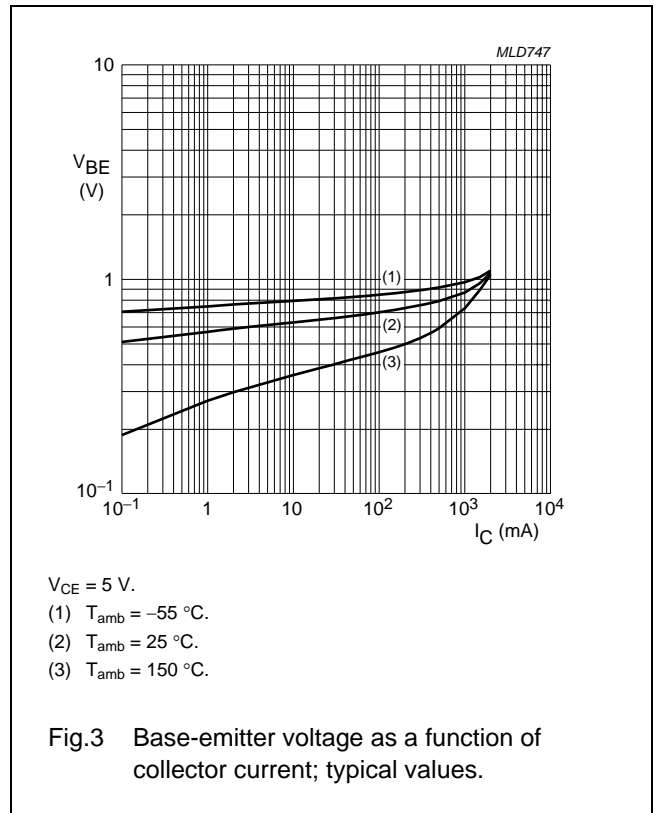
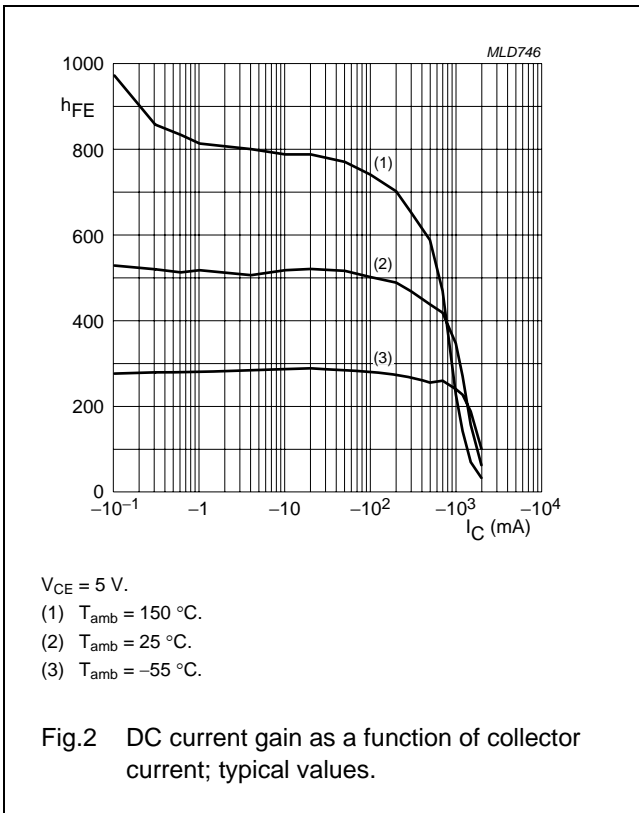
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = 40\text{ V}; I_E = 0$	–	–	100	nA
		$V_{CB} = 40\text{ V}; I_E = 0; T_{amb} = 150\text{ °C}$	–	–	50	μA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0$	–	–	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	300	–	–	
		$V_{CE} = 5\text{ V}; I_C = 500\text{ mA}$	300	–	900	
		$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	200	–	–	
		$V_{CE} = 5\text{ V}; I_C = 2\text{ A}; \text{note 1}$	75	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 100\text{ mA}; I_B = 1\text{ mA}$	–	50	80	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	70	110	mV
		$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	–	150	190	mV
		$I_C = 2\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	320	440	mV
R_{CEsat}	equivalent on-resistance	$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	–	150	<190	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	–	1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	–	–	1.1	V
f_T	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$	150	–	–	MHz
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	10	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.

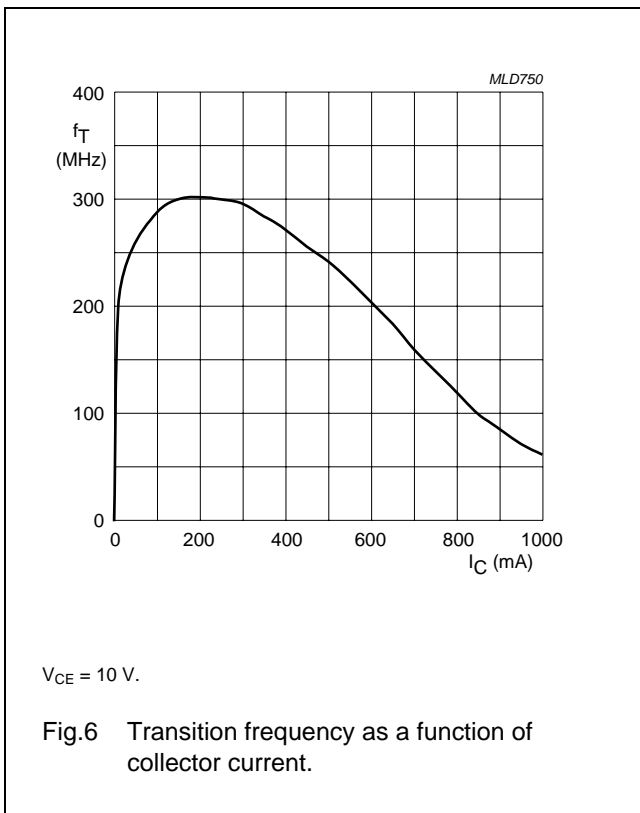
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PBSS4140V



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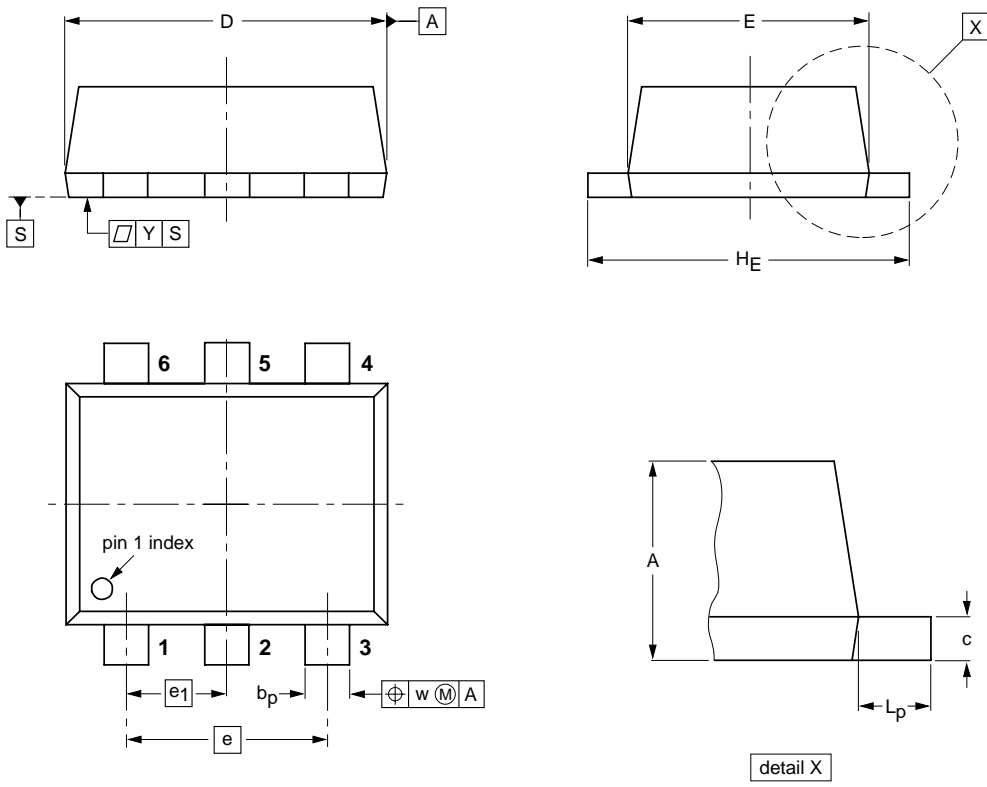
40 V low V_{CEsat} NPN transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

40 V low V_{CEsat} NPN transistor

PBSS4140V

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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For additional information please visit: **<http://www.nxp.com>**

For sales offices addresses send e-mail to: **salesaddresses@nxp.com**

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