512Mb (8M×4Bank×16) Double DATA RATE 2 SDRAM

Features

- JEDEC Standard VDD/VDDQ=1.8V ± 0.1V.
- All inputs and outputs are compatible with SSTL_18 interface.
- Fully differential clock inputs (CK,/CK) operation.
- 4 Banks
- Posted CAS
- Burst Length: 4 and 8.
- Programmable CAS Latency (CL): 3, 4 and 5.
- Programmable Additive Latency (AL): 0, 1, 2, 3 and 4.
- Write Latency (WL) =Read Latency (RL) -1.
- Read Latency (RL) = Programmable Additive Latency (AL) + CAS Latency (CL)
- Bi-directional Differential Data Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available.
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination (ODT)
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- Average Refresh Period 7.8us at lower than T_{case} 85°C, 3.9us at 85°C < T_{case} ≦ 95°C
- RoHS Compliance
- Partial Array Self-Refresh (PASR)
- High Temperature Self-Refresh rate enable

Description

The EM44BM1684LBB is a high speed Double Date Rate 2 (DDR2) Synchronous DRAM fabricated with ultra high performance CMOS process containing 536,870,912 bits which organized as 8Mbits x 4 banks by 16 bits.

This synchronous device achieves high speed double-data-rate transfer rates of up to 667 Mb/sec/pin (DDR2-667) for general applications.

The chip is designed to comply with the following key DDR2 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) Off-Chip Driver (OCD) impedance adjustment and On Die Termination (4) normal and weak strength data output driver.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style.

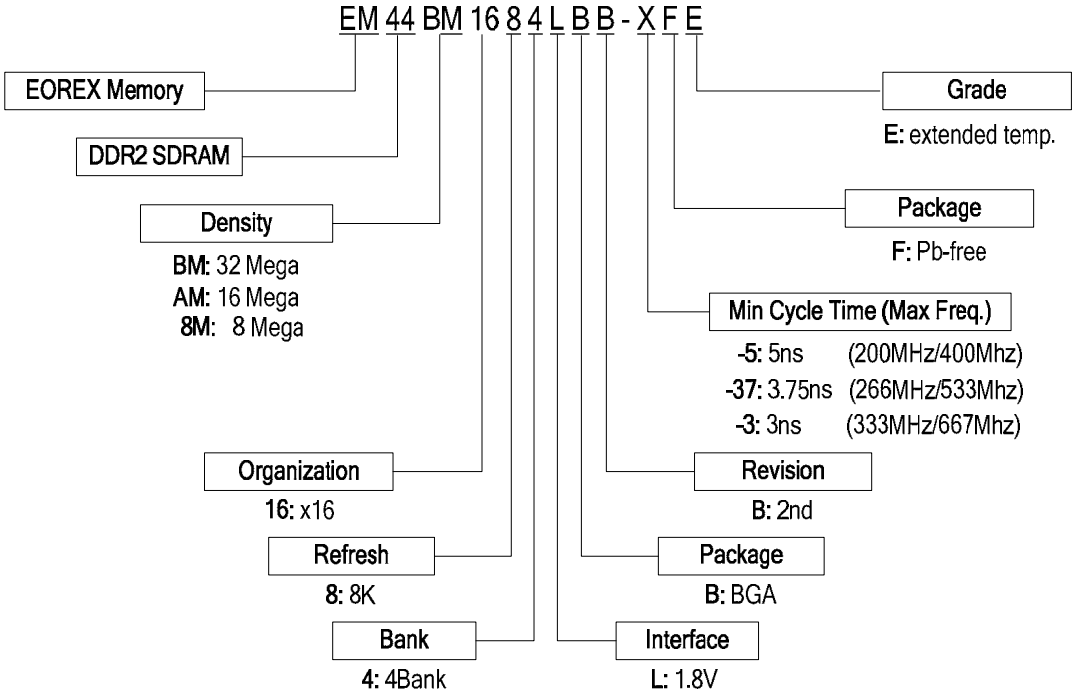
The 512Mb DDR2 device operates with a single power supply: 1.8V ± 0.1V VDD and VDDQ.

Available package: TFBGA-84Ball (13mmx10.5mm, 0.8mm x 0.8mm ball pitch).

Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM44BM1684LBB-3F	32M X 16	t_{CK} 5: DDR2-667Mhz 5-5-5 t_{CK} 4: DDR2-533Mhz 4-4-4 t_{CK} 3: DDR2-400Mhz 3-3-3 **(Note)**	TFBGA-84 Ball	Commercial	Free

Note : Speed (t_{CK*}) is in order of CL-tRCD-tRP



* EOREX reserves the right to change products or specification without notice.

Pin Assignment: Top View

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	/UDQS	VDDQ
DQ14(UDQ6)	VSSQ	UDM	B	UDQS	VSSQ	DQ15(UDQ7)
VDDQ	DQ9(UDQ1)	VDDQ	C	VDDQ	DQ8(UDQ0)	VDDQ
DQ12(UDQ4)	VSSQ	DQ11(UDQ3)	D	DQ10(UDQ2)	VSSQ	DQ13(UDQ5)
VDD	NC	VSS	E	VSSQ	/LDQS	VDDQ
DQ6(LDQ6)	VSSQ	LDM	F	LDQS	VSSQ	DQ7(LDQ7)
VDDQ	DQ1(LDQ1)	VDDQ	G	VDDQ	DQ0(LDQ0)	VDDQ
DQ4(LDQ4)	VSSQ	DQ3(LDQ3)	H	DQ2(LDQ2)	VSSQ	DQ5(LDQ5)
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	/WE	K	/RAS	/CK	ODT
NC	BA0	BA1	L	/CAS	/CS	
	A10/AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

84ball TFBGA / (13.0mm x 10.5mm x 1.2mm)

Note:

1. VDDL and VSSDL are power and ground for the DLL.

2. In case of only 8 DQs out of 16 DQs are used, LDQS, LDQSB and DQ0~7 must be used.

Pin Description (Simplified)

Pin	Name	Function
J8,K8	CK,/CK	**(System Clock)** CK and CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and CK (both directions of crossing).
L8	/CS	**(Chip Select)** All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
K2	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self- Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE are disabled during Self-Refresh.
M8,M3,M7,N2,N8, N3,N7,P2,P8,P3, M2,P7,R2	A0~12	**(Address)** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged. A0~A12:Row address ; A0~9 :Column address. The address inputs also provide the op-code during Mode Register Set commands.
L2,L3	BA0, BA1	**(Bank Address)** BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied (For 256Mb and 512Mb, BA2 is not applied). Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
K9	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.
K7, L7, K3	/RAS, /CAS, /WE	**(Command Inputs)** /RAS, /CAS and /WE (along with /CS) define the command being entered.
B7,A8,F7,E8	UDQS,/UDQS, LDQS,/LDQS	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobes LDQS and UDQS may be used in single ended mode or paired with optional complementary signals /LDQS and /UDQS

		to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to A10 = 0 of EMRS(1) using LDQS/LDQS and UDQS/UDQS. "single-ended DQS signals" refers to A10 = 1 of EMRS(1) using LDQS and UDQS.
B3,F3	UDM,LDM	**(Input Data Mask)** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
G8,G2,H7,H3,H1, H9,F1,F9,C8, C2,D7,D3,D1, D9,B1,B9	DQ0~15	**(Data Input/Output)** Data inputs and outputs are on the same pin.
A1,E1,J9,M9,R1/ A3,E3,J3,N1,P9	VDD/VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
A9,C1,C3,C7,C9,E 9,G1,G3,G7,G9/ A7,B2,B8,D2,D8,E 7,F2,F8,H2,H8	VDDQ/VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
J1/J7	VDDL/VSSDL	**(DLL Power Supply/DLL Ground)** VDDL and VSSDL are power supply for DLL circuits
J2	VREF	**(Reference Voltage)** SSTL_1.8 reference voltage
A2,E2,L1,R3,R7, R8	NC	**(No Connection)** No internal electrical connection is present.

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ +2.3	V
V_{DD}, $V_{DDQ,}$	Power Supply Voltage	-0.5 ~ +2.3	V
$V_{DDL,}$	DLL Power Supply Voltage	-0.5 ~ +2.3	V
T_{OP}	Operating Temperature Range	0 ~ +85	°C
T_{STG}	Storage Temperature Range	-55 ~ +100	°C
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Current	50	mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (V_{CC}=1.8V ±0.1V, f=1MHz, T_A=25°C)

Symbol	Parameter	DDR2-400/533		DDR2-667		Units
		Min.	Max.	Min.	Max.	
C_{CK}	Input Capacitance of CK, /CK	1.0	2.0	1.0	2.0	pF
CD_{CK}	Input Capacitance delta of CK, /CK	-	0.25	-	0.25	pF
C_I	Input Capacitance for others: CKE, Address, /CS, /RAS, /CAS, /WE	1.0	2.0	1.0	2.0	pF
CD_I	Input Capacitance delta for others	-	0.25	-	0.25	pF
C_{IO}	Input/Output Capacitance DQ, DM, DQS, DQS, RDQS, RDQS	2.5	4	2.5	3.5	pF
C_{DIO}	Input/Output Capacitance delta	-	0.5	-	0.5	pF

Recommended DC Operating Conditions (T_A=0°C ~85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.7	1.8	1.9	V
V_{DDDL}	Power Supply for DLL Voltage	1.7	1.8	1.9	V
V_{DDQ}	Power Supply for Output Voltage	1.7	1.8	1.9	V
V_{REF}	Input Reference Voltage	0.49* V_{DDQ}	0.5* V_{DDQ}	0.51* V_{DDQ}	V
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF}	V_{REF} +0.04	V
V_{ID}	DC differential Input Voltage	0.25	-	V_{DDQ}+0.6	V
V_{IH}	Input Logic High Voltage	V_{REF} +0.125	-	V_{DDQ}+0.3	V
V_{IL}	Input Logic Low Voltage	-0.3	-	V_{REF} - 0.125	V

Note: * All voltages referred to V_{SS}.

Recommended DC Operating Conditions

(V_{DD}=1.8V±0.1V, T_A=0°C ~ 85°C)

Symbol	Parameter	Test Conditions	-5 3-3-3	-37 4-4-4	-3 5-5-5	Units
			Max.	Max.	Max.	
I_{DD1}	Operating Current ***(Note 1)***	Burst length=2, $t_{RC} \geq t_{RC}$(min.), I_{OL}=0mA, One bank active	110	110	120	mA
I_{DD2P}	Precharge Standby Current in Power Down Mode	CKE≤V_{IL}(max.), t_{CK}=min	8	8	8	mA
I_{DD2N}	Precharge Standby Current in Non-power Down Mode	CKE≥V_{IH}(min.), t_{CK}=min, /CS≥V_{IH}(min.) Input signals SWITCHING	35	40	40	mA
I_{DD3P}	Active Standby Current in Power Down Mode ***(A12=0)***	CKE≤V_{IL}(max.), t_{CK}=min	30	30	30	mA
I_{DD3P}	Active Standby Current in Power Down Mode ***(A12=1)***	CKE≤V_{IL}(max.), t_{CK}=min	12	12	12	mA
I_{DD3N}	Active Standby Current in Non-power Down Mode	CKE≥V_{IH}(min.), t_{CK}=min, /CS≥V_{IH}(min.) Input signals SWITCHING	45	50	50	mA
I_{DD4}	Operating Current (Burst Mode) ***(Note 2)***	$t_{CK} \geq t_{CK}$(min.), I_{OL}=0mA, All banks active	140	180	200	mA
I_{DD5}	Refresh Current (Burst Mode) ***(Note 3)***	$t_{RC} \geq t_{RFC}$ (min.), All banks active	150	150	160	mA
I_{DD6}	Self Refresh Current	CKE≤0.2V	8	8	8	mA
I_{DD7}	Operating Current	All bank Interleave read	320	320	320	mA

*All voltages referenced to V_{SS}.

Note 1: I_{DD1} depends on output loading and cycle rates. (CL=CL min. AL=0)

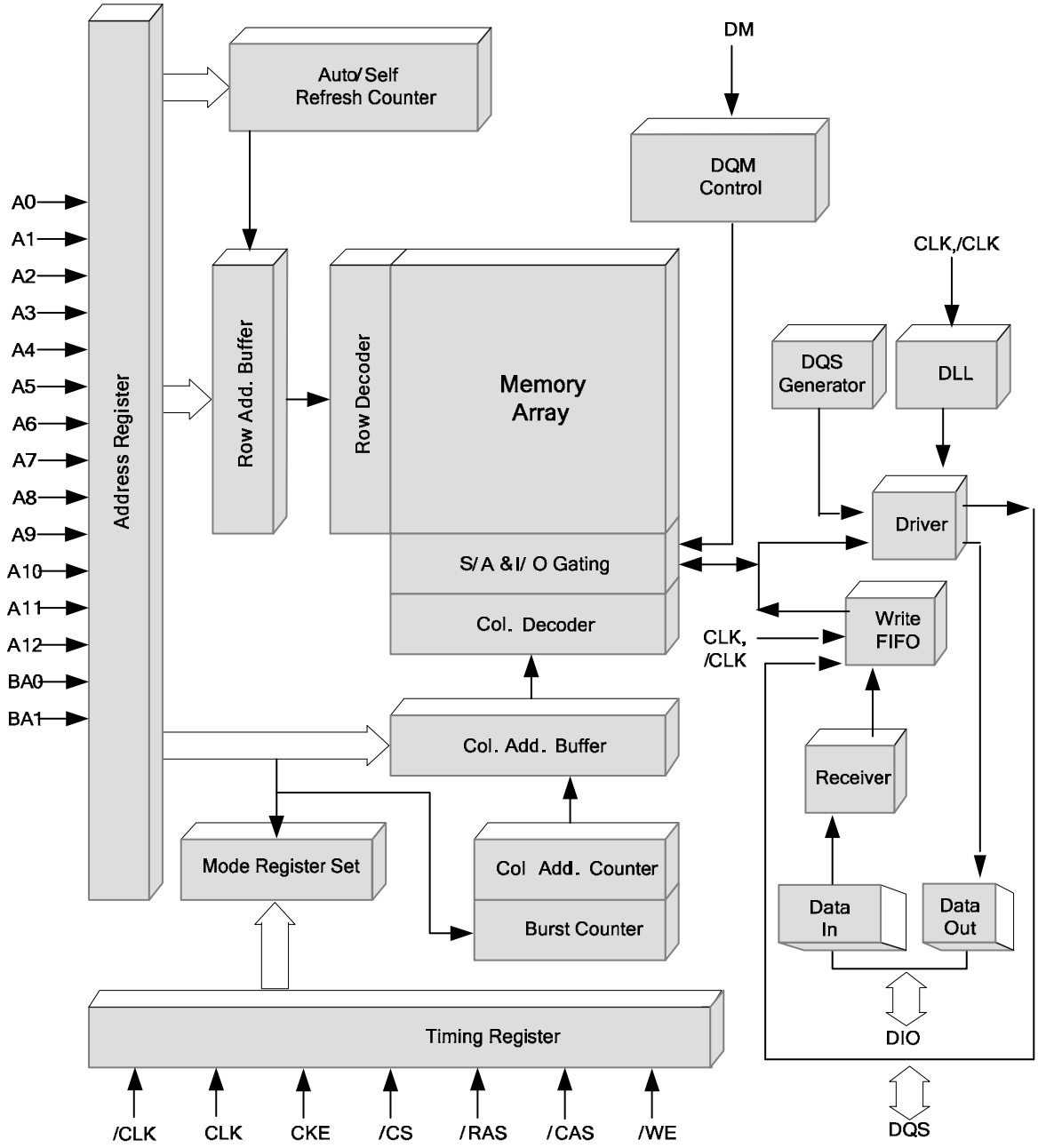
Note 2: I_{DD4} depends on output loading and cycle rates.
Input signals SWITCHING.

Note 3: Min. of t_{RFC} (Auto refresh Row Cycle Times) is shown at AC Characteristics.

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{IL}	Input Leakage Current	0≤V_I≤V_{DDQ}, V_{DDQ}=V_{DD} All other pins not under test=0V	-2	+2	uA
I_{OL}	Output Leakage Current	0≤V_O≤V_{DDQ}, D_{OUT} is disabled	-5	+5	uA
V_{OH}	High Level Output Voltage	I_O=-13.4mA	V_{TT}+0.603		V
V_{OL}	Low Level Output Voltage	I_O=+13.4mA		V_{TT}-0.603	V

Block Diagram



OCD Default Setting Table

Symbol	Parameter	Min.	Typ.	Max.	Units
-	Output Impedance	12.6	18	23.4	Ω
-	Pull-up / Pull down mismatch	0	-	4	Ω
-	Output Impedance step size for OCD calibration	0	-	1.5	Ω
-	Output Slew Rate	+1.5	-	5.0	V/ns

AC Operating Test Conditions

(V_{DD}=1.8V ± 0.1V, T_A=0°C ~85°C)

Symbol	Item	Conditions
VSWING(max)	Input Signal maximum peak to peak swing	1.0 V
SLEW	Input Signals minimum slew rate	1.0 V/ns
V_{REF}	Input Reference Level	0.5*V_{DDQ}

AC Operating Test Conditions(Continued)

Symbol	Parameter	Min.	Max.	Units
V_{ID}	AC differential Input Voltage	0.5	V_{DDQ}+0.6	V
V_{IX}	AC differential corss point Input Voltage	0.5*V_{DDQ} - 0.175	0.5*V_{DDQ} + 0.175	V
V_{OX}	AC differential corss point Output Voltage	0.5*V_{DDQ} - 0.125	0.5*V_{DDQ} + 0.125	V
V_{OH}	High Level Output Voltage	V_{TT}+0.603	-	V
V_{OL}	Low Level Output Voltage	-	V_{TT}-0.603	V

Symbol	Parameter	DDR2-400/533		DDR2-667		Units
		Min.	Max.	Min.	Max.	
V_{IH}	Input Logic High Voltage	V_{REF} + 0.25	-	V_{REF} + 0.2	-	V
V_{IL}	Input Logic Low Voltage	-	V_{REF} - 0.25	-	V_{REF} - 0.2	V

AC Operating Test Characteristics

(V_{DD}=1.8V±0.1V, T_A=0°C ~85°C)

Symbol	Parameter		-3		Units
			Min.	Max.	
t_{DQCK}	DQ output access from CLK,/CLK		-0.45	+0.45	ns
t_{DQSCK}	DQS output access time from CLK,/CLK		-0.4	+0.4	ns
t_{CL},t_{CH}	CL low/high level width		0.45	0.55	t_{CK}
t_{CK}	Clock Cycle Time	CAS Latency =5	3	8	ns
		CAS Latency =4	3.75	8	ns
		CAS Latency =3	5	8	ns
t_{DS}	DQ and DM setup time		0.1	-	ns
t_{DH}	DQ and DM hold time		0.18	-	ns
t_{DIPW}	DQ and DM input pulse width for each input		0.35	-	t_{CK}
t_{HZ}	Data out high impedance time from CLK,/CLK		-0.45	+0.45	ns
t_{LZ}	Data out low impedance time from CLK,/CLK		-0.45	+0.45	ns
t_{DQSQ}	DQS-DQ skew for associated DQ signal		-	0.24	ns
t_{QSH}	Data hold skew factor		-	0.34	ns
t_{DQSS}	Write command to first latching DQS transition		WL -0.25	WL +0.25	t_{CK}
t_{DQSL},t_{DQSH}	DQS Low/High input pulse width		0.35	-	t_{CK}
t_{DSL},t_{DSH}	DQS input valid window		0.2	-	t_{CK}
t_{MRD}	Mode Register Set command cycle time		2	-	t_{CK}
t_{WPRES}	Write Preamble setup time		0	-	ns
t_{WPRE}	Write Preamble		0.35	-	t_{CK}
t_{WPST}	Write Postamble		0.4	0.6	t_{CK}
t_{IS}	Address/control input setup time		0.2	-	ns
t_{IH}	Address/control input hold time		0.28	-	ns
t_{RPRE}	Read Preamble		0.9	1.1	t_{CK}

AC Operating Test Characteristics (Continued)

(V_{DD}=1.8V±0.1V, T_A=0°C ~85°C)

Symbol	Parameter	-3		Unit
		Min.	Max.	
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}
t_{RAS}	Active to Precharge command period	45	70K	ns
t_{RC}	Active to Active command period	60	-	ns
t_{RFC}	Auto Refresh Row Cycle Time	105	-	ns
t_{RCD}	Active to Read or Write delay	15	-	ns
t_{RP}	Precharge command period	15	-	ns
t_{RRD}	Active bank A to B command period	10	-	ns
t_{CCD}	Column address to column address delay	2	-	t_{CK}
t_{WR}	Write recovery time	15	-	ns
t_{DAL}	Auto Pre-charge write recovery + pre-charge time	t_{RP}+ t_{WR}	-	t_{CK}
t_{XSRD}	Exit self refresh to Read command	200	-	t_{CK}
t_{XSNR}	Exit self refresh to non-read command	115	-	ns
t_{XARD}	Exit active power-down mode to Read command (Fast exit)	2	-	t_{CK}
t_{XARDS}	Exit active power-down mode to Read command (Slow exit)	6-AL	-	t_{CK}
t_{XP}	Exit pre-charge power-down to any non-read command	2	-	t_{CK}
t_{WTR}	Internal Write to Read command delay	7.5	-	ns
t_{RTP}	Internal Read to pre-charge delay	7.5	-	ns
t_{CKE}	CKE minimum pulse width	3	-	t_{CK}
t_{WPD}	Write to pre-charge delay(same bank)	WL+ BL/2 + t_{WR}	-	t_{CK}
t_{RPD}	Read to pre-charge delay(same bank)	AL+ BL/2+1	-	t_{CK}
t_{OIT}	OCD drive mode output delay	0	12	ns
t_{REFI}	Average periodic refresh interval	-	7.8	us

AC Operating Test Characteristics (Continued)

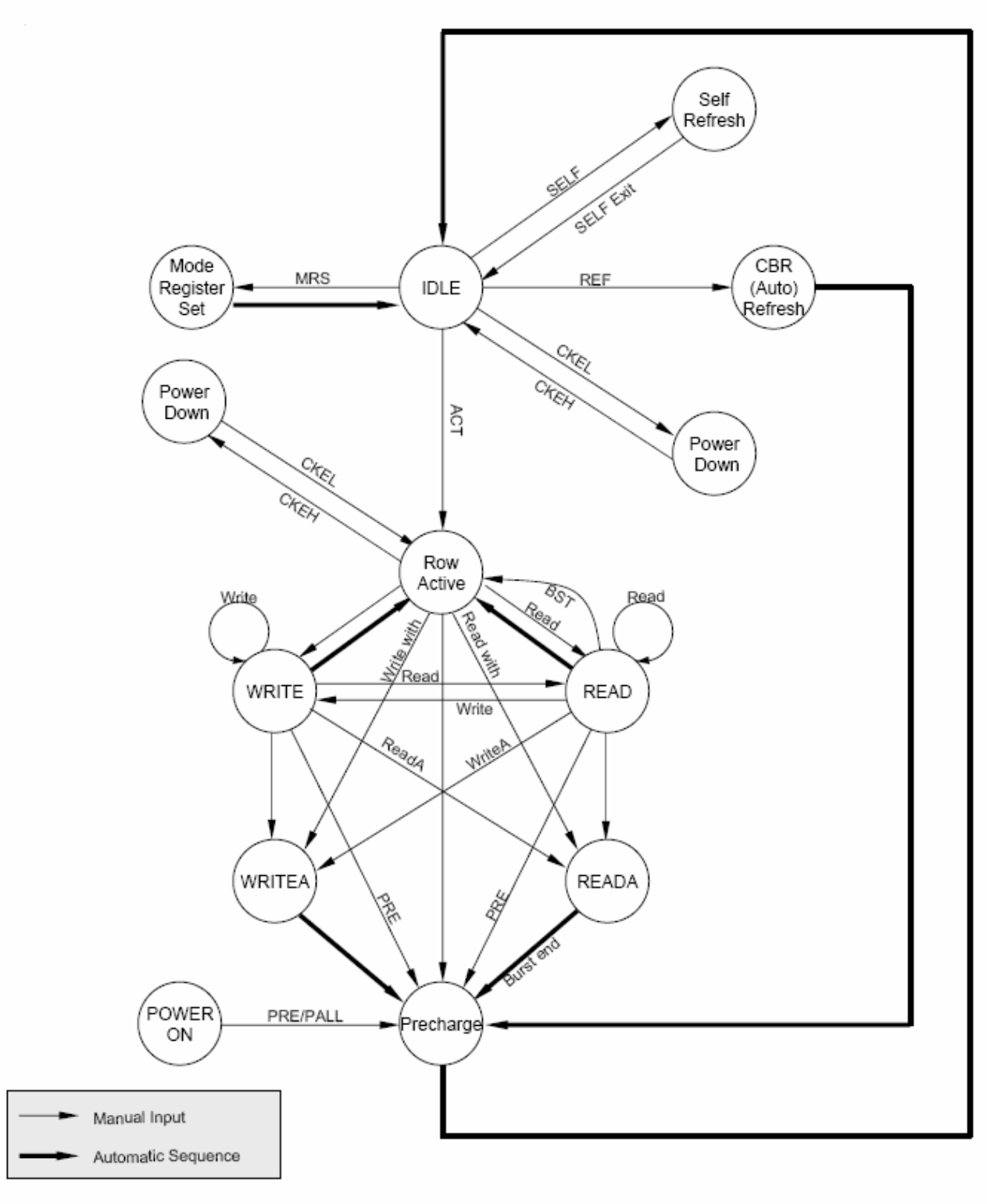
(V_{DD}=1.8V±0.1V, T_A=0°C ~85°C)

Symbol	Parameter	-3		Unit
		Min.	Max.	
t_{AOND}	ODT turn-on delay	2		t_{CK}
t_{AOFD}	ODT turn-off delay	2.5		t_{CK}
t_{AON}	ODT turn-on ***(Note 1)***	tAC (MIN)	tAC (MAX) + 1	ns
t_{AOF}	ODT turn-off ***(Note 2)***	tAC (MIN)	tAC (MAX) + 0.6	ns
t_{AONPD}	ODT turn-on (Power-Down Modes)	tAC (MIN) + 2ns	2Tck+ tAC (MAX) + 1ns	ns
t_{AOFPD}	ODT turn-off (Power-Down Modes)	tAC (MIN) + 2ns	2.5Tck + tAC (MAX) + 1ns	ns
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	-	t_{CK}
t_{AXPD}	ODT Power Down Exit Latency	8	-	t_{CK}

Note 1: ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measure from tAOND.

Note 2: ODT turn off time min is when the device starts to turn off ODT resistance
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

Simplified State Diagram



1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A12~A0
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Read	READ	H	H	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	H	L	H	L	H	V	H	V
Write	WRIT	H	H	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	H	L	H	L	L	V	H	V
Bank Activate	ACT	H	H	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	H	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	H	L	L	H	L	X	H	X
(Ext.) Mode Register Set	(E)MRS	H	H	L	L	L	L	V	V	V

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	H	X	X	X	X
			H	L	L	H	H	H	X
Power Down	Power Down Exit		L	H	H	X	X	X	X
			L	H	L	H	H	H	X

Remark H = High level, L = Low level, X = High or Low level (Don't care)

3. Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT/BW	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	Bank active,Latch RA
	L	L	H	L	BA, A10	PRE/PREA	NOP*(Note 3)*
	L	L	L	H	X	REFA	Auto refresh*(Note 4)*
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode register
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA/CA/A10	READ/READA	Begin read,Latch CA, Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write,Latch CA, Determine auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	Precharge/Precharge all
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	Terminal burst
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst,Latch CA, Begin new read, Determine Auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst, PrecharE
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst with DM=”H”,Latch CA,Begin read,Determine auto-precharge *(Note 2)*
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst,Latch CA,Begin new write, Determine auto-precharge *(Note 2)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst with DM=”H”, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	BA/CA/A10	TERM	ILLEGAL
	L	H	L	X	BA/RA	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/A10	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	X	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP}) *(Note 3)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	NOP(Row active after t_{RCD})
	L	H	H	H	X	NOP	NOP(Row active after t_{RCD})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA/CA/A10	READ	ILLEGAL *(Note 1)*
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 1: ILLEGAL to bank in specified states;
Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 2: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 3: NOP to bank precharging or in idle state.May precharge bank indicated by BA.

Note 4: ILLEGAL of any bank is not idle.

4. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Self-Refresh
	L	H	L	H	H	H	X	Exist Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain self refresh)
Both bank precharge power down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Power down
	L	H	L	H	H	H	X	Exist Power down
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power down)
All Banks Idle	H	H	X	X	X	X	X	Refer to function true table
	H	L	H	X	X	X	X	Enter power down mode *(Note 3)*
	H	L	L	H	H	H	X	Enter power down mode *(Note 3)*
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row active/Bank active
	H	L	L	L	L	H	X	Enter self-refresh *(Note 3)*
	H	L	L	L	L	L	Op-Code	Mode register access
	H	L	L	L	L	L	Op-Code	Special mode register access
	L	X	X	X	X	X	X	Refer to current state
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to command truth table

Remark: H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1: After CKE's low to high transition to exist self refresh mode.And a time of t_{RC}(min) has to be Elapse after CKE's low to high transition to issue a new command.

Notes 2:CKE low to high transition is asynchronous as if restarts internal clock.

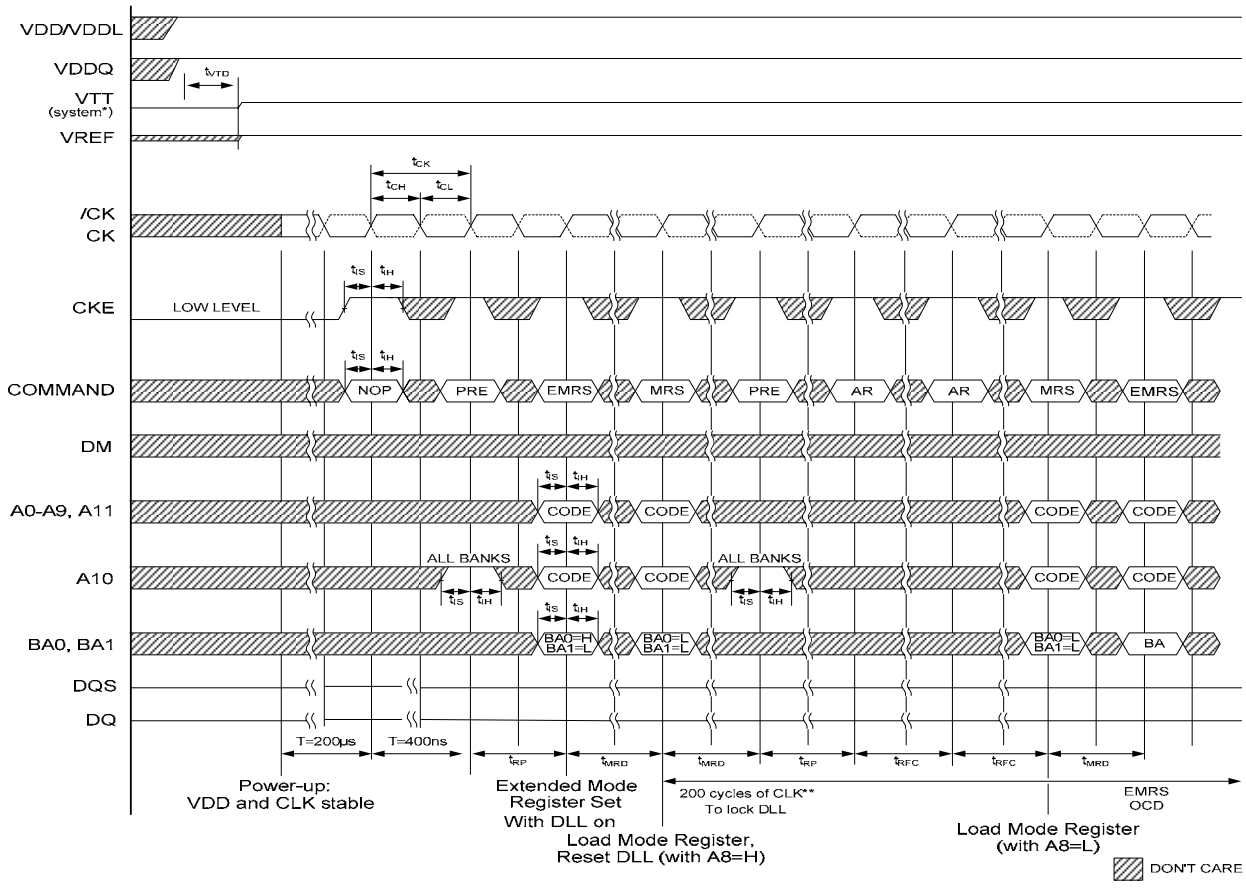
Notes 3:Power down and self refresh can be entered only from the idle state of all banks.

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power and attempt to maintain CKE below 0.2 * VDDQ and ODT at a low state (all other inputs may be undefined). To guarantee ODT off, VREF must be valid and a low level must be applied to the ODTpin.
   - VDD,VDDL and VDDQ are driven from a single power converter output, AND
     VTT is limited to 0.95 V max, AND VREF tracks VDDQ/2 or
   - Apply VDD before or at the same time as VDDL; Apply VDDL before or at the same time as VDDQ; Apply VDDQ before or at the same time as VTT & VREF.

   at least one of these two sets of conditions must be met.
2. Start clock (CK, /CK) and maintain stable power and clock condition for a minimum of 200 µs.
3. Apply NOP or Deselect commands & take CKE high.
4. Wait minimum of 400ns, then issue a Precharge-all command.
5. Issue Reserved command EMRS(2) or EMRS(3).
6. Issue EMRS(1) command to enable DLL. (A0=0 and BA0=1 and BA1=0)
7. Issue MRS command (Mode Register Set) for "DLL reset". (A8=1 and BA0=BA1=0)
8. Issue Precharge-All command.
9. Issue 2 or more Auto-Refresh commands.
10. Issue a MRS command with low on A8 to initialize device operation. (without resetting the DLL)
11. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8=A7=1) followed by EMRS(1) OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other parameters of EMRS(1).
12. The DDR2 SDRAM is now initialized and ready for normal operation.



Mode Register Definition

Mode Register Set

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM which contains addressing mode, burst length, /CAS latency, WR (write recovery), test mode, DLL reset and various vendor's specific opinions. The defaults values of the register is not defined, so the mode register must be written after power up for proper DDR2 SDRAM operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0/1. The state of the address pins A0-A12 in the same cycle as /CS, /RAS, /CAS, /WE and BA0,1 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operating as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, addressing mode uses A3, /CAS latency (read latency from column address) uses A4-A6. A7 is used for test mode. A8 is used for DDR reset. A9 ~ A11 are used for write recovery time (WR) ,A7 must be set to low for normal MRS operation. With address bit A12 two Power-Down modes can be selected, a "standard mode" and a "low-power" Power-Down mode.

Address input for Mode Register Set (MRS)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	PD	WR			DLL	TM	CAS Latency			BT	Burst Length		

DLL Rest	A8
No	0
Yes	1

Mode	A7
Normal	0
Test	1

Burst Length	A2	A1	A0
4	0	1	0
8	0	1	1

Active Power-Down	A12
Fast Exit (Normal)	0
Slow Exit (low power)	1

Burst Type	A3
Sequential	0
Interleave	1

Write Recovery	A11	A10	A9
Reserved	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
Reserved	1	1	0
Reserved	1	1	1

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
Reserved	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
Reserved	1	1	0
Reserved	1	1	1

BA1	BA0	MRS Mode
0	0	Mode Register (MRS)
0	1	Extended Mode Register / EMRS(1)
1	0	EMRS(2) * Reserved
1	1	EMRS(3) * Reserved

Burst Type (A3)

Burst Length	A3	A2	A1	A0	Sequential Addressing	Interleave Addressing
4	X	X	0	0	0 1 2 3	0 1 2 3
	X	X	0	1	1 2 3 0	1 0 3 2
	X	X	1	0	2 3 0 1	2 3 0 1
	X	X	1	1	3 0 1 2	3 2 1 0
8	X	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	X	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	X	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	X	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	X	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	X	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	X	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	X	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0

* Page length is a function of I/O organization and column addressing

Write Recovery

WR (Write Recovery) is for Writes with Auto-Precharge only and defines the time when the device starts pre-charge internally. WR must be programmed to match the minimum requirement for the analogue tWR timing.

Power-Down Mode

Active power-down (PD) mode is defined by bit A12. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit A12 does not apply to precharge power-down mode. When bit A12 = 0, standard Active Power-down mode or 'fast-exit' active power-down mode is enabled. The tXARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode.
When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The tXARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the IDD table.

Address input for Extended Mode Register Set (EMRS(1))

The EMRS (1) is written by asserting low on /CS, /RAS, /CAS, /WE,BA1 and high on BA0 (The DDR2 should be in all bank pre-charge with CKE already prior to writing into the extended mode register.)
The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency,OCD program, ODT, DQS and output buffers disable, RQDS and RDQS enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation.The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the EMRS(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation when all banks are in pre-charge state.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Q off	RDQS	/DQS	OCD Program			Rtt	AL			Rtt	D.I.C	DLL

Q off	A12
Disable	0
Enable	1
Output buffers	

/ DQS	A10
Enable	0
Disable	1

Rtt	A6	A2
Disable	0	0
75Ω	0	1
150Ω	1	0
50Ω	1	1

DLL Rest	A0
Enable	0
Disable	1

RDQS, /RQDS	A11	I/O
Disable	0	
Enable	1	only X8

Output Driver Impedence Control	A1
Normal (100%)	0
Weak (60%)	1

OCD Operation	A9	A8	A7
OCD calibration mode exit	0	0	0
Drive (1)	0	0	1
Drive (0)	0	1	0
Adjust mode *(Note 1)*	1	0	0
OCD Calibration default *(Note 2)*	1	1	1

Additive Latency	A5	A4	A3
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
Reserved	1	1	0
Reserved	1	1	1

BA1	BA0	MRS Mode
0	0	Mode Register (MRS)
0	1	Extended Mode Register / EMRS(1)
1	0	EMRS(2) * Reserved
1	1	EMRS(3) * Reserved

Note 1: When adjust mode is issued, AL from previously set value must be applied.
Note 2: After setting to default, OCD mode needs to be exited by setting A9 ~A7 to 000.
Refer to the chapter Off-Chip Driver (OCD) Impedance Adjustment for detailed information.

Output Drive Strength

The output drive strength is defined by bit A1. Normal drive strength outputs are specified to be SSTL_18.
Programming bit A1 = 0 selects normal (100 %) drive strength for all outputs.
Programming bit A1 = 1 will reduce all outputs to approximately 60 % of the SSTL_18 drive strength.
This option is intended for the support of the lighter load and/or point-to-point environments.

Single-ended and Differential Data Strobe Signals

EMRS		Stobe Function Matrix				signals
A11 (RDQS Enable)	A10 (/DQS Enable)	RDQS DM	/RDQS	DQS	/DQS	
0 (Disable)	0 (Enable)	DM	Hi -Z	DQS	/DQS	differential DQS signals
0 (Disable)	1 (Disable)	DM	Hi -Z	DQS	Hi -Z	single-ended DQS signals
1 (Enable) only for X8	0 (Enable)	RDQS	/RDQS	DQS	/DQS	differential DQS signals (for X8)
1 (Enable) only for X8	1 (Disable)	RDQS	Hi -Z	DQS	Hi -Z	single-ended DQS signals (for X8)

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMRS(1) is set to (0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current.

Address input for Extended Mode Register Set (EMRS(2)) * Reserved

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	SRF	0	0	0	0	PASR		

High Temperature Self-Refresh Rate Enable	A7
Disable	0
Enable** (85C Tcase 95C)	1

Partial Array Self Refresh	A2	A1	A0
Full array	0	0	0
Half Array (BA[1:0]=00&01)	0	0	1
Quarter Array (BA[1:0]=00)	0	1	0
Not defined	0	1	1
3/4 array(BA[1:0]=01,10,&11)	1	0	0
Half array (BA[1:0]=10&11)	1	0	1
Quarter array (BA[1:0]=11)	1	1	0
Not defined	1	1	1

BA1	BA0	MRS Mode
0	0	Mode Register (MRS)
0	1	Extended Mode Register / EMRS(1)
1	0	EMRS(2) * Reserved
1	1	EMRS(3) * Reserved

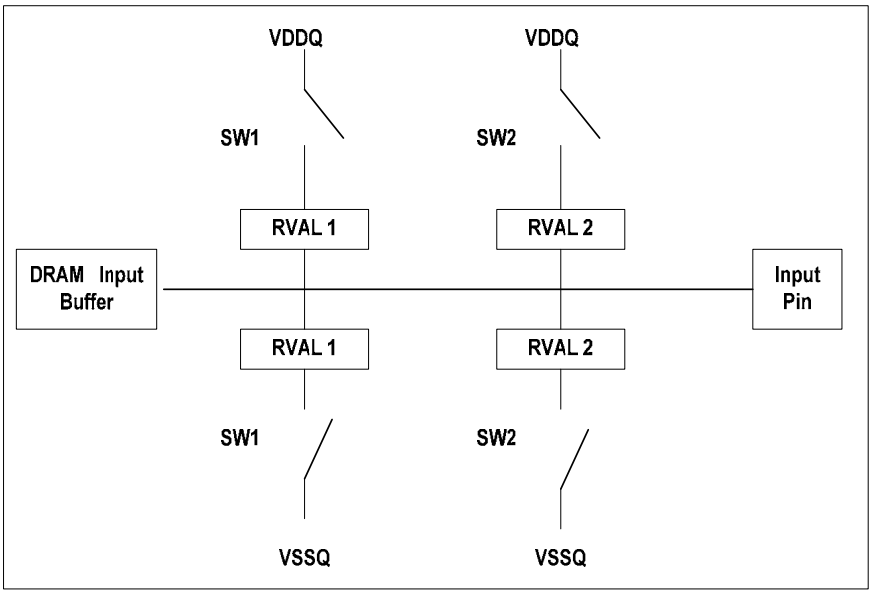
Address input for Extended Mode Register Set (EMRS(3)) * Reserved

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

On-Die Termination (ODT)

ODT (On-Die Termination) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each UDQ, LDQ, UDQS, UDQS, LDQS, LDQS, UDM and LDM signal via the ODT control pin for x16 configuration, where UDQS and LDQS are terminated only when enabled in the EMRS(1) by address bit A10 = 0.
The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.
The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

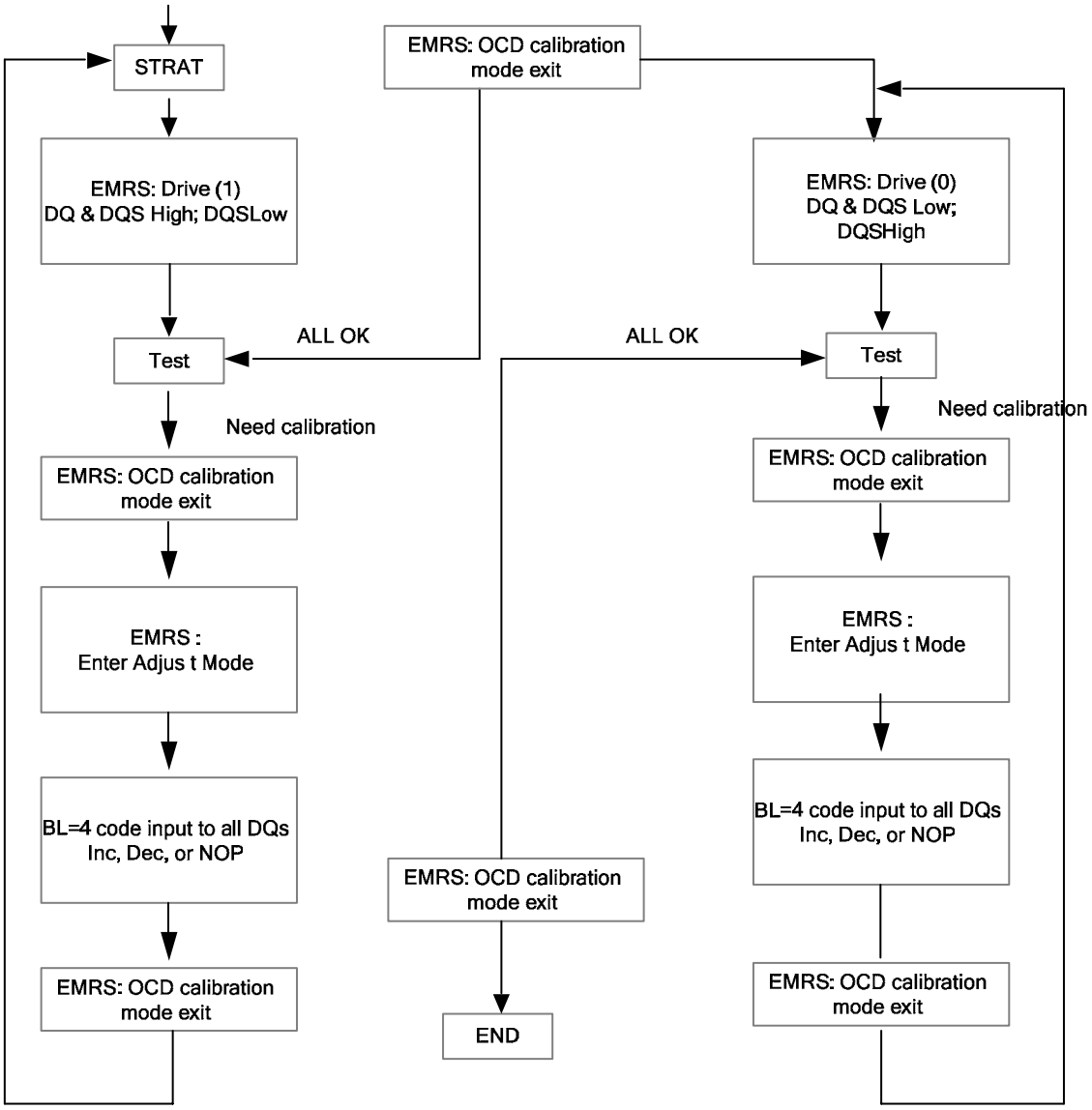
ODT Function



Switch sw1 or sw2 is enabled by the ODT pin. Selection between sw1 or sw2 is determined by “Rtt (nominal)” in EMRS(1) address bits A6 & A2. Target Rtt = 0.5 * Rval1 or 0.5 * Rval2.
The ODT pin will be ignored if the EMRS(1) is programmed to disable ODT.

Off-Chip Driver (OCD) Impedance Adjustment

DR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS(1) command along with a 4 bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 is the table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment can be up to 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the maximum step count range. When Adjust mode command is issued, AL from previously set value must be applied.

Off-Chip-Driver Adjust Program

4 bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (no operation)	NOP (no operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	Reserved

Package Description

(BGA-84 balls Package)