

NTHD3100C

Power MOSFET

20 V, +3.9 A / -4.4 A,
Complementary ChipFET™

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Trench P-Channel for Low On Resistance
- Low Gate Charge N-Channel for Test Switching
- Pb-Free Packages are Available

Applications

- DC-DC Conversion Circuits
- Load Switch Applications Requiring Level Shift
- Drive Small Brushless DC Motors
- Ideal for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V _{DSS}	20	V		
Gate-to-Source Voltage	N-Ch	±12	V		
	P-Ch	±8.0			
N-Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	2.9	A
		T _A = 85°C		2.1	
	t ≤ 10 s	T _A = 25°C		3.9	
P-Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	-3.2	A
		T _A = 85°C		-2.3	
	t ≤ 10 s	T _A = 25°C		-4.4	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.1	W
				t ≤ 5 s	
Pulsed Drain Current (Note 1)	N-Ch	t = 10 μs	I _{DM}	12	A
	P-Ch	t = 10 μs		-13	
Operating Junction and Storage Temperature	T _J , T _{STG}	-55 to 150		°C	
Source Current (Body Diode)	I _S	2.5		A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	T _L	260		°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

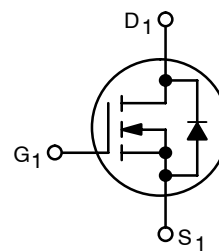
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



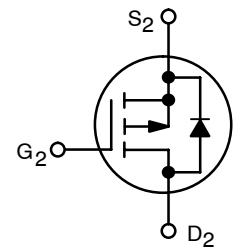
ON Semiconductor®

<http://onsemi.com>

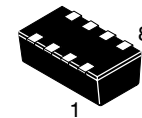
V _{(BR)DSS}	R _{DS(on)} Typ	I _D MAX
N-Channel 20 V	58 mΩ @ 4.5 V	3.9 A
	77 mΩ @ 2.5 V	
P-Channel -20 V	64 mΩ @ -4.5 V	-4.4 A
	85 mΩ @ -2.5 V	



N-Channel MOSFET

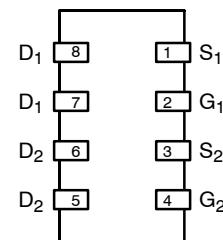


P-Channel MOSFET

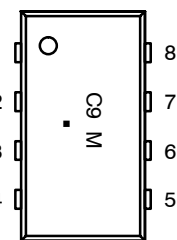


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



- C9 = Specific Device Code
- M = Month Code
- = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NTHD3100C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	113	$^{\circ}C/W$
Junction-to-Ambient – $t \leq 10$ s (Note 2)	$R_{\theta JA}$	60	$^{\circ}C/W$

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 3)							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0$ V	$I_D = 250$ μ A	20		V
		P		$I_D = -250$ μ A	-20		
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 25$ $^{\circ}C$		1.0	μ A
		P	$V_{GS} = 0$ V, $V_{DS} = -16$ V			-1.0	
		N	$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 125$ $^{\circ}C$		5.0	
		P	$V_{GS} = 0$ V, $V_{DS} = -16$ V			-5.0	
Gate-to-Source Leakage Current	I_{GSS}	N	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA
		P	$V_{DS} = 0$ V, $V_{GS} = \pm 8.0$ V			± 100	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250$ μ A	0.6		1.2	V
		P		$I_D = -250$ μ A	-0.45		-1.5	
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5$ V, $I_D = 2.9$ A		58	80	m Ω	
		P	$V_{GS} = -4.5$ V, $I_D = -3.2$ A		64	80		
		N	$V_{GS} = 2.5$ V, $I_D = 2.3$ A		77	115		
		P	$V_{GS} = -2.5$ V, $I_D = -2.2$ A		85	110		
Forward Transconductance	g_{FS}	N	$V_{DS} = 10$ V, $I_D = 2.9$ A		6.0		S	
		P	$V_{DS} = -10$ V, $I_D = -3.2$ A		8.0			

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	N	$f = 1$ MHz, $V_{GS} = 0$ V	$V_{DS} = 10$ V		165	pF	
		P		$V_{DS} = -10$ V		680		
Output Capacitance	C_{OSS}	N		$V_{DS} = 10$ V		80		
		P		$V_{DS} = -10$ V		100		
Reverse Transfer Capacitance	C_{RSS}	N		$V_{DS} = 10$ V		25		
		P		$V_{DS} = -10$ V		70		
Total Gate Charge	$Q_{G(TOT)}$	N		$V_{GS} = 4.5$ V, $V_{DS} = 10$ V, $I_D = 2.9$ A		2.3		nC
		P		$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -3.2$ A		7.4		
Threshold Gate Charge	$Q_{G(TH)}$	N		$V_{GS} = 4.5$ V, $V_{DS} = 10$ V, $I_D = 2.9$ A		0.2		
		P		$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -3.2$ A		0.6		
Gate-to-Source Gate Charge	Q_{GS}	N	$V_{GS} = 4.5$ V, $V_{DS} = 10$ V, $I_D = 2.9$ A		0.4			
		P	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -3.2$ A		1.4			
Gate-to-Drain "Miller" Charge	Q_{GD}	N	$V_{GS} = 4.5$ V, $V_{DS} = 10$ V, $I_D = 2.9$ A		0.7			
		P	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -3.2$ A		2.5			

3. Pulse Test: pulse width ≤ 250 μ s, duty cycle $\leq 2\%$.

NTHD3100C

ELECTRICAL CHARACTERISTICS (continued) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)							
Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5\text{ V}, V_{DD} = 10\text{ V},$ $I_D = 2.9\text{ A}, R_G = 2.5\ \Omega$		6.3		ns
Rise Time	t_r				10.7		
Turn-Off Delay Time	$t_{d(OFF)}$				9.6		
Fall Time	t_f				1.5		
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V},$ $I_D = -3.2\text{ A}, R_G = 2.5\ \Omega$		5.8		
Rise Time	t_r				11.7		
Turn-Off Delay Time	$t_{d(OFF)}$				16		
Fall Time	t_f				12.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0\text{ V}, T_J = 25\ ^\circ\text{C}$	$I_S = 2.5\text{ A}$		0.8	1.15	V
		P		$I_S = -2.5\text{ A}$		-0.8	-1.2	
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0\text{ V},$ $dI_S / dt = 100\text{ A}/\mu\text{s}$	$I_S = 1.5\text{ A}$		12.5		ns
		P		$I_S = -1.5\text{ A}$		13.5		
Charge Time	t_a	N		$I_S = 1.5\text{ A}$		9.0		
		P		$I_S = -1.5\text{ A}$		9.5		
Discharge Time	t_b	N		$I_S = 1.5\text{ A}$		3.5		
		P		$I_S = -1.5\text{ A}$		4.0		
Reverse Recovery Charge	Q_{RR}	N		$I_S = 1.5\text{ A}$		6.0		nC
		P		$I_S = -1.5\text{ A}$		6.5		

4. Switching characteristics are independent of operating junction temperatures.

NTHD3100C

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

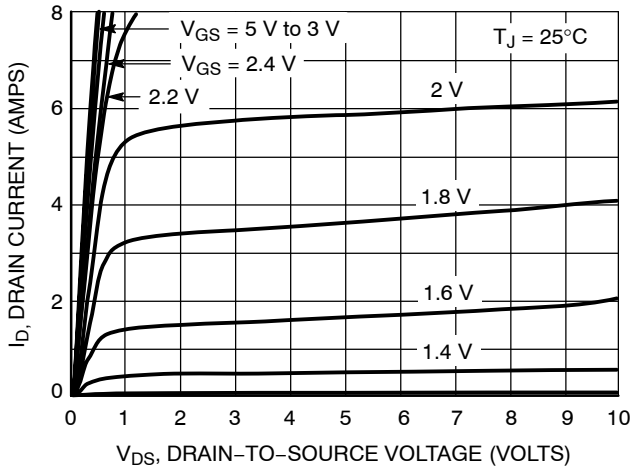


Figure 1. On-Region Characteristics

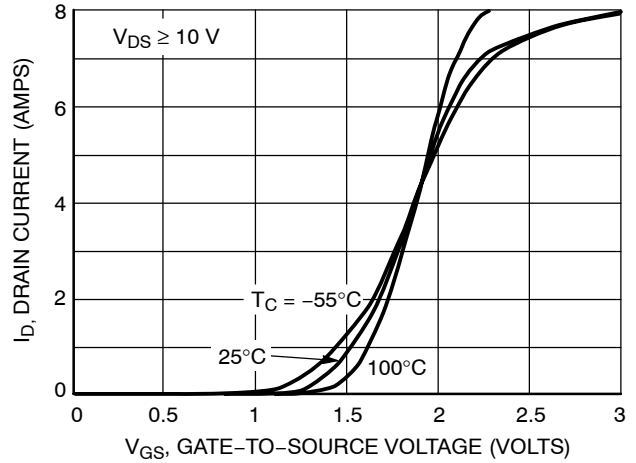


Figure 2. Transfer Characteristics

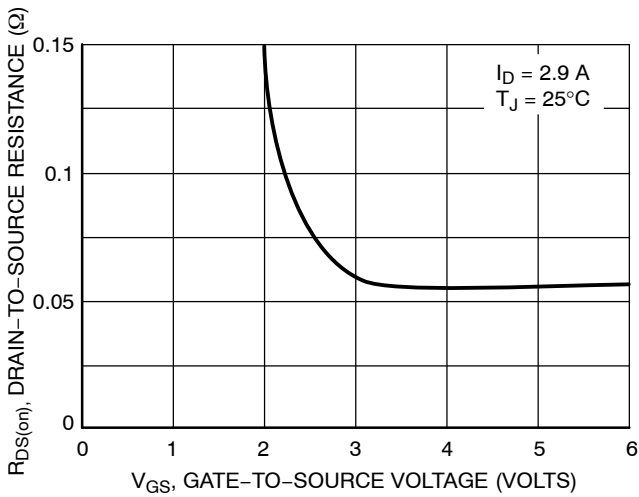


Figure 3. On-Resistance vs. Gate-to-Source Voltage

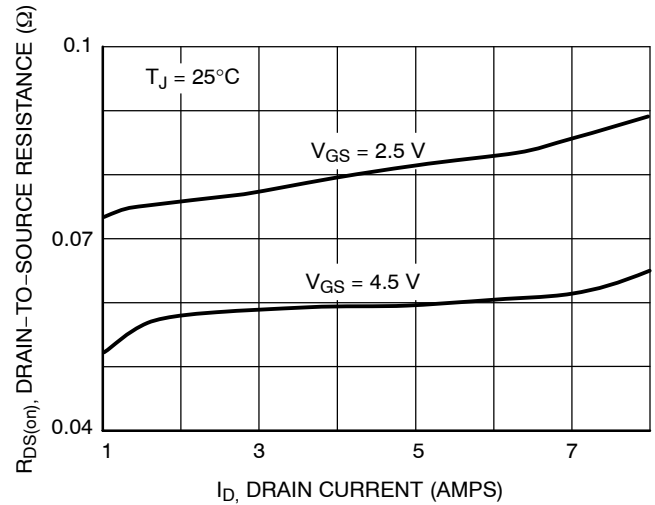


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

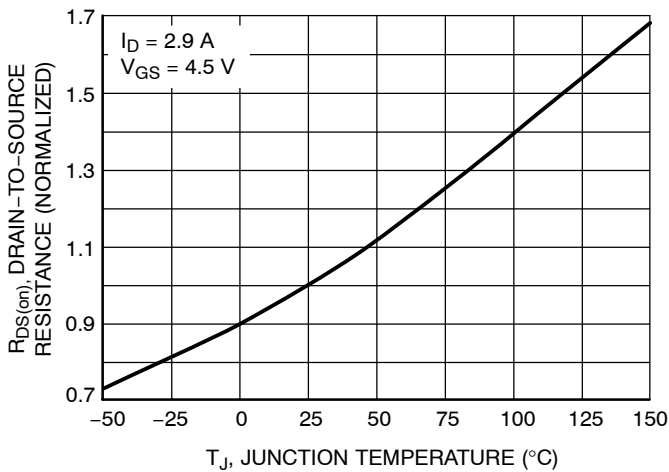


Figure 5. On-Resistance Variation with Temperature

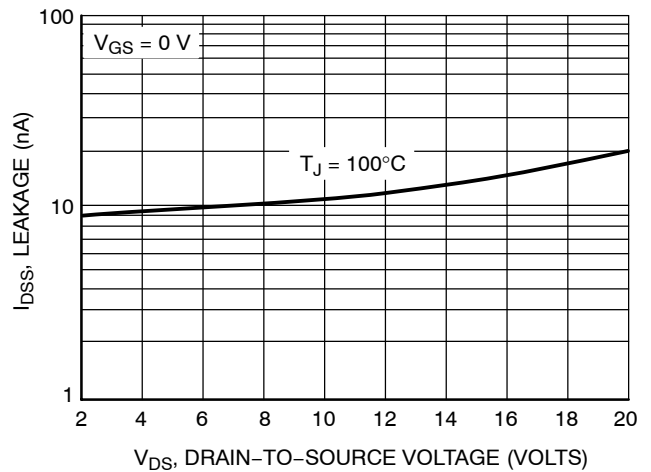


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTHD3100C

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

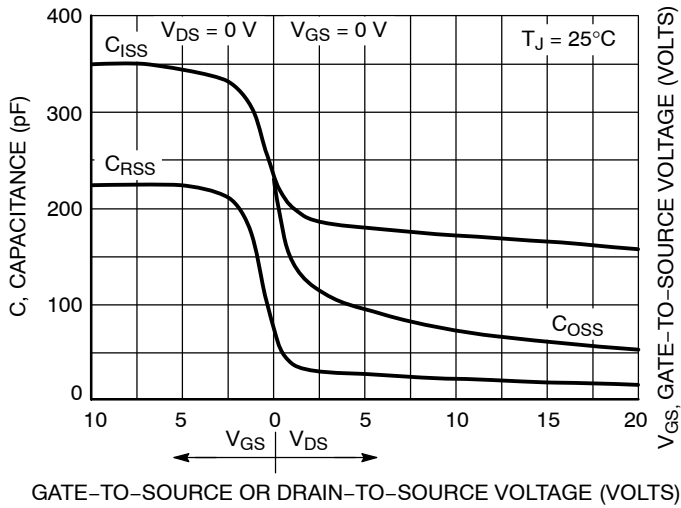


Figure 7. Capacitance Variation

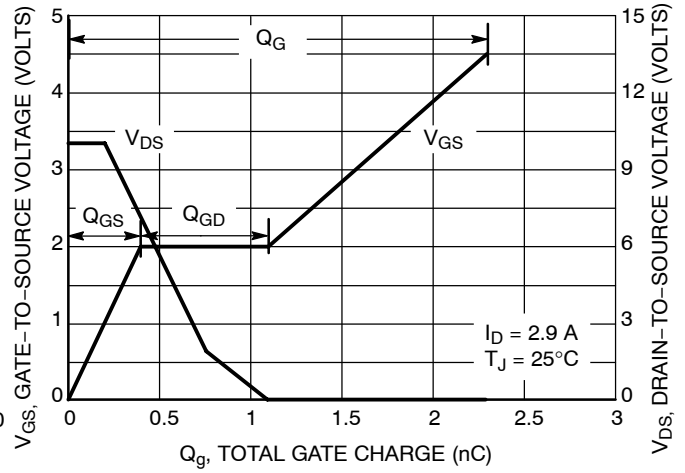


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

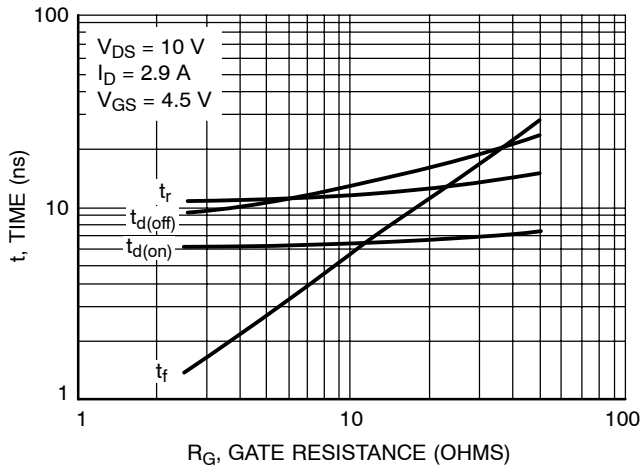


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

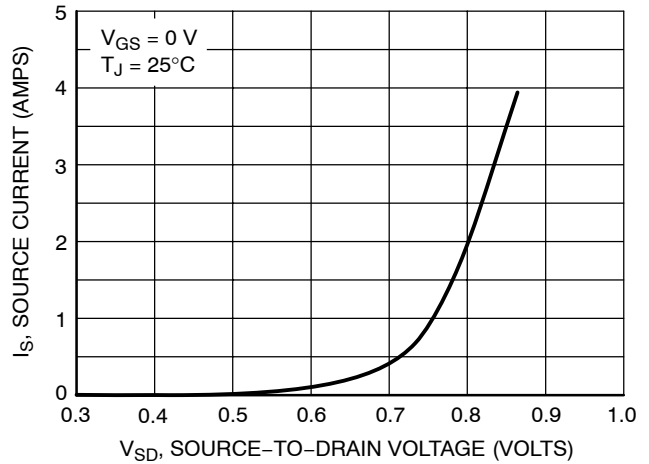


Figure 10. Diode Forward Voltage vs. Current

NTHD3100C

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

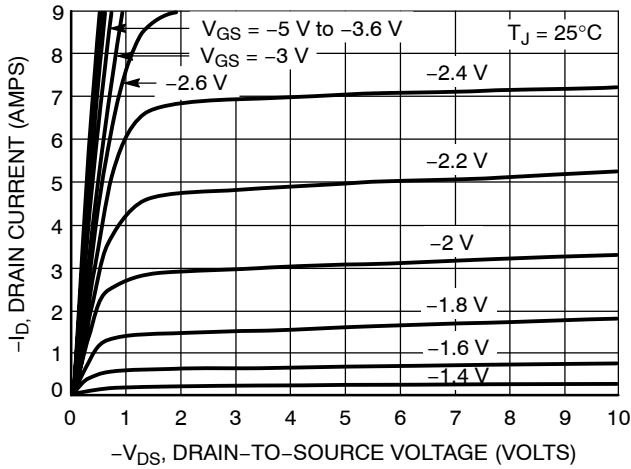


Figure 11. On-Region Characteristics

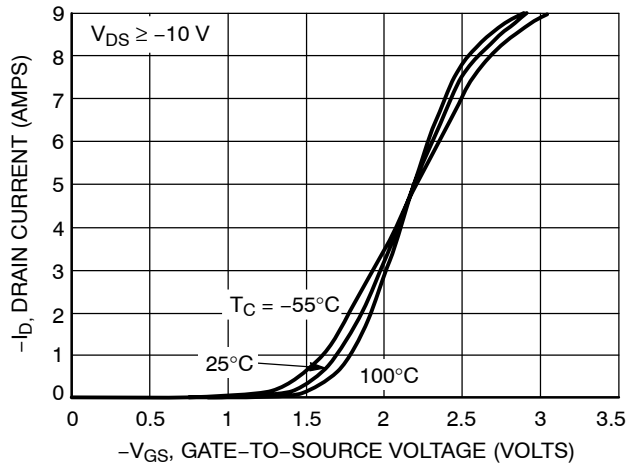


Figure 12. Transfer Characteristics

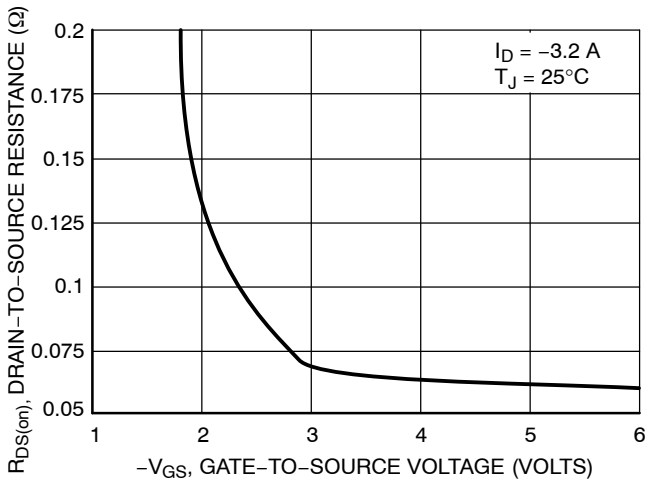


Figure 13. On-Resistance vs. Gate-to-Source Voltage

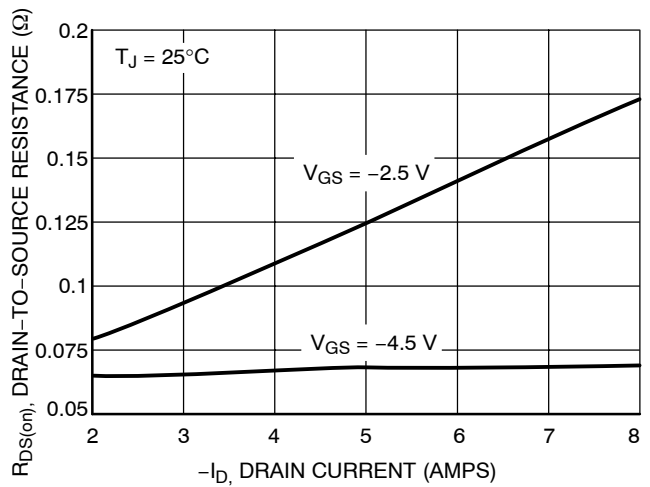


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

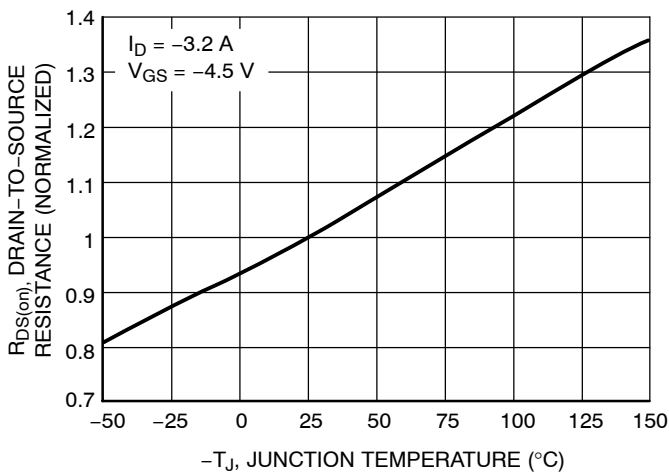


Figure 15. On-Resistance Variation with Temperature

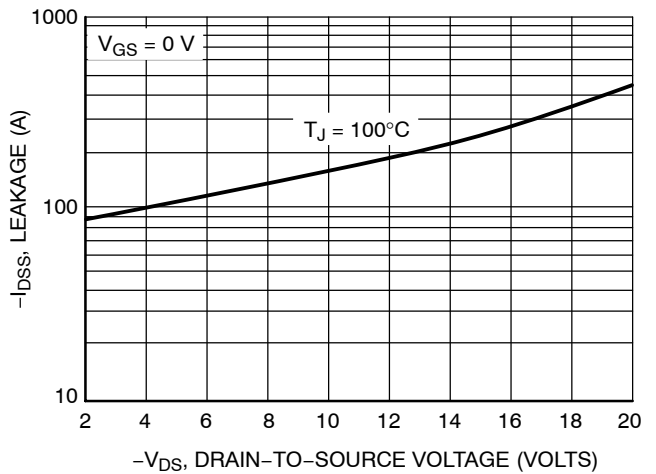


Figure 16. Drain-to-Source Leakage Current vs. Voltage

NTHD3100C

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

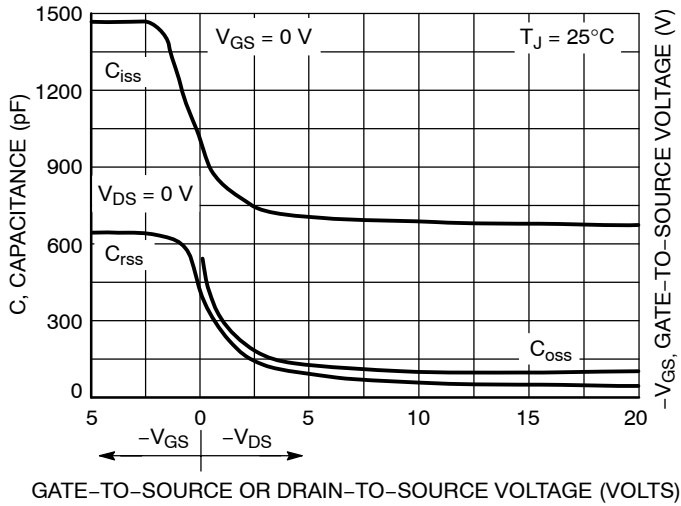


Figure 17. Capacitance Variation

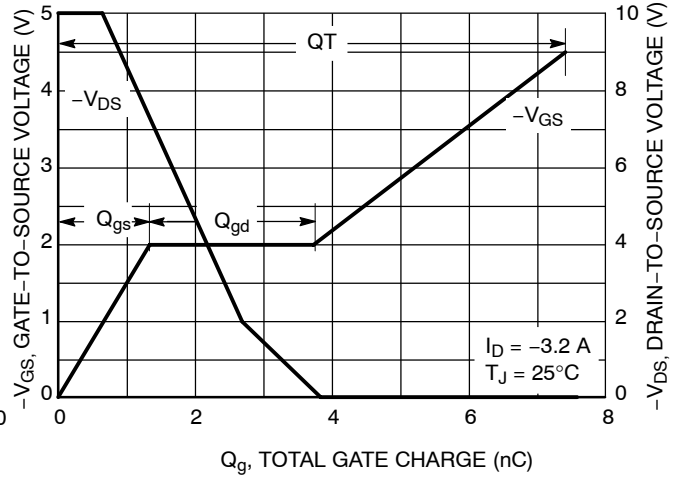


Figure 18. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

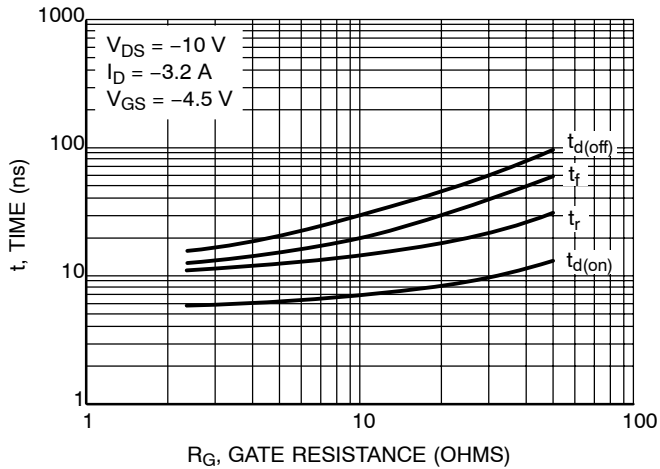


Figure 19. Resistive Switching Time Variation vs. Gate Resistance

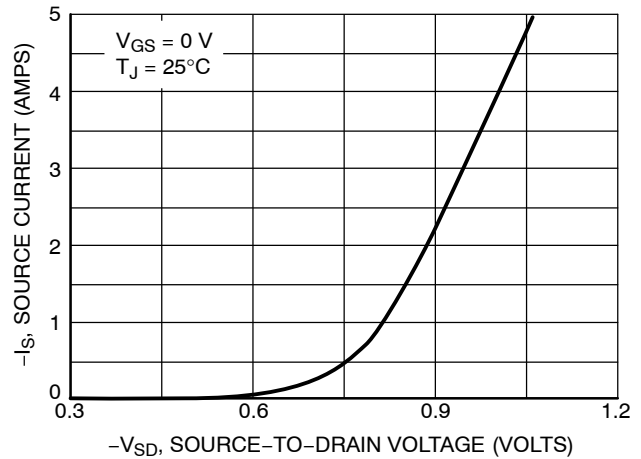


Figure 20. Diode Forward Voltage vs. Current

DEVICE ORDERING INFORMATION

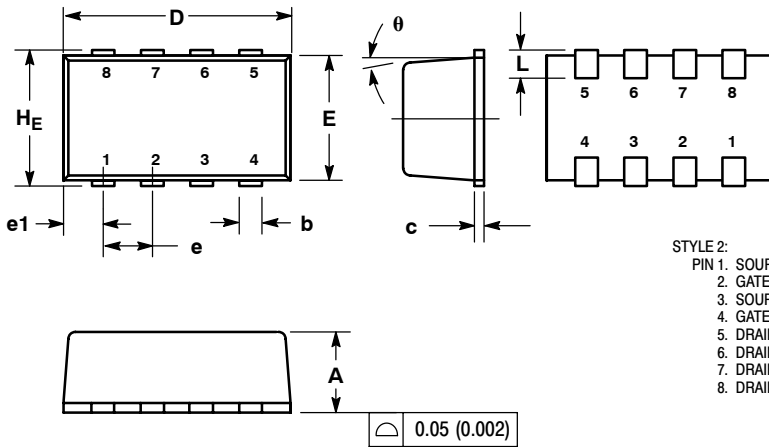
Device	Package	Shipping [†]
NTHD3100CT1	ChipFET	3000 / Tape & Reel
NTHD3100CT1G	ChipFET (Pb-Free)	3000 / Tape & Reel
NTHD3100CT3	ChipFET	10000 / Tape & Reel
NTHD3100CT3G	ChipFET (Pb-Free)	10000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD3100C

PACKAGE DIMENSIONS

ChipFET™
CASE 1206A-03
ISSUE G



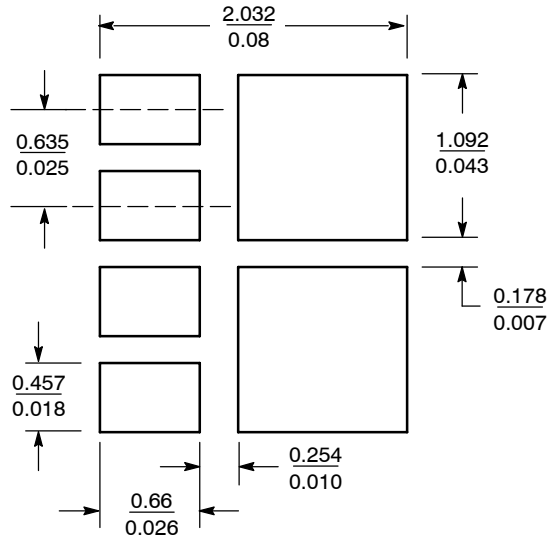
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H _E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

- STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ChipFET is a trademark of Vishay Siliconix.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.