EEPROM Programmable PLL Die for LVCMOS Crystal Oscillator

IDT5V7855

DATA SHEET

General Description

The IDT5V7855 is a programmable PLL-based clock generator used for crystal oscillator modules. The device incorporates an on-chip crystal oscillator with a programmable capacitor tuning array to support direct connection with fundamental-mode crystals between 16MHz – 50MHz. The capacitor tuning array offers a total of 9 bits of resolution and provides a step of 0.01pF.

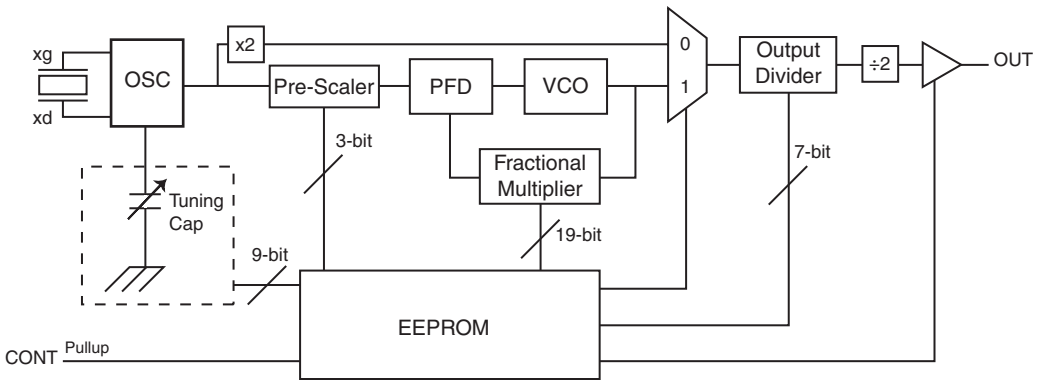
The device incorporates on-chip non-volatile EEPROM cells which can store all the device settings and maintain them even when there is no power. The serial programming interface is implemented with dual-use pins for the clock and data. The CONT input can be programmed as either a power down input or an output enable input. Crystal oscillator modules using this device can be stocked as blank parts and custom frequencies programmed in package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for expensive dedicated crystals.

The IDT PLL uses a patent-pending fractional multiplier technique to provide ultra-high resolution multiplication and division from input to output with low jitter. In addition, prescaler and post-divider circuits are included to enhance the granularity of clock scaling. The PLL may also be bypassed in order to operate the device as a non-PLL fundamental-mode crystal oscillator for applications that do not require frequency multiplication. The device is fabricated using advance technology and can support both 2.5V and 3.3V operation. The device is small enough to fit into small-footprint crystal oscillators. This is the industry's smallest programmable die and can support crystal oscillator packages as small as 20mm x 16mm.

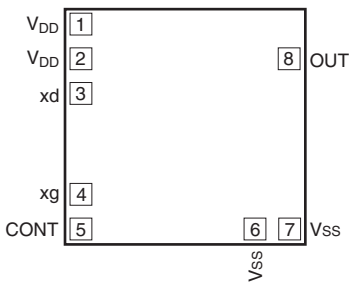
Features

- Input: 16MHz – 50MHz fundamental mode crystal
- Output frequency range: 1MHz – 170MHz in PLL mode, 1MHz – 50MHz in non-PLL mode
- On-chip EEPROM to store device configuration
  – 19-bit high-resolution fractional programmable multiplier
  – 3-bit prescaler
  – 7-bit output divider
  – 9-bit crystal oscillator tuning capacitor array
  – Selectable function power down or OE control pin
- In-package serial programming interface through dual-use pins
- Full 2.5V and 3.3V operating supply
- Maximum frequency shift across supply voltage: ±1ppm
- Available in die pack, lead-free RoHS compliant
- ESD Human Body Model (HBM) and Machine Model (MM):
  – HBM: 2000V
  – MM: 200V
- Small die size: 0.75mm x 0.75mm
- Supports 20mm x 16mm package size
- -40°C to 85°C ambient operating temperature

Functional Block Diagram



Pad Assignment



IDT5V7855

0.75mm x 0.75mm Die

Table 1. Pad Descriptions

Number	Name	Type		Description
1, 2	V_{DD}	Power		Power supply pins. Both pads must be bonded.
3, 4	xd, xg	Input		Crystal oscillator interface. xg is the input. xd is the output.
5	CONT	Input	Pullup	Programmable to function as power down or output enable. Serves as VPP and data input during programming mode.
6, 7	V_{SS}	Power		Power supply ground. Only one pad should be bonded. Either pad can be used to accommodate optimal bond wire placement
8	OUT	I/O		Single-ended clock output. Serves as clock input during programming mode.

NOTE: *Pullup* refers to internal input resistor.

Table 2. Pad Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DD} = 3.3V		25		Ω
		V_{DD} = 2.5V		37		Ω

Functional Description

The output frequency of the IDT5V7855 is determined by the crystal frequency and the three programmable divider/multiplier registers: Prescaler (P), Fractional Multiplier (M), and Output Divider (D). The prescaler (P) is a 3-bit integer register while the output divider (D) is a 7-bit integer register. The fractional multiplier (M) is a 19-bit register and has the feature of a fractional component in addition to the integer value. This allows the IDT5V7855 to be programmed to a wide variety of output frequencies from a single input crystal frequency.

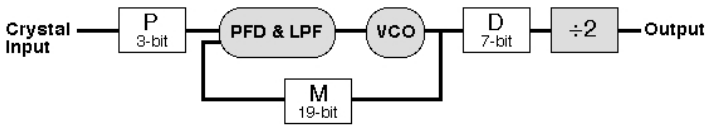


Figure 1. Simplified Block Diagram

The actual values which may be programmed into the various registers depend on the specified operational ranges of some of the PLL components such as the VCO and crystal oscillator. As shown in tables 5 and 6A, these ranges are:

VCO Range: 170MHz to 340MHz
XTAL Oscillator Range: 16MHz to 50MHz

The minimum value permitted for the feedback register is a function of the minimum VCO frequency and the maximum phase detector reference frequency. The maximum phase detector reference frequency is set by the maximum crystal frequency (50MHz) divided by the minimum prescaler divider (1) and is therefore 50MHz. The feedback fractional multiplier register operational range can be determined as:

M Min: 170MHz ÷ 50MHz = 3.4
M Max: 31.9993896 ≈ 32

The maximum value that can be programmed into the fractional multiplier (all 19 bits "1") is approximately 32 (actual value is 31.99993896).

Given the VCO range and the feedback divider range, the minimum phase detector frequency can be determined from the minimum VCO frequency and the maximum feedback divider as:

Phase Detector Min: 170MHz ÷ 32 = 5.3125MHz
Phase Detector Max: 50MHz

The maximum value is set by the specified maximum crystal frequency.

Prescaler (P)

The Prescaler (P) divides down the input crystal frequency prior to the internal phase detector. The prescaler register is a 3-bit register so the possible values which may be programmed are 1 through 7.

The specified input crystal frequency range is: 16MHz to 50MHz and the phase detector range is: 5.3125MHz to 50MHz. So the possible settings and ranges are:

Table 3A. Prescaler Table

Crystal Range (MHz)	Prescaler (P)	Phase Detector Frequency (MHz)
16 – 50	1	16 – 50
16 – 50	2	8 – 25
16 – 50	3	5.3333 – 16.6667
21.25 – 50	4	5.3125 – 12.5
26.5625 – 50	5	5.3125 – 10
31.875 – 50	6	5.3125 – 8.3333
37.1875 – 50	7	5.3125 – 7.1429

Fractional Multiplier (M)

The Fractional Multiplier (M) is a 19-bit register. The operational range of the fractional multiplier is 3.4 to approximately 32 (actually 31.99993896). The decimal multiplier value obtained from the 19-bit fractional multiplier register can be determined as:

$$M_{DEC} = \frac{M_{BIN}}{16384}$$

$\mathbf{M_{DEC}}$ is the fractional multiplier (decimal) value

$\mathbf{M_{BIN}}$ is the value programmed in the 19-bit register

The fractional portion of the fractional multiplier allows a programming frequency resolution to $61/M_{DEC}$ ppm. Note that higher M_{DEC} values will produce lower ppm error.

Examples:

For a fractional multiplier register M_{BIN} of 1010101000000000000 binary

$$M_{DEC} = \frac{348160}{16384} = 21.2500$$

The ppm resolution (single LSB bit change in the M_{BIN}) for this setting is:

$$\frac{61ppm}{21.25} = 2.9ppm$$

For a fractional multiplier register M_{BIN} of 0010101010000000000 binary

$$M_{DEC} = \frac{87040}{16384} = 5.3125$$

The ppm resolution (single LSB bit change in the M_{BIN}) for this setting is:

$$\frac{61ppm}{5.3125} = 11.5ppm$$

Output Divider (D)

The Output Divider register is a 7-bit register so the possible values which may be programmed are 1 through 127. Combining the information from the three registers, including the final output divider and the crystal frequency, the output frequency may be derived.

The actual frequency produced from a given crystal frequency may be determined as:

$$FOUT = (FXTAL) \times \frac{MDEC}{P \times (D \times 2)}$$

F_{OUT} is the output frequency
F_{XTAL} is the Crystal Frequency
P is the Prescaler Value
D is the Output Divider Value
M_{DEC} is the Fractional Divider (decimal) Value

Fine Frequency Adjustment

The IDT5V7855 also has a fine frequency adjustment capability utilizing adjustable tuning capacitors in the crystal oscillator. These capacitors are set through a tuning capacitor register which is a 9-bit register and the resolution of the tuning capacitance is approximately 0.01pF per bit. The frequency ppm tuning performance can be found by:

$$FREQ(ppm) = \frac{C1}{2} \times \left(\frac{1}{C0 + CL + C_{STEP} \times T_{REG}} - \frac{1}{C0 + CL} \right) \times 10^6 ppm$$

C1 is the Crystal Motional Capacitance
C0 is the Crystal Shunt Capacitance
CL is the Inherent (parasitic) Load Capacitance
C_{STEP} is the Tuning Capacitance Resolution 0.01pF
T_{REG} is the Tuning Capacitor Register Value from 0 to 511

Determining the Appropriate Register Settings

A typical use for this type of device is generating virtually any frequency between 1MHz to 170MHz from a single crystal frequency value. The steps required to accomplish this are:

1. Determine the crystal frequency.
2. Determine the desired output frequency.
3. Determine the proper prescaler value using the crystal frequency and the associated phase detector frequency.
4. Determine the proper output divider using the desired output frequency to optimize the internal VCO frequency.
5. Determine the appropriate fractional multiplier value using the phase detector frequency and the VCO frequency.
6. Determine the M_{BIN} value by multiplying the M_{DEC} value by 16384.

Using table 3B, identify the crystal frequency from the given ranges and select the associated prescaler (P) value. The phase detector frequency is then calculated as:

$$F_{PHASE-DET} = \left(\frac{F_{XTAL}}{P} \right)$$

Table 3B. Crystal Range Table

Crystal Range (MHz)	Prescaler (P)	Phase Detector Frequency (MHz)
16 – 50	1	16 – 50
16 – 50	2	8 – 25
16 – 50	3	5.3333 – 16.6667
21.25 – 50	4	5.3125 – 12.5
26.5625 – 50	5	5.3125 – 10
31.875 – 50	6	5.3125 – 8.3333

Identify the range(s) that match the desired output frequency and select the associated Output Divider (D) value. The VCO frequency is then calculated as:

$$F_{VCO} = (F_{OUT} \times D \times 2)$$

Table 3C. F_{VCO} Table

Output Frequency Range (MHz) F_{OUT}	Output Divider (D)	VCO Frequency (MHz)
85.0000 – 170.0000	1	170 – 340
42.5000 – 85.0000	2	170 – 340
28.3333 – 56.6667	3	170 – 340
21.2500 – 42.5000	4	170 – 340
17.0000 – 34.0000	5	170 – 340
14.1667 – 28.3333	6	170 – 340
• • •	• • •	• • •
0.6800 – 1.3600 (NOTE)	125	170 – 340
0.6746 – 1.3492 (NOTE)	126	170 – 340
0.6693 – 1.3386 (NOTE)	127	170 – 340

NOTE: The specified minimum output frequency is 1MHz. While output frequencies less than 1MHz are possible, specified device performance is not guaranteed.

The fractional multiplier is determined from the phase detector frequency and the VCO frequency using the following equations.

Calculate the fractional multiplier decimal value:

$$M_{DEC} = \frac{F_{VCO}}{F_{PHASE-DET}}$$

Calculate the fractional multiplier register binary value:

$$M_{BIN} = M_{DEC} \times 16384$$

Example 1:

The crystal frequency is 27MHz and the desired output frequency is 166.66667MHz.

1. With a crystal frequency of 27MHz, the appropriate prescaler value is 1 and the associated phase detector frequency would be: 27MHz ÷ 1 = 27MHz.
2. For an output frequency of 166.6667MHz, the output divider which can be used with a VCO frequency in the proper 170MHz to 340MHz range is 1, and the resulting VCO frequency is: 166.6667MHz x 1 x 2 = 333.33MHz.
3. The fractional multiplier is calculated as the VCO frequency divided by the phase detector frequency or 333.33MHz ÷ 27MHz = 12.345679.
4. The M_{BIN} is found by 12.345679 x 16384 = 202271.6 and is rounded to 202272.
5. Due to the rounding, the actual M_{DEC} value will be 12.3457 and the actual output frequency will be:

$$F_{OUT} = F_{XTAL} \times \frac{M_{DEC}}{P \times (D \times 2)} = 27MHz \times \frac{12.3457}{1 \times 1 \times 2}$$

F_{OUT} = 166.66699MHz
(NOTE: This is an error of only 1.94ppm.)

Example 2:

The starting crystal frequency is 48MHz and the desired output frequency is 25MHz.

1. With a starting crystal frequency of 48MHz, the appropriate prescaler value can be either 1, 2 or 3 and the associated phase detector frequency would be either:
48MHz ÷ 1 = 484MHz,
48MHz ÷ 2 = 24MHz or,
48MHz ÷ 3 = 16MHz.
2. For an output frequency of 25MHz, the output dividers which can be used with a VCO frequency in the proper 170MHz to 340MHz range are: 4, 5, or 6, and the resulting VCO frequencies is: 200MHz, 250MHz, or 300MHz.
3. The fractional multiplier is calculated as the VCO frequency divided by the phase detector frequency. So, for the possible combinations identified, the resulting fractional multiplier could be one of nine possibilities.

Table 3D. Fractional Multiplier Table

	P = 1 F_{PHASE_DET} (48MHz)	**P = 2 F_{PHASE_DET} (24MHz)**	**P = 3 F_{PHASE_DET} (16MHz)**
D = 4 F_{VCO} = 200MHz	$M_{DEC} = \frac{200MHz}{48MHz}$ 4.16666	$M_{DEC} = \frac{200MHz}{24MHz}$ 8.33333	$M_{DEC} = \frac{200MHz}{16MHz}$ 12.5
D = 5 F_{VCO} = 250MHz	$M_{DEC} = \frac{250MHz}{48MHz}$ 5.20833	$M_{DEC} = \frac{250MHz}{24MHz}$ 10.41666	$M_{DEC} = \frac{250MHz}{16MHz}$ 15.625
D = 6 F_{VCO} = 300MHz	$M_{DEC} = \frac{300MHz}{48MHz}$ 6.5	$M_{DEC} = \frac{300MHz}{24MHz}$ 12.5	$M_{DEC} = \frac{300MHz}{16MHz}$ 18.75

4. With the different M_{DEC} values to choose from, how does one select the 'best' value? In general, selecting a fractional value which reduces the ppm error is the first selection criteria. This applies to M_{DEC} values which have the fewest non-zero decimal places or M_{DEC} values which have large integer values. This criteria would eliminate the M_{DEC} = 4.16666, 5.208333, 8.33333, and 10.4166666 options. After the ppm error selection is made and if there are still other options, generally the higher VCO frequency will provide better performance. In this example, the higher VCO frequency corresponds with D = 6 and the associated P and M_{DEC} values of 1 and 6.25, 2 and 12.5, or 3 and 18.75. Lastly, the higher phase detector frequency generally provides better performance. So for this example, the condition of P = 1, M_{DEC} = 6.25, and D = 6 would be the preferred choice.
5. The M_{BIN} is found by: 6.25 x 16384 = 102400. (No rounding is necessary.)
6. Verifying the values

$$F_{OUT} = F_{XTAL} \times \frac{M_{DEC}}{P \times (D \times 2)} = 48MHz \times \frac{12.5}{2 \times 6 \times 2}$$

Programming Instructions

The IDT5V7855 registers, along with some control functions, are written and the EEPROM burned through a serial write using the CONT and OUT pins. During the programming the CONT pin functions as a Data input while the OUT pin functions as a Clock input. The data registers are not addressed individually but are all written sequentially with the most significant bit first. All registers must be written when programming the device. The order of registers / control bits and the number of bits per register are:

9 bits	Tuning Capacitor Register T[8:0]
19 bits	Fractional Multiplier Register M[18:0]
3 bits	Prescaler Register P[2:0]
3 bits	Factory Test Mode Register F[2:0]
1 bit	PLL Bypass Mode (0 = crystal oscillator connected directly to output divider, 1 = PLL used)
1 bit	Power Down Control (0 = CONT acts as an output enable, 1 = CONT acts as power down)
1 bit	Output Enable Type (0 = synchronous output enable, 1 = asynchronous output enable)
7 bits	Output Divider Register D[6:0]

Table 3E. Register Table

Register Name	Tuning Capacitor	Fractional Multiplier	Prescaler (P)	Factory Test Mode	PLL Mode	Power Down Control	Output Enable Control	Output Divider
# of Bits	9-bit	19-bit	3-bit	3-bit	1-bit	1-bit	1-bit	7-bit
Symbol	T[8:0]	M[18:0]	P[2:0]	F[2:0]				D[6:0]

The procedure to program the registers and control bits without writing to the EEPROM is as follows:

1. Set CONT and OUT to 0.0 volts with no power applied.
2. Apply power, wait for 1ms.
3. Apply four clock pulses on OUT to enter serial programming mode (see timing diagram below).
4. Enter serial data (bit order as described above) via the CONT pin, with a positive pulse on OUT pin for each data bit.
   NOTE: CONT must only change while OUT is LOW to write the data properly.
5. To activate the registers and exit serial programming mode, while OUT is held LOW, set CONT HIGH.
   After 1µs with CONT still HIGH, set OUT HIGH. After 1µs with OUT still HIGH, set CONT LOW.
6. Remove the programming voltage from OUT pin.
7. Enable the output by setting CONT HIGH.

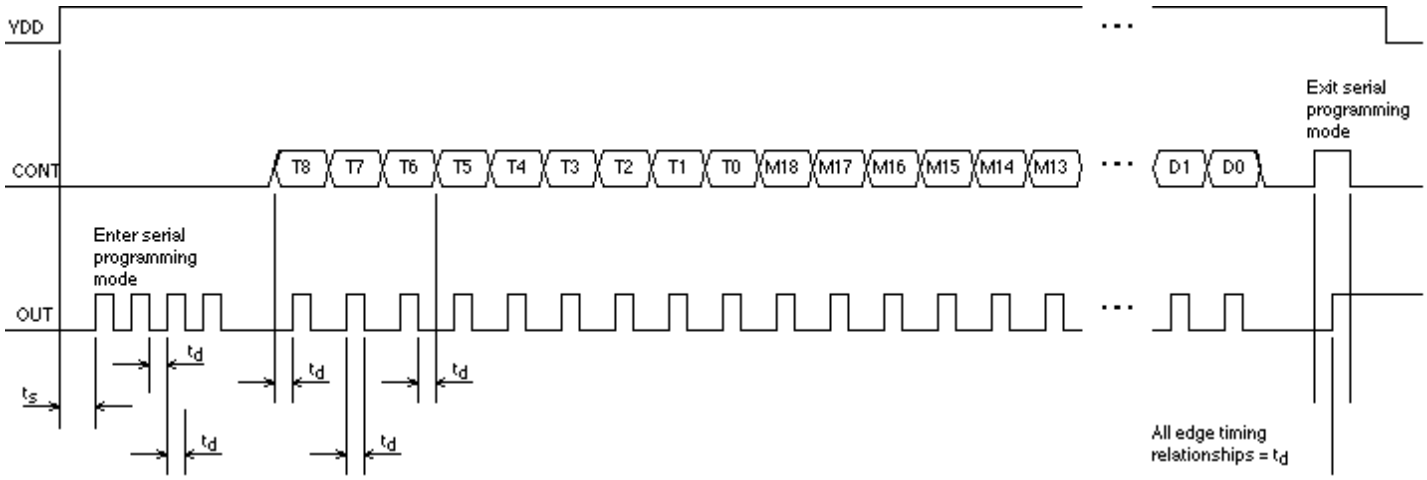


Figure 2. Timing Diagram

3F. Timing/Voltage Requirements Table

Symbol	Parameter	Minimum	Maximum	Units
t_s	Enter Serial Data Mode	1		ms
t_d	Data & Clock Timing	1		µs
V_{DD}	Supply Voltage	2.2	3.6	V

The procedure to program the registers and control bits and write the data to the EEPROM is as follows:

1. Set CONT and OUT to 0.0 volts with no power applied.
2. Apply power, wait for 1ms.
3. Apply four clock pulses to OUT to enter serial programming mode (see timing diagram below).
4. Wait 1ms.
5. Apply EEPROM programming pulse (12V) on CONT to erase EEPROM.
   [WARNING: Do not apply High Voltage Programming pulse prior to entering serial mode.]
6. Wait 1ms.
7. Enter serial data (bit order as described above) via the CONT pin, with a positive pulse on OUT pin for each data bit.
   NOTE: CONT must only change while OUT is LOW to write the data properly.
8. Complete the serial write with a Stop Bit set to 0.
9. Wait 1ms
10. While OUT is held LOW, apply EEPROM programming pulse (12V) to CONT to store the data in EEPROM.
11. Remove power from the device.

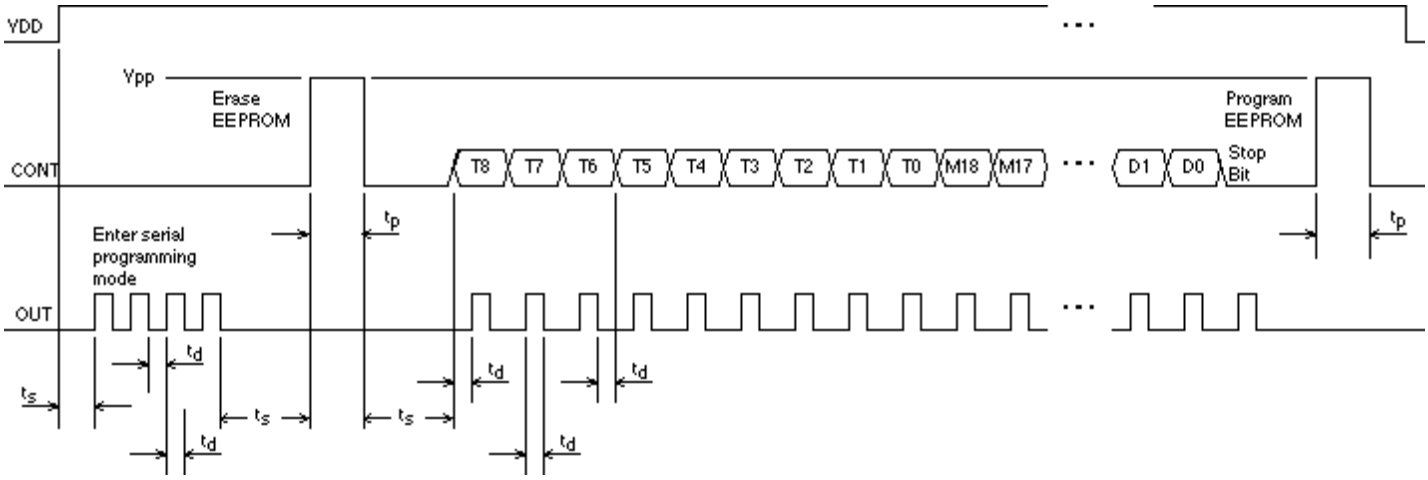


Figure 3. Timing Diagram

3G. Timing/Voltage Requirements Table

Symbol	Parameter	Test Conditions	Minimum	Maximum	Units
t_s	Enter Serial Data Mode		1		ms
t_d	Data & Clock Timing		1		µs
t_p	Programming EEPROM Timing		100	110	ms
t_R / t_F	Rise/Fall Time of V_{PP}	10% - 90%		5	ms
V_{DD}	Supply Voltage; NOTE		2.2	3.6	V
V_{PP}	Programming EEPROM Voltage		11.5	12.5	V

NOTE: The supply voltage on V_{DD} must be able to sink at least 2mA when V_{PP} is applied to CONT to ensure transient currents are safely absorbed. Alternatively, a 1kΩ resistor may be connected between V_{DD} and GND during programming.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs/Outputs, V_I / $V_{O;}$ NOTE	-0.5V to V_{DD} + 0.5V
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: 12.5V can be applied to the CONT pin during serial programming mode only after applying four clock pulses to the OUT pin.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.3V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage			2.3	3.0	3.6	V
I_{DD}	Power Supply Current	No Load	f_{OUT} = 50MHz, Non-PLL mode			6	mA
		No Load	f_{OUT} = 170MHz, PLL mode			15	mA
		PWRDN	Power-Down Mode			40	µA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.7V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{OUT} = ≥ V_{OH} (min.)	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{OUT} = ≤ V_{OH} (max.)	-0.3		0.8	V
I_{IN}	Input Current	CONT	V_{IN} = max.;			±5	µA
		OUT	V_{IN} = 0V or V_{IN} = V_{DD}			±15	
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{DD} = min. V_I = V_{IH} or V_{IL}	V_{DD} – 0.2			V
		I_{OH} = -4mA		2.2			
V_{OL}	Output Low Voltage	I_{OL} = 100µA	V_{DD} = min. V_I = V_{IH} or V_{IL}			0.2	V
		I_{OL} = 4mA				0.4	

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.3V to 2.7V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{OUT} = ≥ V_{OH} (min.)	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{OUT} = ≤ V_{OH} (max.)	-0.3		0.7	V
I_{IN}	Input Current	CONT	V_{IN} = max.;			±5	µA
		OUT	V_{IN} = 0V or V_{IN} = V_{DD}			±15	
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{DD} = min.; V_I = V_{IH} or V_{IL}	2.1			V
		I_{OH} = -1mA		2			
		I_{OH} = -2mA		1.7			
V_{OL}	Output Low Voltage	I_{OH} = -100µA	V_{DD} = min.; V_I = V_{IH} or V_{IL}			0.2	V
		I_{OH} = -1mA				0.4	
		I_{OH} = -2mA				0.7	

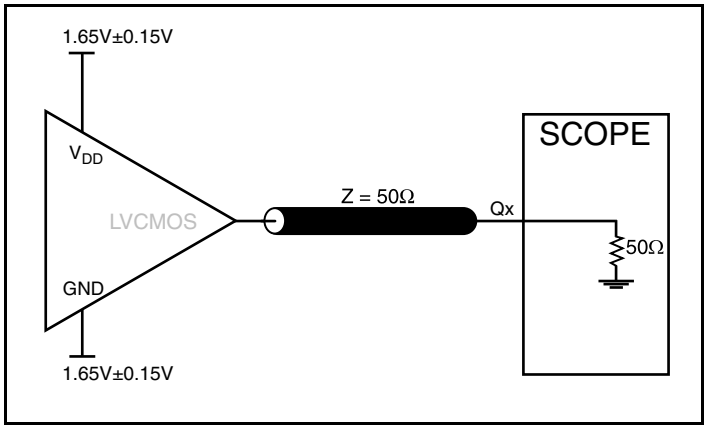
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 2.3V to 3.6V, T_A = -40°C to 85°C

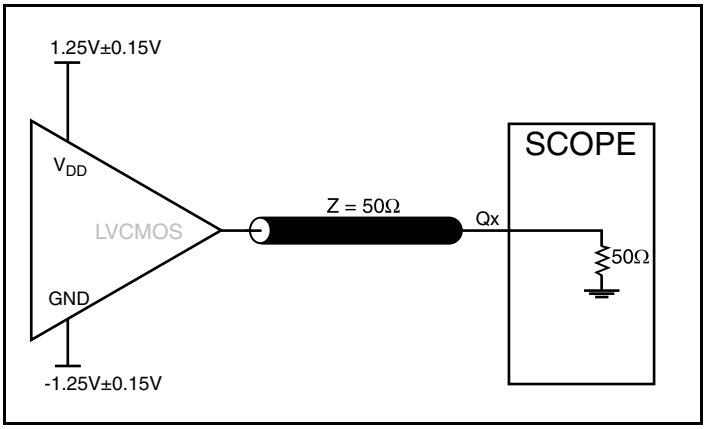
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency			170		340	MHz
f_{OUT}	Output Frequency	PLL Mode		1		170	MHz
		Non-PLL Mode		1		50	MHz
$t_{jit(per)}$	Period Jitter, RMS; NOTE 1, 2	PLL Mode	Measured over 50,000 cycles; f_{OUT} > 40MHz			30	ps
		Non-PLL Mode	Measured over 50,000 cycles; f_{OUT} > 16MHz			9	ps
t_{p-p}	Peak-to-Peak Jitter; NOTE 1, 2	PLL Mode	Measured over 50,000 cycles; f_{OUT} > 40MHz			230	ps
		Non-PLL Mode	Measured over 50,000 cycles; f_{OUT} > 16MHz			90	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1, 2	PLL Mode	Measured over 50,000 cycles; f_{OUT} > 40MHz			130	ps
		Non-PLL Mode	Measured over 50,000 cycles; f_{OUT} > 16MHz			75	ps
t_R / t_F	Output Rise/Fall Time; NOTE 2		f_{OUT} > 40MHz, 20% to 80%	100		700	ps
odc	Output Duty Cycle; NOTE 2		PLL	48		52	%
			Bypass	45		55	%
t_{OSC}	Oscillation Startup Time					10	ms

NOTE 1: Measured on Wavecrest SIA3000.
NOTE 2: Output terminated with 50Ω to V_{DD}/2.

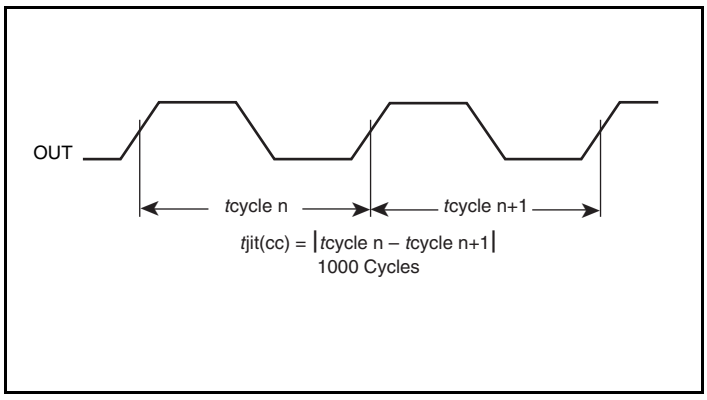
Parameter Measurement Information



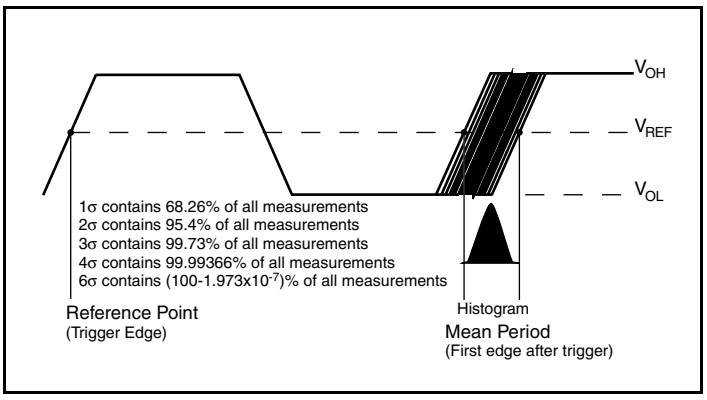
3.3V Output Load AC Test Circuit



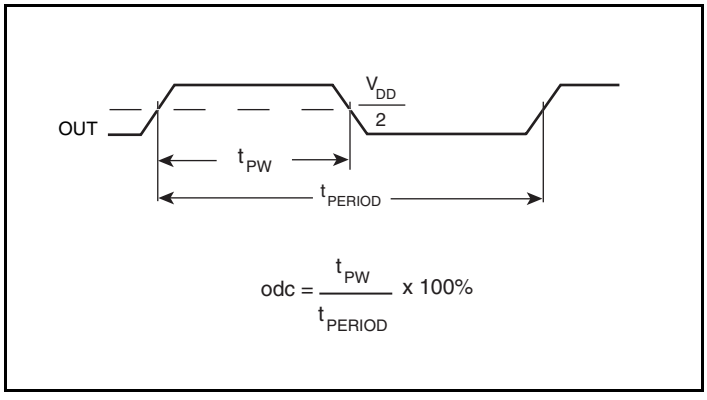
2.5V Output Load AC Test Circuit



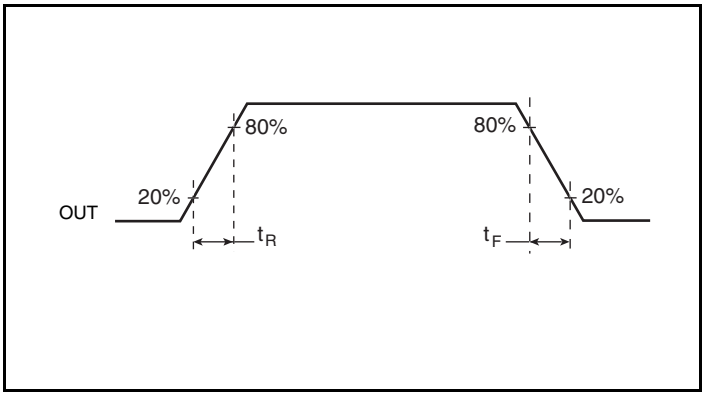
Cycle-to-Cycle Jitter



Period Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Pad Information

Table 7. Bond Pad Coordinates

Pad	Name	Pad Size (µm)	Coordinates	
			X(µm)	Y(µm)
1	V_{DD}	75 x 75	-266	266
2	V_{DD}	75 x 75	-266	161
3	xd	75 x 75	-266	56
4	xg	75 x 75	-266	-161
5	CONT	75 x 75	-266	-266
6	V_{SS}	75 x 75	161	-266
7	V_{SS}	75 x 75	266	-266
8	OUT	75 x 75	191	219

NOTE: Pad locations specify the center of the pad relative to the center of the die.
NOTE The substrate of the die should be connected to V_{SS}.
NOTE: Not all of the V_{SS} pads need to be bonded, but all of the V_{DD} pads need to be bonded.

Ordering Information

Table 8. Ordering Information

Part/Order Number	Package	Shipping Packaging	Temperature
5V7855-DPK	Die	Waffle	-40°C to 85°C
5V7855SWFR	Sawn Wafer	Film Frame	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		7	Deleted procedure 5. *Complete the serial write with a Stop Bit set to 0.* Updated Figure 2. Timing Diagram.	2/20/08
A	T8	12	Ordering Information Table - added Sawn Wafer package.	3/11/10

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056