CADEKA
Amplify the Human Experience

SPT7863

10-BIT, 40 MSPS, 160 mW A/D CONVERTER

TECHNICAL DATA

AUGUST 21, 2001

FEATURES

- Monolithic 40 MSPS converter
- 160 mW power dissipation
- On-chip track-and-hold
- Single +5 V power supply
- TTL/CMOS outputs
- 5 pF input capacitance
- Low cost
- Tri-state output buffers
- High ESD protection: 3,500 V minimum
- Selectable +3 V or +5 V logic I/O

APPLICATIONS

- All high-speed applications where low power dissipation is required
- Video imaging
- Medical imaging
- Radar receivers
- IR imaging
- Digital communications

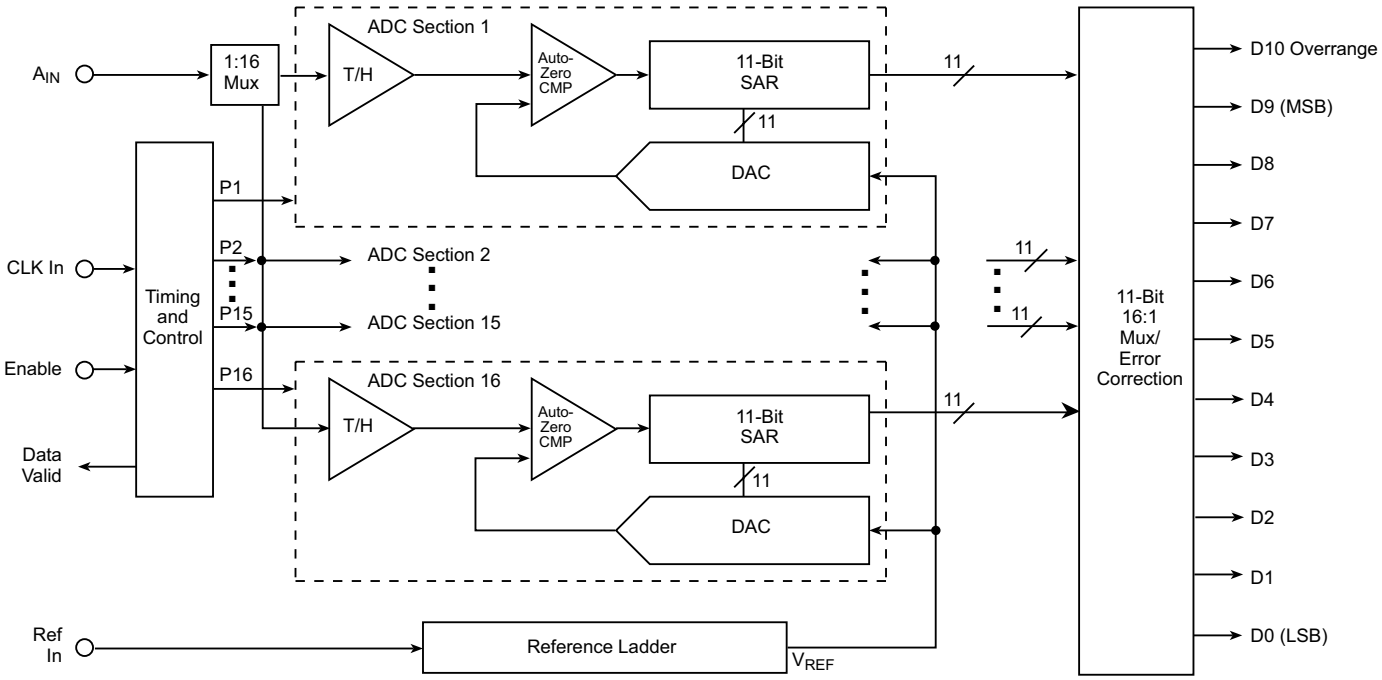
GENERAL DESCRIPTION

The SPT7863 is a 10-bit monolithic, low-cost, ultralow-power analog-to-digital converter capable of minimum word rates of 40 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7863's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 160 mW typical at 40 MSPS with a power supply of +5.0 V. The digital outputs are +3 V or +5 V, and are user selectable. The SPT7863 is pin-compatible with an entire family of 10-bit, CMOS converters (SPT7835/40/50/55/60/61), which simplifies upgrades. The SPT7863 has incorporated proprietary circuit design and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7863 is available in 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... –0.5 V to AV_{DD} +0.5 V
V_{REF} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
$AV_{DD} – DV_{DD}$ ..... ±100 mV
AGND – DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}=OV_{DD}=+5.0$ V, $V_{IN}=0$ to 4 V, f_S=40 MSPS, V_{RHS}=4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7863 MIN	SPT7863 TYP	SPT7863 MAX	UNITS
Resolution			10			Bits
DC Accuracy	51% duty cycle					
Integral Linearity Error (ILE)		VI		±1.0		LSB
Differential Linearity Error (DLE)		VI		±0.5		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range		VI	V_{RLS}		V_{RHS}	V
Input Resistance		IV	50			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V	250			MHz
Offset		V		±2.0		LSB
Gain Error		V		±0.2		%
Reference Input						
Resistance		VI	300	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0		2.0	V
V_{RHS}		IV	3.0		AV_{DD}	V
$V_{RHS} – V_{RLS}$		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} – V_{RHS})$		V		90		mV
$\Delta(V_{RLS} – V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		VI	40			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		4.0		ns
Aperture Jitter Time		V		30		ps (p-p)
Dynamic Performance						
Effective Number of Bits (ENOB)						
f_{IN} = 3.58 MHz		VI		9.2		Bits
f_{IN} = 10 MHz		V		8.7		Bits
Signal-to-Noise Ratio (SNR) (without Harmonics)						
f_{IN} = 3.58 MHz		VI	55	57		dB
f_{IN} = 10 MHz		V		54		dB

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}=OV_{DD}=+5.0$ V, $V_{IN}=0$ to 4 V, $f_S=40$ MSPS, $V_{RHS}=4.0$ V, $V_{RLS}=0.0$ V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7863 MIN	SPT7863 TYP	SPT7863 MAX	UNITS
Dynamic Performance						
Total Harmonic Distortion (THD)						
f_{IN} = 3.58 MHz		VI	64	67		dB
f_{IN} = 10 MHz		V		62		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN} = 3.58 MHz		VI	54	57		dB
f_{IN} = 10 MHz		V		54		dB
Spurious Free Dynamic Range	f_{IN} = 3.580 MHz	V		70		dB
Differential Phase		V		±0.3		Degree
Differential Gain		V		±0.3		%
Inputs						
Logic 1 Voltage		VI	2.0			V
Logic 0 Voltage		VI			0.8	V
Maximum Input Current Low		VI	–10		+10	µA
Maximum Input Current High		VI	–10		+10	µA
Input Capacitance		VI		+5		pF
Digital Outputs						
Logic 1 Voltage	I_{OH} = 0.5 mA	VI	3.5			V
Logic 0 Voltage	I_{OL} = 1.6 mA	VI			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages OV_{DD}		IV	3.0		5.0	V
DV_{DD}		IV	4.75	5.0	5.25	V
AV_{DD}		IV	4.75	5.0	5.25	V
Currents AI_{DD}		VI		17	21	mA
DI_{DD}		VI		16	21	mA
Power Dissipation		VI		160	210	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

CLOCK DUTY CYCLE

Ratio of positive clock time (t_{CH}) to total clock period (t_{CLK}) times 100%.

$$\text{Duty Cycle} = \frac{t_{CH}}{t_{CLK}} \text{ X } 100\%$$

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{\text{SINAD} - 1.76}{6.02}$$

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL LINEARITY ERROR (DLE)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL LINEARITY ERROR (ILE)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from –FS through +FS. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

The ratio of the total power of the first 9 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

Figure 1A – Timing Diagram 1

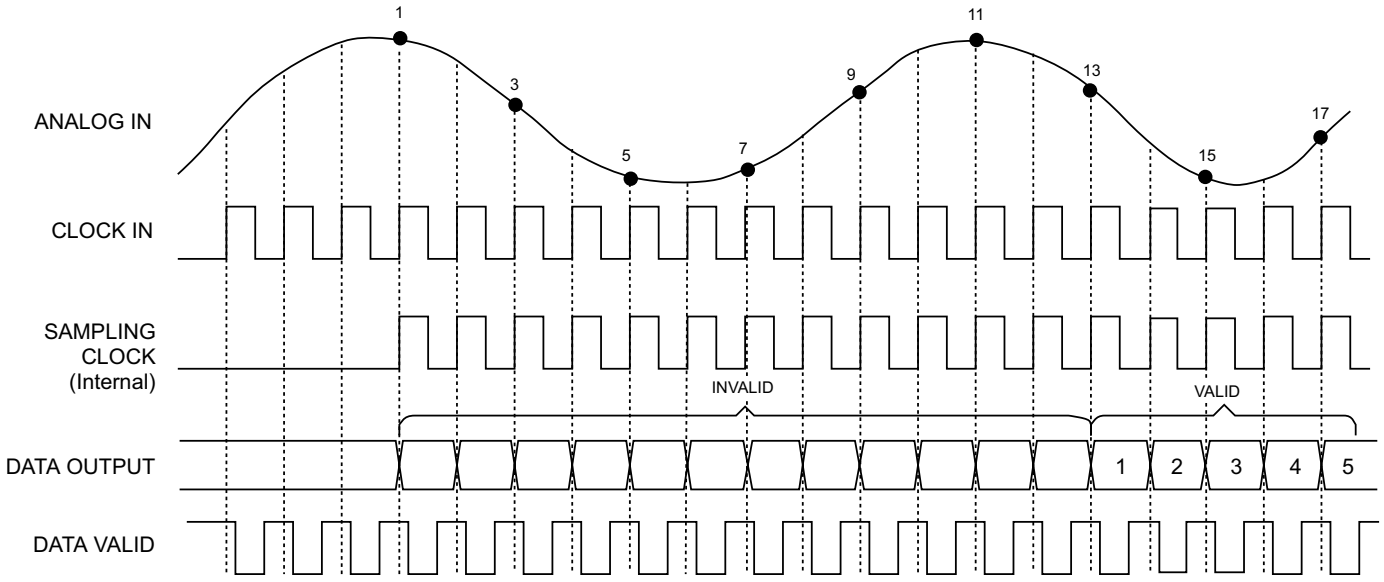


Figure 1B – Timing Diagram 2

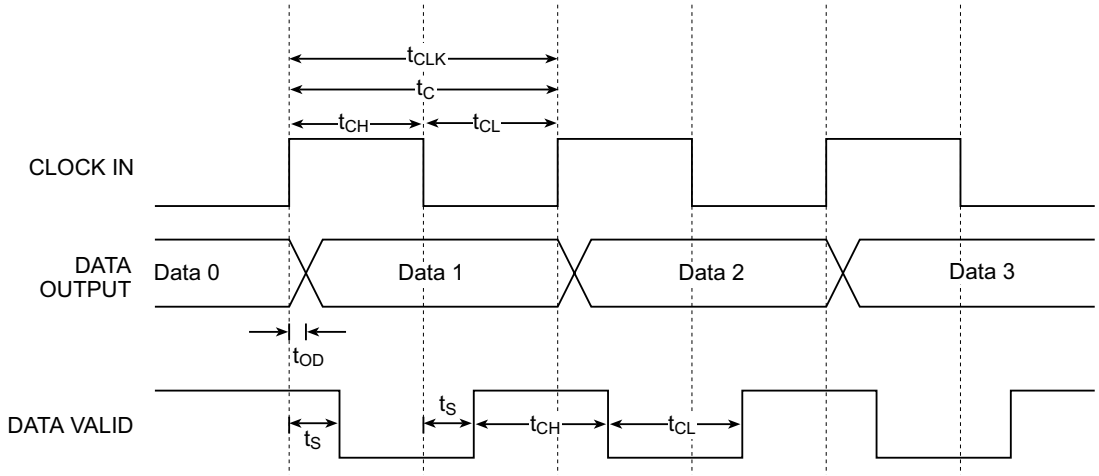
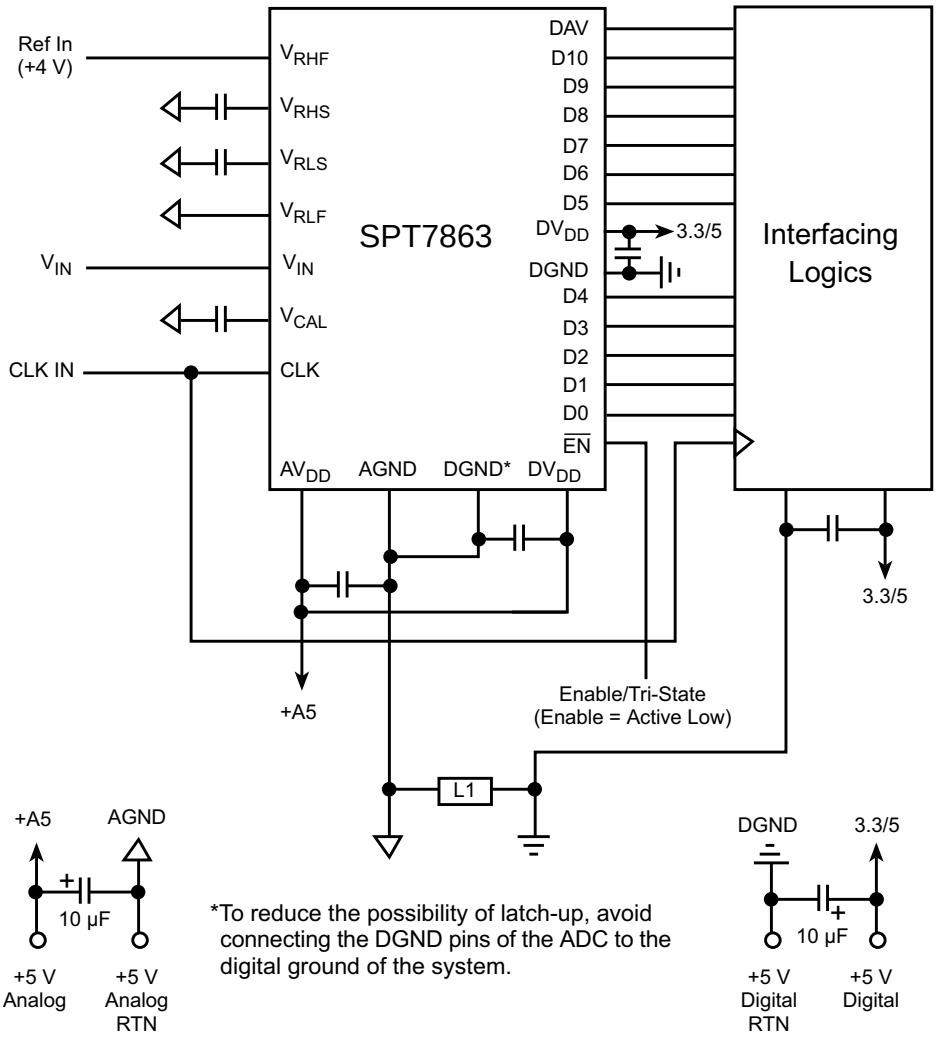


Table I – Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_C	t_{CLK}			ns
Clock Period	t_{CLK}	25			ns
Clock to Output Delay (15 pF Load)	t_{OD}		17		ns
Clock to DAV	t_S		10		ns

Figure 2 – Typical Interface Circuit



NOTES: 1) L1 is to be located as closely to the device as possible.
2) All capacitors are 0.1 µF surface-mount unless otherwise specified.
3) L1 is a 10 µH inductor or a ferrite bead.

TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 2 shows the typical interface requirements when using the SPT7863 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

CADEKA suggests that both the digital and the analog supply voltages on the SPT7863 be derived from a single analog supply as shown in figure 2. A separate digital supply should be used for all interface circuitry. Fairchild suggests using this power supply configuration to prevent a possible latch-up condition on powerup.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains 16 identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator that provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as shown in table II.

Table II – Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16-phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparator's response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter that are not sampling the signal are isolated from the input by transmission gates.

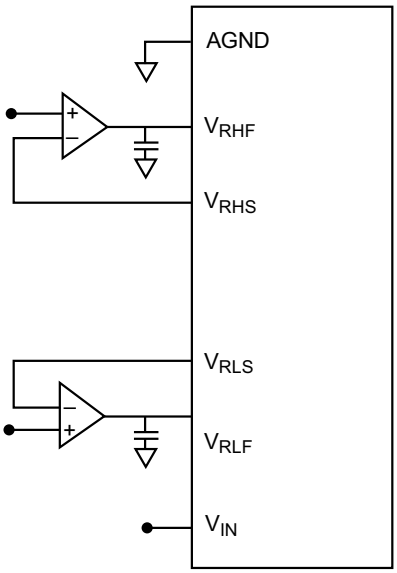
VOLTAGE REFERENCE

The SPT7863 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 3, offset and gain errors of less than ±2 LSB can be obtained.

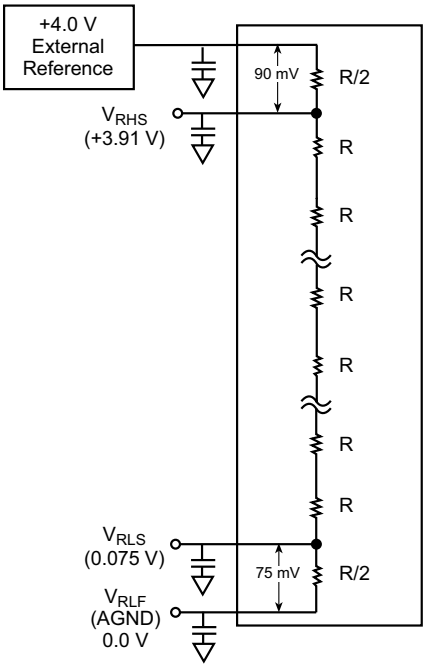
In cases where wider variations in offset and gain can be tolerated, V_{REF} can be tied directly to V_{RHF}, and AGND can be tied directly to V_{RLF} as shown in figure 4. Decouple force and sense lines to AGND with a .01 µF capacitor

Figure 3 – Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 4 – Reference Ladder



R=30 Ω (typ)
All capacitors are 0.01 µF

(chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account.

The reference ladder circuit shown in figure 4 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$$V_{RHF} - V_{RHS} = 2.25\ \%\ \text{of}\ (V_{RHF} - V_{RLF})\ \text{(typical)},$$

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$$V_{RLS} - V_{RLF} = 1.9\ \%\ \text{of}\ (V_{RHF} - V_{RLF})\ \text{(typical)}.$$

Figure 4 shows an example of expected voltage drops for a specific case. V_{REF} of 4.0 V is applied to V_{RHF}, and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V), and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

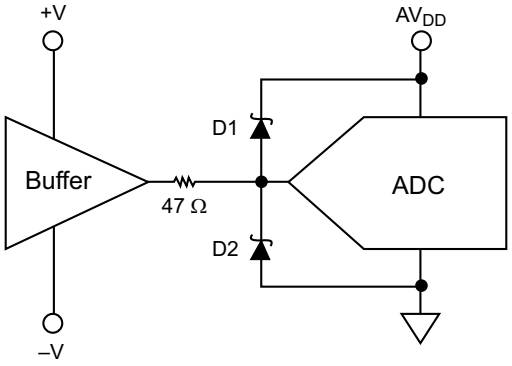
ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7863's extremely low input capacitance of only 5 pF and very high input resistance in excess of 50 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 5.

Figure 5 – Recommended Input Protection Circuit



D1 = D2 = Hewlett-Packard HP5712 or equivalent

CALIBRATION

The SPT7863 uses an auto-calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

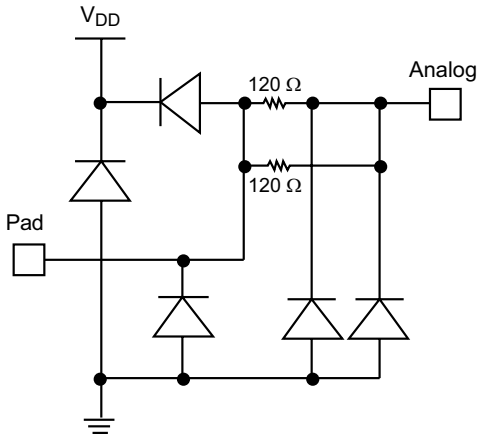
Upon powerup, the SPT7863 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon powerup of 250 µsec (for a 40 MHz clock). Once calibrated, the SPT7863 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7863 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 6. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 6 – On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants that could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7863 is driven from a single-ended TTL-input clock. Because of the aggressive design of the SPT7863, its clock duty cycle ranges from 40% to 51% (see figure 7 – DLE vs Clock Duty Cycle). Operation beyond 51% duty cycle may result in missing codes.

Figure 7 – DLE vs Clock Duty Cycle

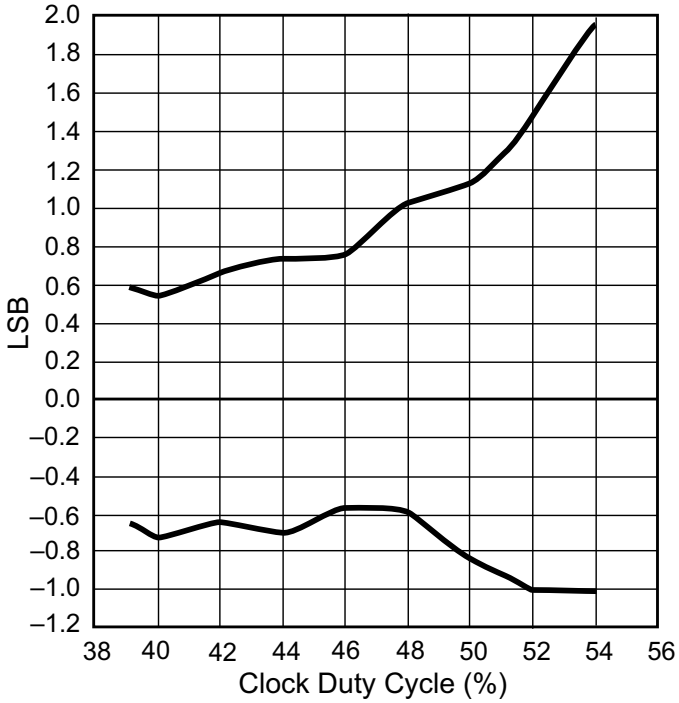
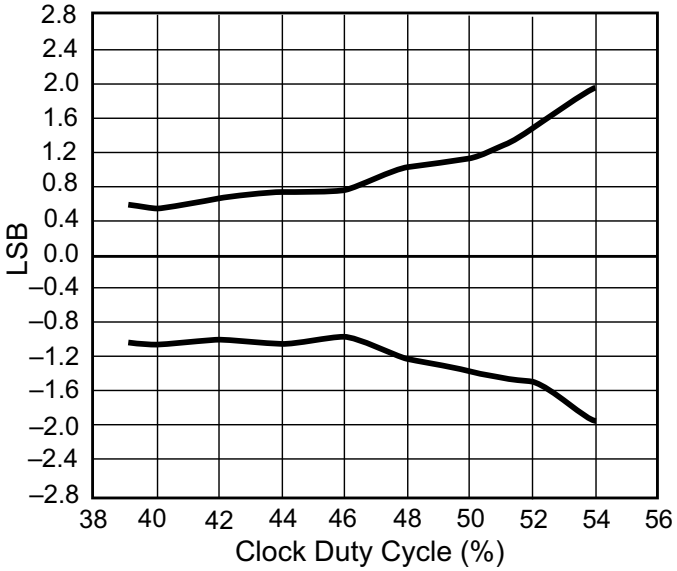


Figure 8 – ILE vs Clock Duty Cycle



DIGITAL OUTPUTS

The digital outputs (D0–D10) are driven by a separate supply (OV_{DD}) ranging from +3 V to +5 V. This feature makes it possible to drive the SPT7863's TTL/CMOS-compatible outputs with the user's logic system supply. The format of the output data (D0–D9) is straight binary. (See table III.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table III – Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
+F.S. + 1/2 LSB	1	1 1 1 1 1 1 1 1 1 1
+F.S. –1/2 LSB	0	1 1 1 1 1 1 1 1 1 Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	0 0 0 0 0 0 0 0 0 Ø
0.0 V	0	0 0 0 0 0 0 0 0 0 0

(Ø indicates the flickering bit between logic 0 and 1.)

OVERRANGE OUTPUT

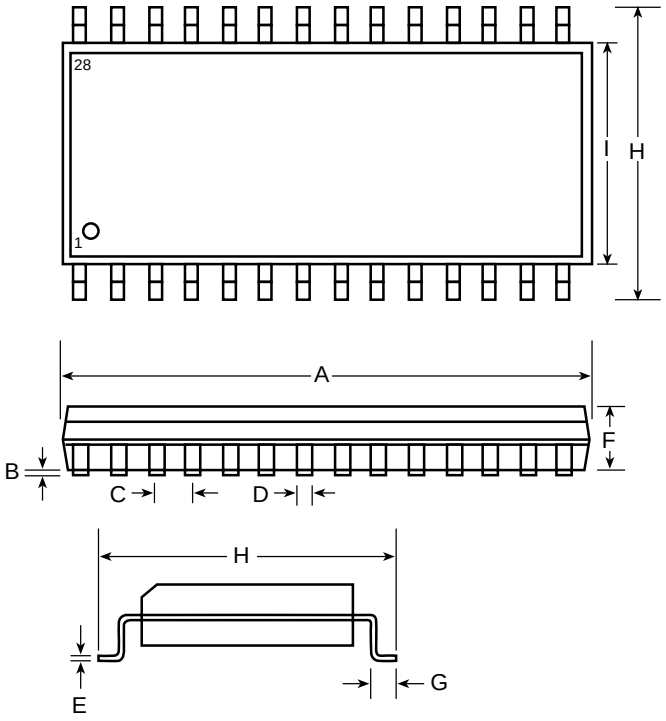
The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full-scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7863 in higher resolution systems.

EVALUATION BOARD

The EB7863 evaluation board is available to aid designers in demonstrating the full performance of the SPT7863. This board includes a reference circuit, clock driver circuit, output data latches, and an on-board reconstruction of the digital data. An application note describing the operation of this board, as well as information on the testing of the SPT7863, is also available. Contact the factory for price and availability.

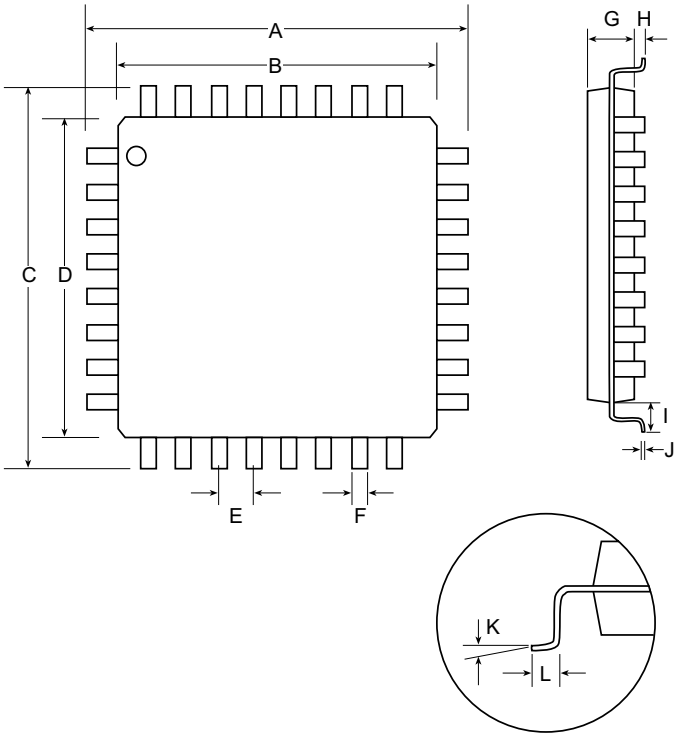
PACKAGE OUTLINES

28-Lead SOIC



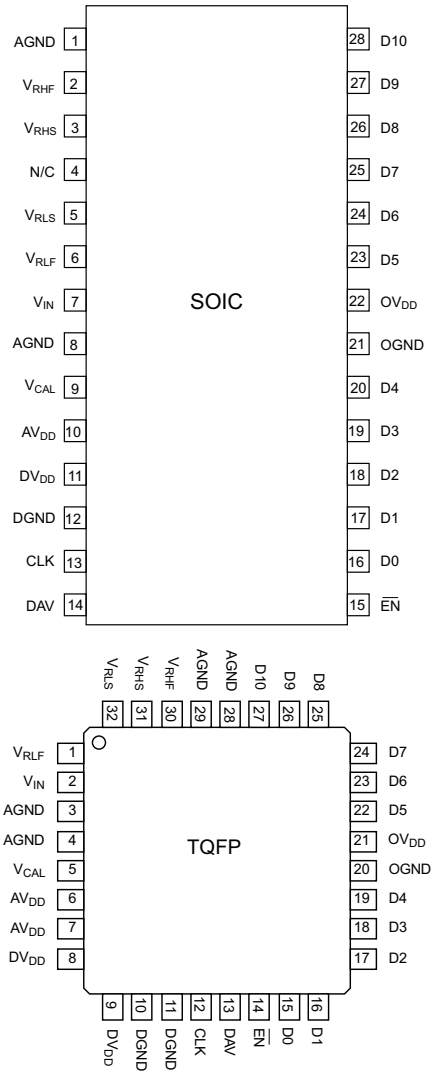
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.699	0.709	17.75	18.01
B	0.005	0.011	0.13	0.28
C	0.050 typ		1.27 typ	
D	0.018 typ		0.46 typ	
E	0.0077	0.0083	0.20	0.21
F	0.090	0.096	2.29	2.44
G	0.031	0.039	0.79	0.99
H	0.396	0.416	10.06	10.57
I	0.286	0.292	7.26	7.42

32-Lead TQFP



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.346	0.362	8.80	9.20
B	0.272	0.280	6.90	7.10
C	0.346	0.362	8.80	9.20
D	0.272	0.280	6.90	7.10
E	0.031 typ		0.80 BSC	
F	0.012	0.016	0.30	0.40
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.037	0.041	0.95	1.05
J		0.007		0.17
K	0°	7°	0°	7°
L	0.020	0.030	0.50	0.75

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} = FS (TTL)
$\overline{EN}$	Output Enable
D0–9	Tri-State Data Output, (D0=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output
OV_{DD}	Digital Output Supply
OGND	Digital Output Ground
N/C	No Connect

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7863SCS	0 to +70 °C	28L SOIC
SPT7863SCT	0 to +70 °C	32L TQFP

For additional information regarding our products, please visit CADEKA at: cadeka.com

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T: 877.663.5452 (toll free)

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