ON Semiconductor®

HDMI Receiver Port Protection and Interface Device

CM2021-02TR

Features

- HDMI 1.3 compliant
- 0.05pF matching capacitance between the TMDS intra-pair
- Level shifting/isolation circuitry
- Provides ESD protection to IEC61000-4-2 Level 4:
  ±8kV contact discharge
  ±15kV air discharge
- Matched 0.5mm trace spacing (TSSOP)
- Simplified layout for HDMI connectors
- Backdrive protection
- RoHS-compliant, lead-free packaging

Applications

- PC
- Consumer electronics
- Displays and digital television

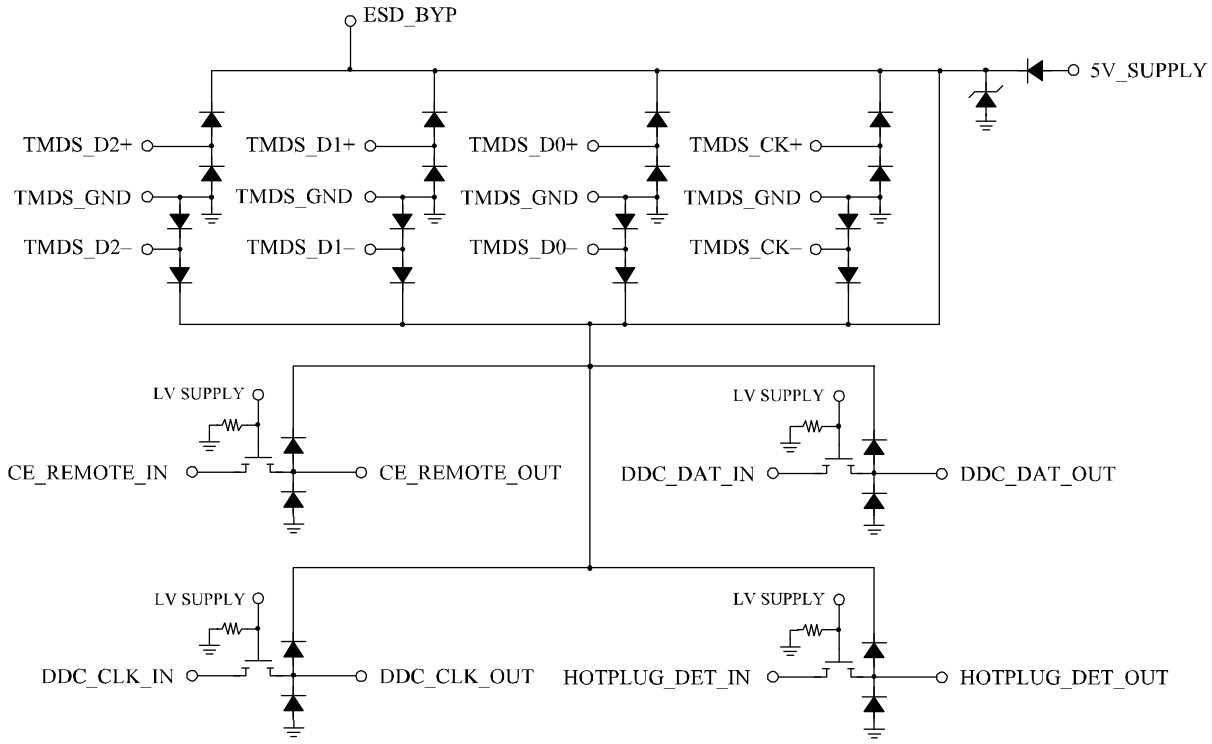
Product Description

The CM2021-02TR HDMI Receiver Port Protection and Interface Device is specifically designed for next generation HDMI Host interface protection.
An integrated package provides all ESD, level shift and backdrive protection for an HDMI port in a single 38-Pin TSSOP package.
The CM2021-02TR part is specifically designed to complement the CM2020 protection part in HDMI transmitters (DVD, STB/OPVR, etc.).

May 2010 – Rev. 3

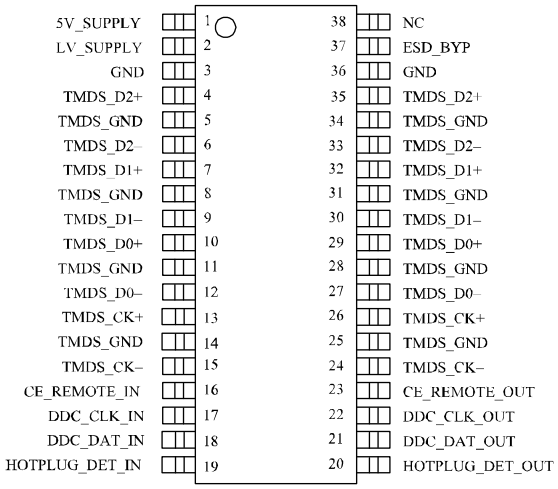
Publication Order Number:
CM2021-02TR/D

Electrical Schematic



PACKAGE / PINOUT DIAGRAM

TOP VIEW



38-PIN TSSOP PACKAGE

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PINS	NAME	ESD Level	DESCRIPTION
4, 35	TMDS_D2+	8kV[2]	TMDS 0.9pF ESD protection.[1]
6, 33	TMDS_D2–	8kV[2]	TMDS 0.9pF ESD protection.[1]
7, 32	TMDS_D1+	8kV[2]	TMDS 0.9pF ESD protection.[1]
9, 30	TMDS_D1–	8kV[2]	TMDS 0.9pF ESD protection.[1]
10, 29	TMDS_D0+	8kV[2]	TMDS 0.9pF ESD protection.[1]
12, 27	TMDS_D0–	8kV[2]	TMDS 0.9pF ESD protection.[1]
13, 26	TMDS_CK+	8kV[2]	TMDS 0.9pF ESD protection.[1]
15, 24	TMDS_CK–	8kV[2]	TMDS 0.9pF ESD protection.[1]
16	CE_REMOTE_IN	2kV[3]	LV_SUPPLY referenced logic level into ASIC.
23	CE_REMOTE_OUT	8kV[2]	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
17	DDC_CLK_IN	2kV[3]	LV_SUPPLY referenced logic level into ASIC.
22	DDC_CLK_OUT	8kV[2]	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
18	DDC_DAT_IN	2kV[3]	LV_SUPPLY referenced logic level into ASIC.
21	DDC_DAT_OUT	8kV[2]	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
19	HOTPLUG_DET_IN	2kV[3]	LV_SUPPLY referenced logic level into ASIC.
20	HOTPLUG_DET_OUT	8kV[2]	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
2	LV_SUPPLY	2kV[3]	Bias for CE / DDC / HOTPLUG level shifters.
1	5V_SUPPLY	2kV[3]	Current source for 5V_OUT.
37	ESD_BYP	2kV[3]	This pin may be connected to a 0.1 F ceramic capacitor, but it is not necessary.
5, 34, 8, 31, 11, 28, 14, 25	TMDS_GND	N/A	TMDS ESD and Parasitic GND return.[4]
3, 36	GND	N/A	Supply GND reference.
38	NC	N/A	No connect.

Note 1: These 2 pins need to be connected together in-line on the PCB.

Note 2: Standard IEC 61000-4-2, $C_{DISCHARGE}$=150pF, $R_{DISCHARGE}$=330Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND=0V, each bypassed with a 0.1μF ceramic capacitor connected to GND.

Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{DISCHARGE}$=100pF, $R_{DISCHARGE}$=1.5kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND=0V, and each bypassed with a 0.1μF ceramic capacitor connected to GND.

Note 4: These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector

Backdrive Protection

Two scenarios below describe what can happen when a powered device is connected to an unpowered device via an HDMI interface, substantiating the need for backdrive protection for this type of interface.

In a classic scenario, a DVD player is connected to a TV via an HDMI interface. If the DVD player is switched off and the TV is left on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player. Typically, the DVD's power supply has some form of bulk supply capacitance associated with it. Because all CMOS logic exhibits a very high impedance on the power rail node when "off," if there is very little parasitic shunt resistance and as little as a few milliamps of "backdrive" current flowing back into the power rail, it is possible over time to charge that bulk supply capacitance to some intermediate level. If this level rises above the power-on-reset (POR) voltage level of some of the integrated circuits in the DVD player, these devices may not reset properly when the DVD player is turned back on.
In a more serious scenario, if any SOC devices are incorporated in the design which have built-in level shifter and DRC diodes for ESD protection, there is even a higher risk for damage. In this case, if there is a pullup resistor (such as with DDC) on the other end of the cable, that resistance will pull the SOC chips "output" up to a high level. This will forward bias the upper ESD diode in the DRC and charge the bulk capacitance in a similar fashion like above. If the current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM2021-02TR is designed to block backdrive current, guaranteeing no more than 5μA on any I/O pin when the I/O pin voltage is greater than the CM2021-02TR supply voltage.

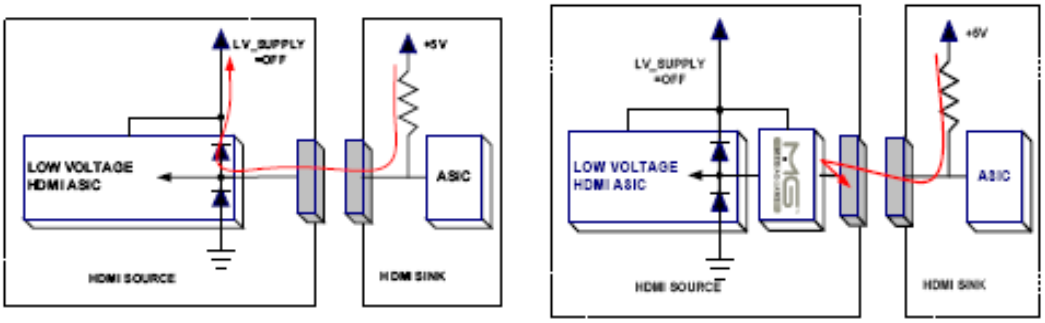


Figure 1. Backdrive Protection Diagram

Ordering Information

PART NUMBERING INFORMATION			
		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking
38	TSSOP-38	CM2021-02TR	CM2021-02TR

Note 1: Parts are shipped in Tape and Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
V_{CC5V}, V_{CCLV}	6.0	V
DC Voltage at any Channel Input	6.0	V
Storage Temperature Range	–65 to +150	ûC

STANDARD (RECOMMENDED) OPERATING CONDITIONS					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
5V_SUPPLY	Operating Supply Voltage	GND	5	5.5	V
LV_SUPPLY	Bias Supply Voltage	1	3.3	5.5	V
	Operating Temperature Range	–40		85	ûC

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC5V}	Operating Supply Current	5V_SUPPLY = 5.0V		110	130	µA
I_{CCLV}	Bias Supply Current	LV_SUPPLY = 3.3V		1	5	µA
I_{OFF}	OFF state leakage current, level shifting NFET	LV_SUPPLY = 0V		0.1	5	µA
$I_{BACKDRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	5V_SUPPLY V_{CH_OUT}; Signal pins: TMDS_[2:0]+/–, TMDS_CK+/–, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT Only		0.1	5	µA
$I_{BACKDRIVE,}$ CEC	Current through CE-REMOTE_OUT when powered down	CE-REMOTE_IN = CE_SUPPLY < CE_REMOTE_OUT		0.1	1	µA
V_{ON}	VOLTAGE drop across level shifting NFET when ON	LV_SUPPLY = 2.5V, V_S = GND, I_{DS} = 3mA	75	95	140	mV
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA, T_A = 25ûC; Note 2	 0.6 0.6	 0.85 0.85	 0.95 0.95	 V V
V_{ESD}	ESD Withstand Voltage (IEC)	Pins 4, 7,10,13, 20, 21, 22, 23, 24, 27, 30, 33; Notes 2 and 3	8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25ûC, I_{PP} = 1A, t_P = 8/20µs; Notes 2 and 4		 11.0 –2.0		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A = 25ûC, I_{PP} = 1A, t_P = 8/20µs; Notes 2 and 4		 1.2 0.9		 Ω Ω
I_{LEAK}	TMDS Channel Leakage Current	T_A = 25ûC; Note 2		0.01	1	µA
$C_{IN,}$ TMDS	TMDS Channel Input Capacitance	5V_SUPPLY = 5.0V, Measured at 1MHz, V_{BIAS}=2.5V; Note 2		0.9	1.2	pF
$\Delta C_{IN,}$ TMDS	TMDS Channel Input Capacitance Matching	5V_SUPPLY = 5.0V, Measured at 1MHz, V_{BIAS}=2.5V; Notes 2 and 5		0.05		pF

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN,}$ DDC	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 5V, Measured at 100KHz, V_{BIAS}=2.5V; Note 2		3.5	4	pF
$C_{IN,}$ CEC	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 5V, Measured at 100KHz, V_{BIAS}=2.5V; Note 2		3.5	4	pF
$C_{IN,}$ HP	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 5V, Measured at 100KHz, V_{BIAS}=2.5V; Note 2		3.5	4	pF

Note 1: Operating characteristics are over standard operating conditions unless otherwise specified.
Note 2: This parameter is guaranteed by design and verified by device characterization.
Note 3: Standard IEC 61000-4-2, $C_{DISCHARGE}$=150pF, $R_{DISCHARGE}$=330Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND=0V, each bypassed with a 0.1µF ceramic capacitor connected to GND.
Note 4: These measurements performed with no external capacitor on ESD_BYP.
Note 5: Intra-pair matching, each TMDS pair (i.e. D+, D–)

Performance Information

Typical Filter Performance (T_A=25ûC, DC Bias=0V, 50 Ohm Environment)

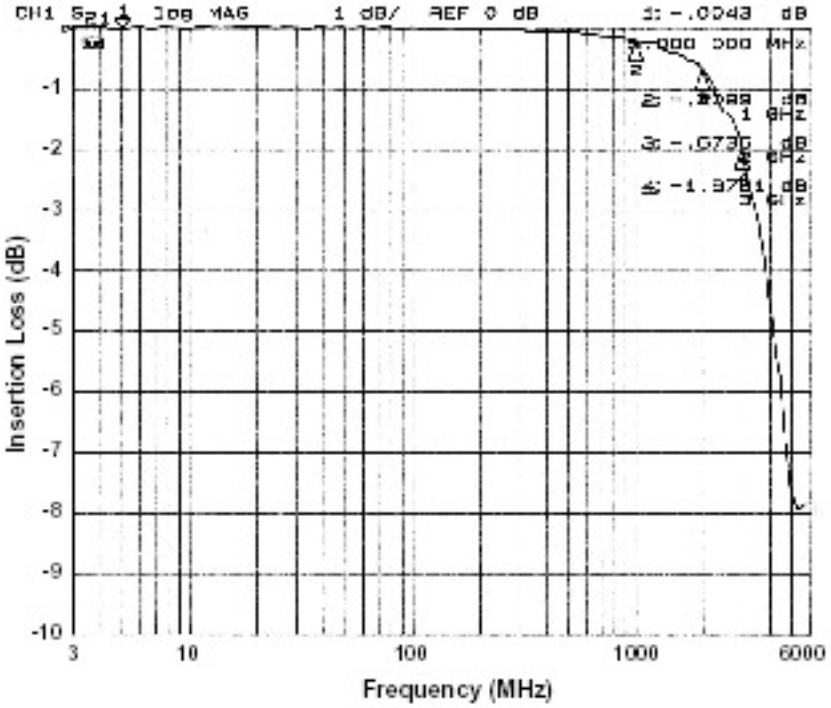
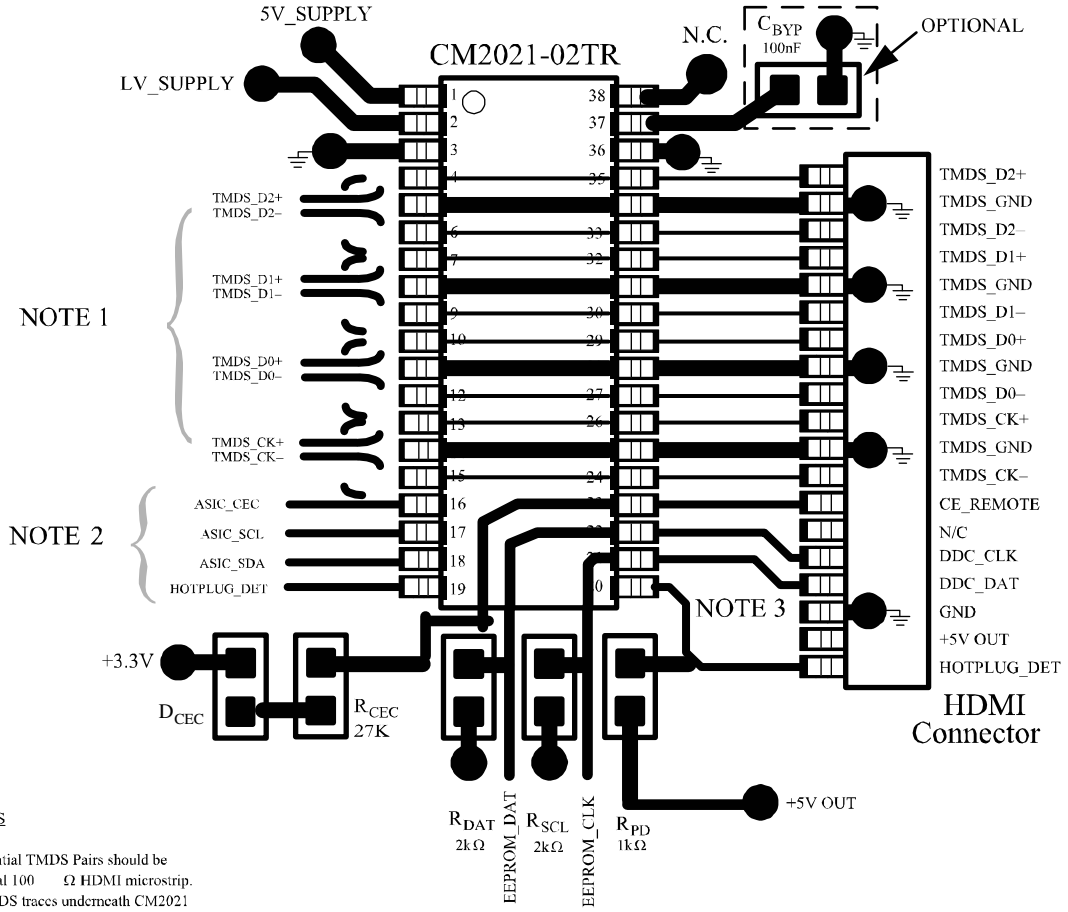


Figure 2. Insertion Loss vs. Frequency (TMDS_D1– to GND)

Application Information



LAYOUT NOTES

NOTE 1) Differential TMDS Pairs should be designed as normal 100 Ω HDMI microstrip. Single Ended TMDS traces underneath CM2021 and between CM2021 and Connector should be tuned to match chip/connector parasitics. (See MediaGuard ™ Application Notes.)

NOTE 2) Level Shifter signals should be biased with a weak pullup to the desired local LV_SUPPLY. If the local ASIC includes sufficient pullups to register a logic high when the CM2021 NFET is "off", then external pullups are not needed.

NOTE 3) Place CM2021 as close to conector as possible, and as with any controlled impedance line avoid ANY silkscreening over TMDS lines.

Figure 3. Typical Application for CM2021-02TR

Application Information

Design Considerations

1. DUT On vs. DUT Off

Many HDMI CTS tests require a power off condition on the System Under Test. Many Dual Rail Clamp (DRC) ESD diode configurations will be forward biased when their VDD rail is lower than the I/O pin bias, thereby exhibiting extremely high apparent capacitance measurements, for example. The *MediaGuard* backdrive isolation circuitry limits this current to less than 10 A, and will help ensure HDMI compliance.

2. EEPROM Configurations

The EDID EEPROM may be connected to either the ASIC LV domain or Connector 5V domain of the CM2021. See the MediaGuard EEPROM Application Note for further circuit connection and layout examples.

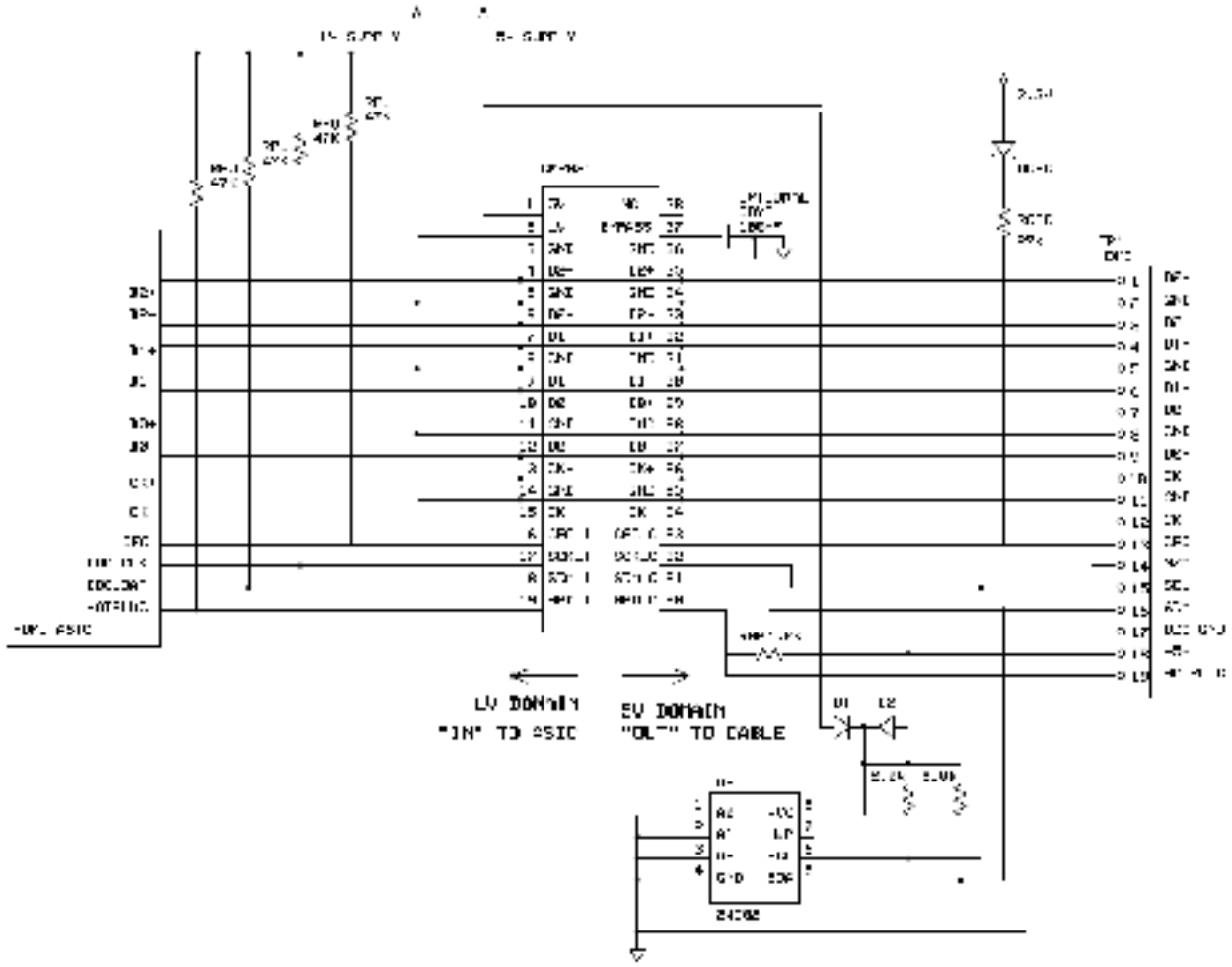


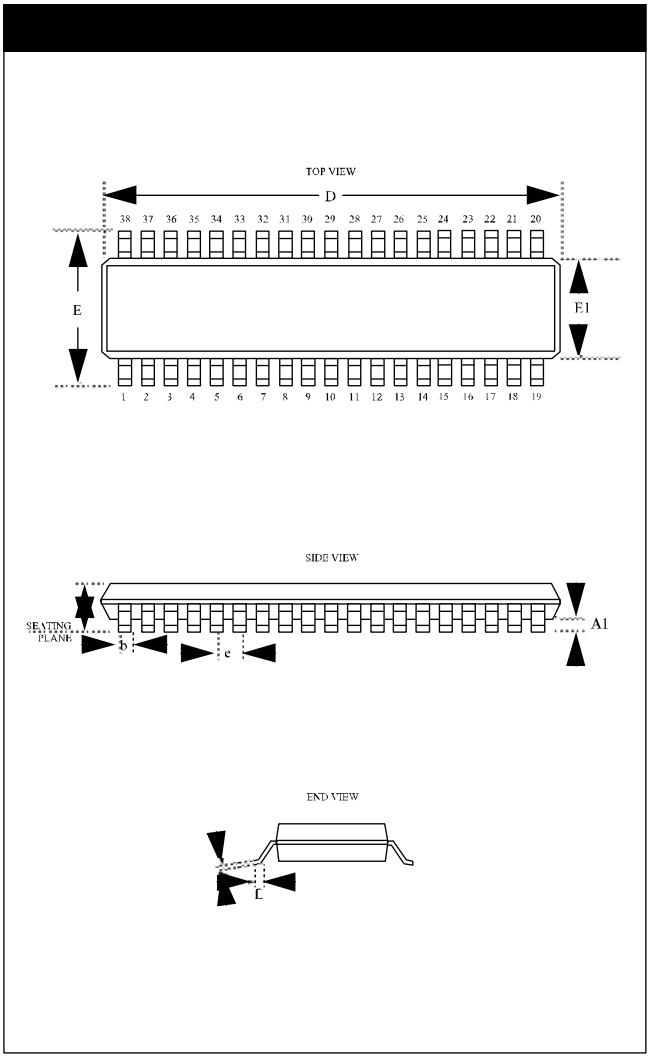
Figure 4. Design Example

Mechanical Details

TSSOP-38 Mechanical Specifications

CM2021-02TR devices are supplied in 38-pin TSSOP packages. Dimensions are presented below.
For complete information on the TSSOP-38, see the California Micro Devices TSSOP Package Information document.

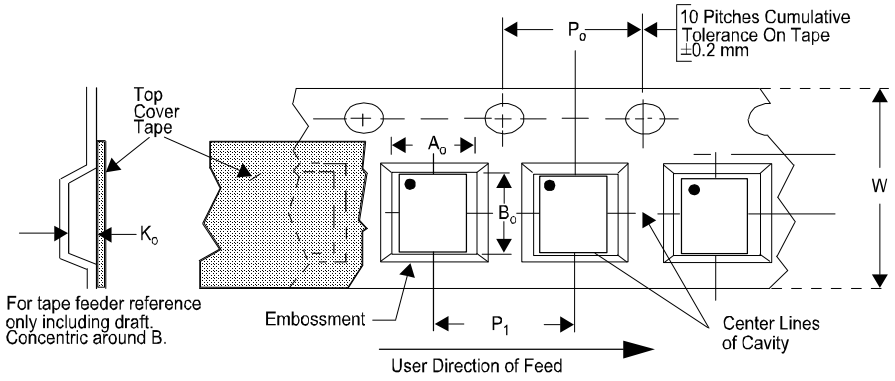
PACKAGE DIMENSIONS				
Package	TSSOP			
JEDEC No.	MO-153 (Variation BD-1)			
Pins	38			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030
# per tape and reel	2500 pieces			
Controlling dimension: millimeters				



Package Dimensions for TSSOP-38

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM2021-02TR	9.70 X 6.40 X 1.20	10.20 X 6.90 X 1.80	16mm	330mm (13")	2500	4mm	12mm



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