PRELIMINARY

CY2545
CY2547

Quad PLL Programmable Spread Spectrum Clock Generator with Serial I²C Interface

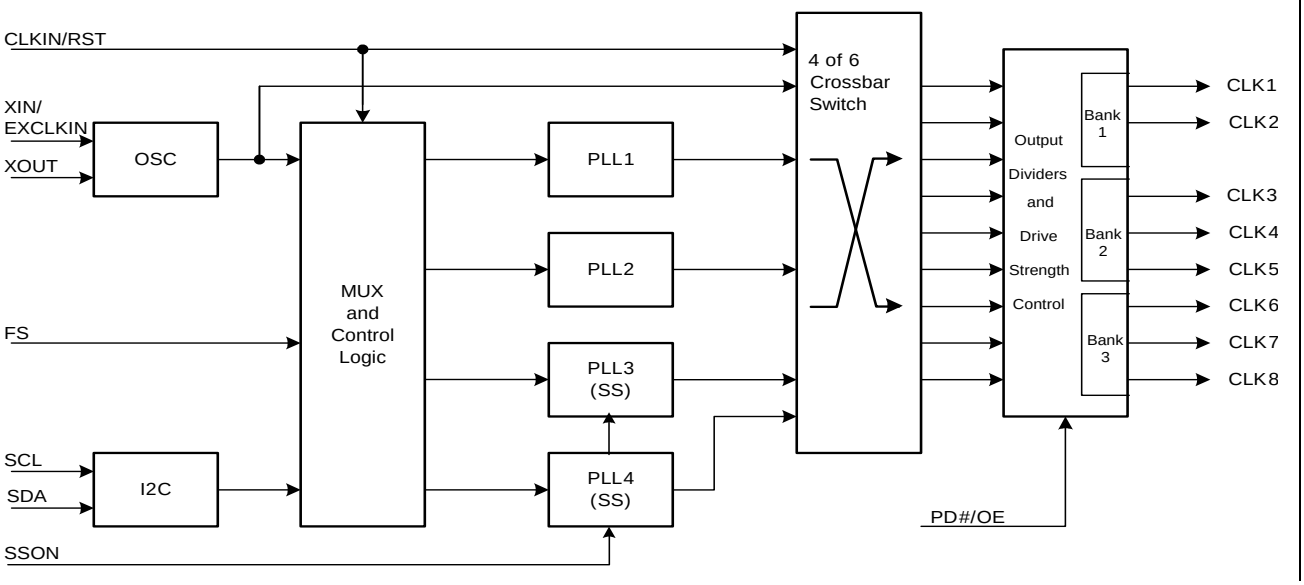
Features

- Four fully integrated phase locked loops (PLLs)
- Input frequency range
  - External crystal: 8 to 48 MHz
  - External reference: 8 to 166 MHz clock
- Wide operating output frequency range
  - 3 to 166 MHz
- Serial programmable over 2-wire I²C interface
- Programmable Spread Spectrum with Center and Down Spread option and Lexmark and Linear modulation profiles
- VDD core voltage options:
  - 2.5V, 3.0V, and 3.3V for CY2545
  - 1.8V for CY2547
- Selectable output clock voltages:
  - 2.5V, 3.0V, and 3.3V for CY2545
  - 1.8V for CY2547
- Power down, output enable, or frequency select features
- Low jitter, high accuracy outputs
- Ability to synthesize nonstandard frequencies with Fractional-N capability
- Up to eight clock outputs with Programmable drive strength
- Glitch-free outputs while frequency switching
- 24-pin QFN package
- Commercial and Industrial temperature ranges

Benefits

- Multiple high performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable EMI reduction using Spread Spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of Zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low power systems

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - CY2545 24 LD QFN

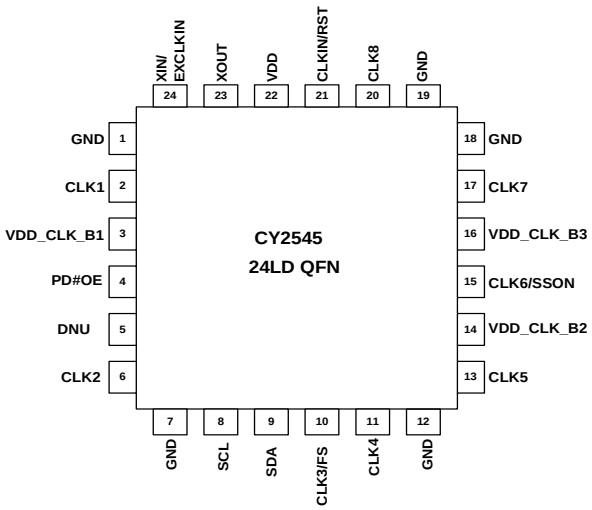


Table 1. Pin Definition - CY2545 24 LD QFN (VDD = 2.5V, 3.0V or 3.3V Supply)

Pin Number	Name	IO	Description
1	GND	Power	Power supply ground
2	CLK1	Output	Programmable output clock, output voltage depends on bank1 voltage
3	VDD_CLK_B1	Power	2.5V/3.0V/3.3V power supply for bank1 (CLK1, CLK2) output
4	PD#/OE	Input	Power down or output enable
5	DNU	DNU	Do not use this pin
6	CLK2	Output	Programmable output clock, output voltage depends on bank1 voltage
7	GND	Power	Power supply ground
8	SCL	Input	Serial data clock
9	SDA	Input/Output	Serial data input/output
10	CLK3/FS	Output/Input	Multifunction programmable pin, CLK3 output or frequency select input pin, FS. Output voltage depends on bank2 voltage
11	CLK4	Output	Programmable output clock, output voltage depends on bank2 voltage
12	GND	Power	Power supply ground
13	CLK5	Output	Programmable output clock, output voltage depends on bank2 voltage
14	VDD_CLK_B2	Power	2.5V/3.0V/3.3V power supply for bank2 (CLK3, CLK4, CLK5) output
15	CLK6/SSON	Output/Input	Multifunction programmable pin, CLK6 output or spread spectrum control input pin, SSON. Output voltage depends on bank3 voltage
16	VDD_CLK_B3	Power	2.5V/3.0V/3.3V Power supply for bank1 (CLK6, CLK7, CLK8) output
17	CLK7	Output	Programmable output clock. output voltage depends on bank3 voltage
18	GND	Power	Power supply ground
19	GND	Power	Power supply ground
20	CLK8	Output	Programmable output clock. output voltage depends on bank3 voltage
21	CLKIN/RST	Input/Input	Multifunction programmable pin. High true reset input or 2.5V/3.0V/3.3V reference clock input. The signal level of CLKIN input must follow VDD power supply on pin 22.

Pin Number	Name	IO	Description
22	VDD	Power	2.5V/3.0V/3.3V Power supply for input and regulator
23	XOUT	Output	Crystal output
24	XIN/EXCLKIN	Input	Crystal input or 1.8V external clock input

Figure 2. Pin Diagram - CY2547 24 LD QFN

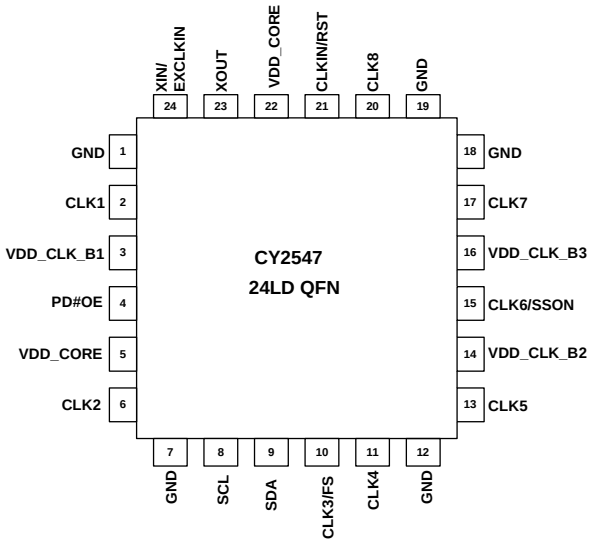


Table 2. Pin Definition - CY2547 24 LD QFN (VDD_CORE = 1.8V Supply)

Pin Number	Name	IO	Description
1	GND	Power	Power supply ground
2	CLK1	Output	Programmable output clock
3	VDD_CLK_B1	Power	1.8V Power supply for bank1 (CLK1, CLK2) output
4	PD#/OE	Input	Power down or output enable
5	VDD_CORE	Power	1.8V Power supply for core
6	CLK2	Output	Programmable output clock
7	GND	Power	Power supply ground
8	SCL	Input	Serial data clock
9	SDA	Input/Output	Serial data input
10	CLK3/FS	Output/Input	Multifunction programmable pin, CLK3 Output or Frequency select input pin, FS
11	CLK4	Output	Programmable output clock
12	GND	Power	Power supply ground
13	CLK5	Output	Programmable output clock
14	VDD_CLK_B2	Power	1.8V Power supply for bank2 (CLK3, CLK4, CLK5) output
15	CLK6/SSON	Output/Input	Multifunction programmable pin, CLK6 Output or spread spectrum control input pin, SSON
16	VDD_CLK_B3	Power	1.8V Power Supply for bank3 (CLK6, CLK7, CLK8) output
17	CLK7	Output	Programmable output clock
18	GND	Power	Power supply ground

Pin Number	Name	IO	Description
19	GND	Power	Power supply ground
20	CLK8	Output	Programmable Output Clock
21	CLKIN/RST	Input/Input	Multifunction programmable pin. High true reset input or 1.8V External low voltage reference clock input
22	VDD_CORE	Power	1.8V Power supply for core
23	XOUT	Output	Crystal output
24	XIN/EXCLKIN	Input	Crystal input or 1.8V external clock input

General Description

Four Configurable PLLs

The CY2545 and CY2547 have four I²C programmable PLLs available to generate output frequencies ranging from 3 to 166 MHz. The advantage of having four PLLs is that a single device generates up to four independent frequencies from a single crystal. Two sets of frequencies for each PLL can be programmed. This enables in system frequency switching using multifunction frequency select pin, FS.

I²C Programming

The CY2545 and CY2547 have a serial I²C interface that programs the configuration memory array to synthesize output frequencies by programmable output divider, spread characteristics, drive strength, and crystal load capacitance. I²C can also be used for in system control of these programmable features.

Input Reference Clocks

The input to the CY2545 and CY2547 is either a crystal or a clock signal. The input frequency range for crystals is 8 MHz to 48 MHz. There is provision for two reference clock inputs, CLKIN and EXCLKIN with frequency range of 8 MHz to 166 MHz. For both devices, when CLKIN signal at pin 21 is used as a reference input, a valid signal at EXCLKIN (as specified in the AC and DC Electrical Specification table), must be present for the devices to operate properly.

Multiple Power Supplies

The CY2545 and CY2547 are designed to operate at internal core supply voltage of 1.8V. In the case of the high voltage part (CY2545), an internal regulator is used to generate 1.8V from the 2.5V/3.0V/3.3V VDD supply voltage at pin 22. For the low voltage part (CY2547), this internal regulator is bypassed and 1.8V at VDD_CORE pin 22 is directly used.

Output Bank Settings

These devices have eight clock outputs grouped in three output driver banks. The Bank 1, Bank 2, and Bank 3 correspond to (CLK1, CLK2), (CLK3, CLK4, CLK5), and (CLK6, CLK7, CLK8), respectively. Separate power supplies are used for each of these banks and they can be any of 2.5V, 3.0V, or 3.3V for CY2545 and 1.8V for CY2547 giving user multiple choice of output clock voltage levels.

Output Source Selection

These devices have eight clock outputs (CLK1 - 8). There are six available clock sources for these outputs. These clock sources are: XIN/EXCLKIN, CLKIN, PLL1, PLL2, PLL3, or PLL4. Output clock source selection is done using four out of six crossbar switch. Thus, any one of these six available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to four independent clock outputs.

Spread Spectrum Control

Two of the four PLLs (PLL3 and PLL4) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK7/SSON). It can be programmed to either center spread range from ±0.125% to ±2.50% or down spread range from –0.25% to –5.0% with Lexmark or Linear profile.

Frequency Select

The device can store two different PLL frequency configurations, output source selection and output divider values for all eight outputs in its nonvolatile memory location. There is a multfunction programmable pin, CLK3/FS which , if programmed as frequency select input, can be used to select between these two arbitrarily programmed settings.

Glitch Free Frequency Switch

When the frequency select pin (FS) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is switched.

Device Reset Function

There is a multifunction CLKIN/RST (pin 21) that can be programmed to use for the device reset function. There are two different programmable modes of operation for this device reset function. First one (called POR like reset), when used brings the device in the default register settings loosing all configuration changes made through the I²C interface. The second (called Clean Start), keeps the I²C programmed values while giving all outputs a simultaneous clean start from its low pull down state.

PD#/OE Mode

PD#/OE (Pin 4) is programable to operate as either power down (PD#) or output enable (OE) mode. PD# is a low true input. If activated it shuts off the entire chip, resulting in minimum device power consumption. Setting this signal high brings the device into operational mode with default register settings.

When this pin is programmed as Output Enable (OE), clock outputs are enabled or disabled using OE (pin 4). Individual clock outputs can be programmed to be sensitive to this OE pin.

Keep Alive Mode

By activating the device in the keep alive mode, power down mode is changed to power saving mode. This disables all PLLs and outputs, but preserves the contents of the volatile registers. Thus, any configuration changes made through the I²C interface are preserved. By deactivating the keep alive mode, I²C memory is not preserved during power down, but power consumption is reduced relative to the keep alive mode.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 3 shows the typical rise and fall times for different drive strength settings.

Table 3. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The device, CY2545/CY2547 can be custom programmed to any desired frequencies and listed features. For customer specific programming and I^2C programmable memory bitmap definitions, please contact your local Cypress Field Application Engineer (FAE) or sales representative.

Serial Programming Interface (SPI) Protocol and Timing

To enhance the flexibility and function of the clock synthesizer, a two signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power up and therefore, use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

The CY2545 and CY2547 use a 2-wire serial interface SDA and SCL that operates up to 400 kbits/s in read or write mode. The SDA and SCL timing and data transfer sequence is shown in Figure 3 on page 8. The basic write serial format is:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit. The basic serial format is illustrated in Figure 4 on page 8.

Device Address

The device serial interface address is 69H. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

Data Valid

Data is valid when the clock is HIGH, and is only transitioned when the clock is LOW, as illustrated in Figure 5 on page 9.

Data Frame

A start and stop sequence indicates every new data frame, as illustrated in Figure 6 on page 9.

Start Sequence - The start frame is indicated by SDA going LOW when SCL is HIGH. Every time a start signal is supplied, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

Stop Sequence - The stop frame is indicated by SDA going HIGH when SCL is HIGH. A stop frame frees the bus to go to another part on the same bus or to another random register address.

Acknowledge Pulse

During write mode the CY2545/CY2547 responds with an acknowledge pulse after every eight bits. Do this by pulling the SDA line LOW during the N*9th clock cycle as illustrated in Figure 7 on page 9 (N = the number of bytes transmitted). During read mode, the master generates the acknowledge pulse after reading the data packet.

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (ack = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (ack = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write multiple bytes at a time, the master does not end the write sequence with a STOP condition; instead, the master sends multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, the same as after the first byte, and accepts data until the STOP condition responds to the acknowledge bit. When receiving multiple bytes, the CY2545 and CY2547 internally increment the register address.

Read Operations

Read operations are initiated the same way as write operations except that the R/W bit of the slave address is set to ‘1’ (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY2545 and CY2547 have an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word ‘n’, then a current address read operation returns the value stored in location ‘n+1’. When the CY2545/CY2547 receive the slave address with the R/W bit set to a ‘1’, the CY2545/CY2547 issue an acknowledge and transmit the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the CY2545/CY2547 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is done by sending the address to the CY2545/CY2547 as part of a write operation. After sending the word address, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to ‘1’. The CY2545/CY2547 then issue an acknowledge and transmit the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the CY2545/CY2547 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmitting the first 8-bit data word. This action increments the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master serially reads the entire contents of the slave device memory. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

Figure 3. Data Transfer Sequence on the Serial Bus

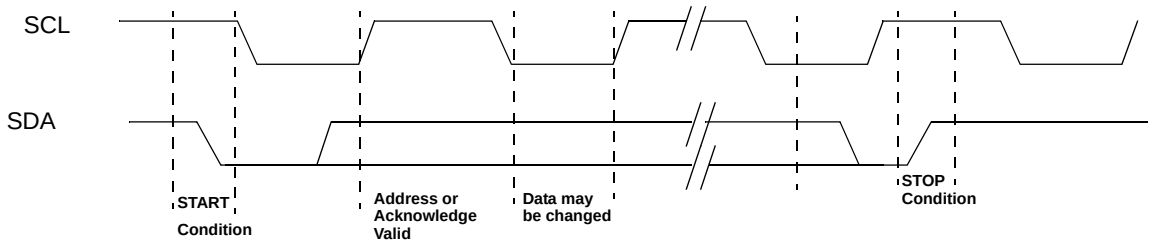


Figure 4. Data Frame Architecture

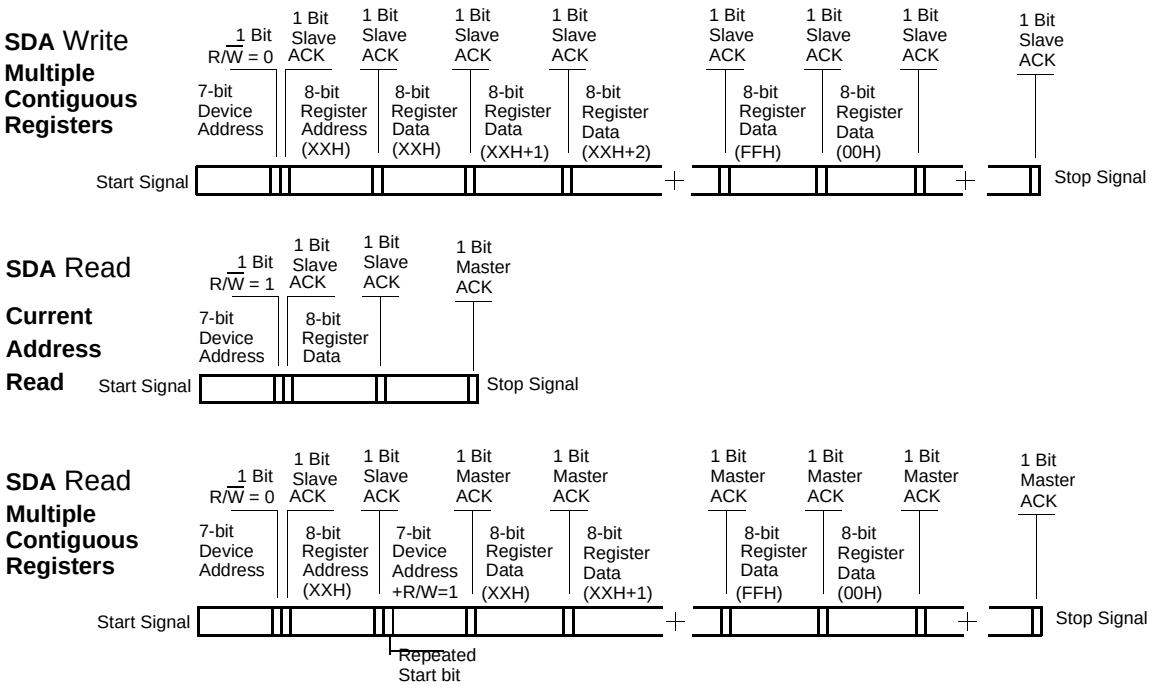
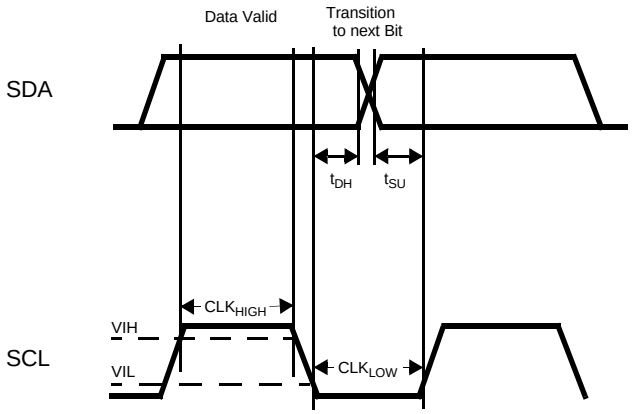


Figure 5. Data Valid and Data Transition Periods



Serial Programming Interface Timing

Figure 6. .Start and Stop Frame

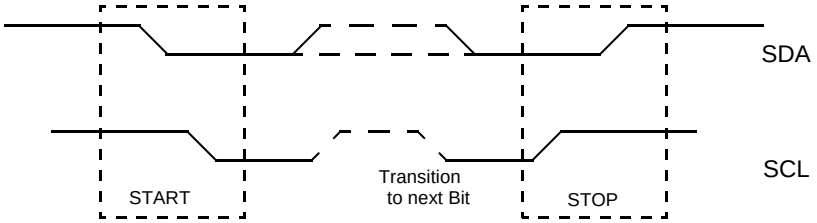
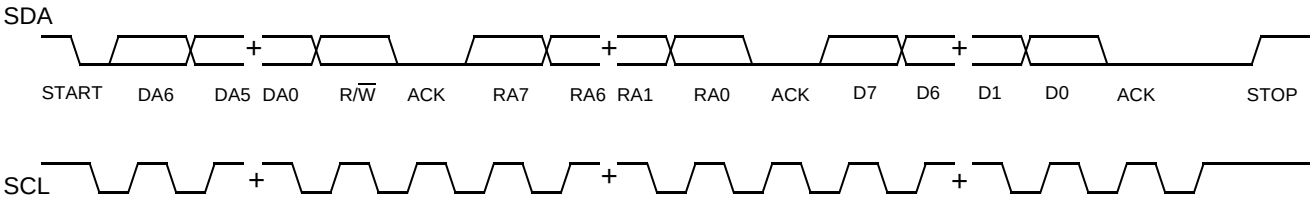


Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Serial Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCL}	Frequency of SCL	–	400	kHz
	Start Mode Time from SDA LOW to SCL LOW	0.6	–	µs
CLK_{LOW}	SCL LOW Period	1.3	–	µs
CLK_{HIGH}	SCL HIGH Period	0.6	–	µs
t_{SU}	Data Transition to SCL HIGH	100	–	ns
t_{DH}	Data Hold (SCL LOW to data transition)	0	–	ns
	Rise Time of SCL and SDA	–	300	ns
	Fall Time of SCL and SDA	–	300	ns
	Stop Mode Time from SCL HIGH to SDA HIGH	0.6	–	µs
	Stop Mode to Start Mode	1.3	–	µs

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage for CY2545		–0.5	4.5	V
V_{DD_CORE}	Core supply voltage for CY2547		–0.5	2.6	V
$V_{DD\_CLK\_BX}$	Output bank supply voltage for CY2545		–0.5	4.5	V
	Output bank supply voltage for CY2547		–0.5	2.6	V
V_{IN}	Input voltage for CY2545	Relative to V_{SS}	–0.5	3.6	V
V_{IN}	Input voltage for CY2547	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature and storage	Nonfunctional	–65	+150	°C
ESD_{HBM}	ESD protection (Human Body Model)	MIL-STD-883, Method 3015	2000		Volts
UL-94	Flammability rating	V-0 @1/8 in.		10	ppm
MSL	Moisture sensitivity level		3		

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	VDD operating voltage, 3.3V for CY2545	3.00	3.3	3.60	V
V_{DD}	VDD operating voltage, 3.0V for CY2545	2.70	3.0	3.30	V
V_{DD}	VDD operating voltage, 2.5V for CY2545	2.25	2.5	2.75	V
V_{DD_CORE}	VDD_CORE operating at 1.8V for CY2547	1.65	1.8	1.95	V
$V_{DD\_CLK\_BX}$	Output driver voltage for bank 1, 2 and 3 operating at 3.3V (CY2545)	3.00	3.3	3.60	V
$V_{DD\_CLK\_BX}$	Output driver voltage for bank 1, 2 and 3 operating at 3.0V (CY2545)	2.70	3.0	3.30	V
$V_{DD\_CLK\_BX}$	Output driver voltage for bank 1, 2 and 3 operating at 2.5V (CY2545)	2.25	2.5	2.75	V
$V_{DD\_CLK\_BX}$	Output driver voltage for bank 1, 2 and 3 operating at 1.8V (CY2547)	1.65	1.8	1.95	V
T_{AC}	Commercial ambient temperature	0	–	+70	°C
T_{AI}	Industrial ambient temperature	–40	--	+85	°C
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power up time for all V_{DDS} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low voltage	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output high voltage	I_{OH} = –2 mA, drive strength = [00]	V_{DD_CLK} – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{OLSD}	Output low voltage, SDA	I_{OL} = 4 mA	–	–	0.4	V
V_{IL1}	Input low voltage, PD#/OE, RST, FS, and SSON for CY2545		–	–	0.2*V_{DD}	V
V_{IL2}	Input low voltage, PD#/OE, RST, FS, and SSON for CY2547		–	–	0.2* V_{DD_CORE}	V
V_{IL3}	Input low voltage, CLKIN for CY2545		–	–	0.1*V_{DD}	V
V_{IL4}	Input low voltage, EXCLKIN for CY2545		–	–	0.18	V
V_{IL5}	Input low voltage, CLKIN, EXCLKIN for CY2547		–	–	0.1* V_{DD_CORE}	V
V_{IH1}	Input high voltage, PD#/OE, RST, FS, and SSON for CY2545		0.8*V_{DD}	–	–	V
V_{IH2}	Input high voltage, PD#/OE, RST, FS, and SSON for CY2547		0.8* V_{DD_CORE}	–	–	V
V_{IH3}	Input high voltage, CLKIN for CY2545		0.9*V_{DD}	–	–	V
V_{IH4}	Input high voltage, EXCLKIN for CY2545		1.62	–	–	V
V_{IH5}	Input high voltage, CLKIN, EXCLKIN for CY2547		0.9* V_{DD_CORE}	–	–	V
I_{ILPD}	Input low current, PD#/OE	V_{IN} = V_{SS}	–	–	10	µA
I_{IHPD}	Input high current, PD#/OE	V_{IN} = V_{DD}	–	–	10	µA
I_{ILSR}	Input low current, SSON# and FS pins	V_{IN} = V_{SS} (Internal pull dn = 160k typ)	–	–	10	µA
I_{IHSR}	Input high current, SSON# and FS pins	V_{IN} = V_{DD} (Internal pull dn = 160k typ)	14	–	36	µA
R_{DN}	Pull down resistor of (CLK1-CLK8) when off, SSON# and FS pins		100	160	250	kΩ
I_{DD}[1,2]	Supply current for CY2547	PD# = High, No load	–	20	–	mA
	Supply current for CY2545	PD# = High, No load	–	22	–	mA
I_{DDS}[1,2]	Standby current	PD# = Low, No load, with I^2C circuit in NOT Keep Alive Mode	–	3	–	µA
I_{PD}[1,2]	Power down current	PD# = Low, No load, with I^2C circuit in Keep Alive Mode	–	–	1	mA
C_{IN}	Input capacitance	SSON, PD#/OE or FS inputs	–		7	pF

AC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{IN} (crystal)	Crystal frequency, XIN		8	–	48	MHz
F_{IN} (clock)	Input clock frequency (CLKIN or EXCLKIN)		8	–	166	MHz
F_{CLK}	Output clock frequency		3	–	166	MHz
DC	Output duty cycle, all clocks except Ref Out	Duty Cycle is defined in Figure 9 on page 14; t_1/t_2, 50% of V_{DD}	45	50	55	%
DC	Ref out duty cycle	Ref In Min 45%, Max 55%	40	–	60	%
T_{RF1}[1]	Output rise/fall time	Output clocks, measured from 20% to 80% of V_{DD_CLK} CL = 15 pF, Drive [0,0]	–	6.8	–	ns
T_{RF2}[1]	Output rise/fall time	Output clocks, measured from 20% to 80% of V_{DD_CLK} CL = 15 pF, Drive [0,1]	–	3.4	–	ns
T_{RF3}[1]	Output rise/fall time	Output clocks, measured from 20% to 80% of V_{DD_CLK} CL = 15 pF, Drive [1,0]	–	2.0	–	ns
T_{RF4}[1]	Output rise/fall time	Output clocks, measured from 20% to 80% of V_{DD_CLK} CL = 15 pF, Drive [1,1]	–	1.0	–	ns
T_{CCJ1}[1,2]	Cycle-to-cycle jitter max (Pk-Pk)	Configuration dependent. See Table 4	–	–	–	ps
T_{10}	PLL Lock time	Measured from 90% of the applied power supply level	–	1	3	ms

Table 4. Configuration Example for C-C Jitter

Ref. Freq. (MHz)	CLK1 Output		CLK2 Output		CLK3 Output		CLK4 Output		CLK5 Output	
	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)
14.3181	8.0	134	166	103	48	92	74.25	81	Not Used	
19.2	74.25	99	166	94	8	91	27	110	48	75
27	48	67	27	109	166	103	74.25	97	Not Used	
48	48	93	27	123	166	137	166	138	8	103

Recommended Crystal Specification for SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum frequency	8	14	28	MHz
Fmax	Maximum frequency	14	28	48	MHz
R1(max)	Maximum motional resistance (ESR)	135	50	30	Ω
C0(max)	Maximum shunt capacitance	4	4	2	pF
CL(max)	Maximum parallel load capacitance	18	14	12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

Recommended Crystal Specification for Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum frequency	8	14	24	MHz
Fmax	Maximum frequency	14	24	32	MHz
R1(max)	Maximum motional resistance (ESR)	90	50	30	Ω
C0(max)	Maximum shunt capacitance	7	7	7	pF
CL(max)	Maximum parallel load capacitance	18	12	12	pF

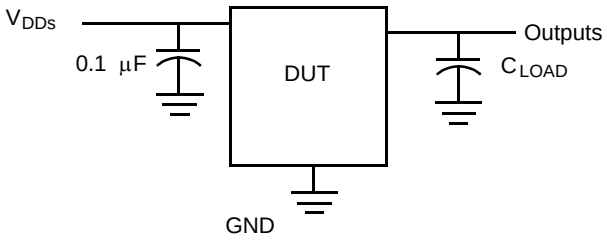
Notes
1. Guaranteed by design but not 100% tested.
2. Configuration dependent.

Recommended Crystal Specification for Thru-Hole Package (continued)

Parameter	Description	Range 1	Range 2	Range 3	Unit
DL(max)	Maximum crystal drive level	1000	1000	1000	µW

Test and Measurement Setup

Figure 8. Test and Measurement Setup



Voltage and Timing Definitions

Figure 9. Duty Cycle Definition

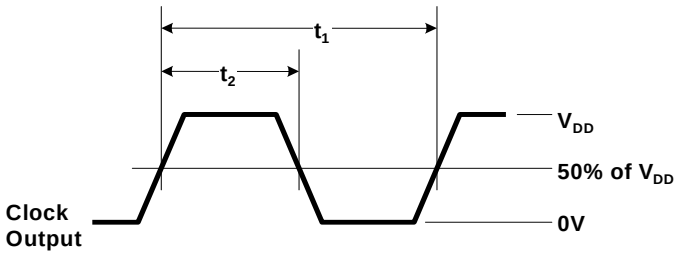
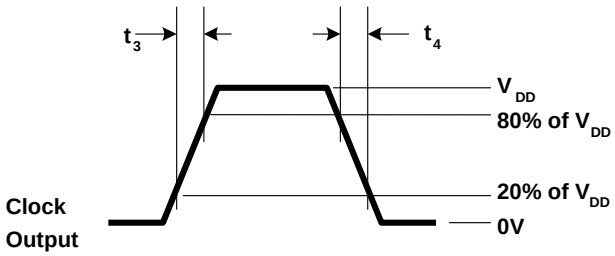


Figure 10. ER = (0.6 x V_{DD}) /t_3, EF = (0.6 x V_{DD}) /t_4



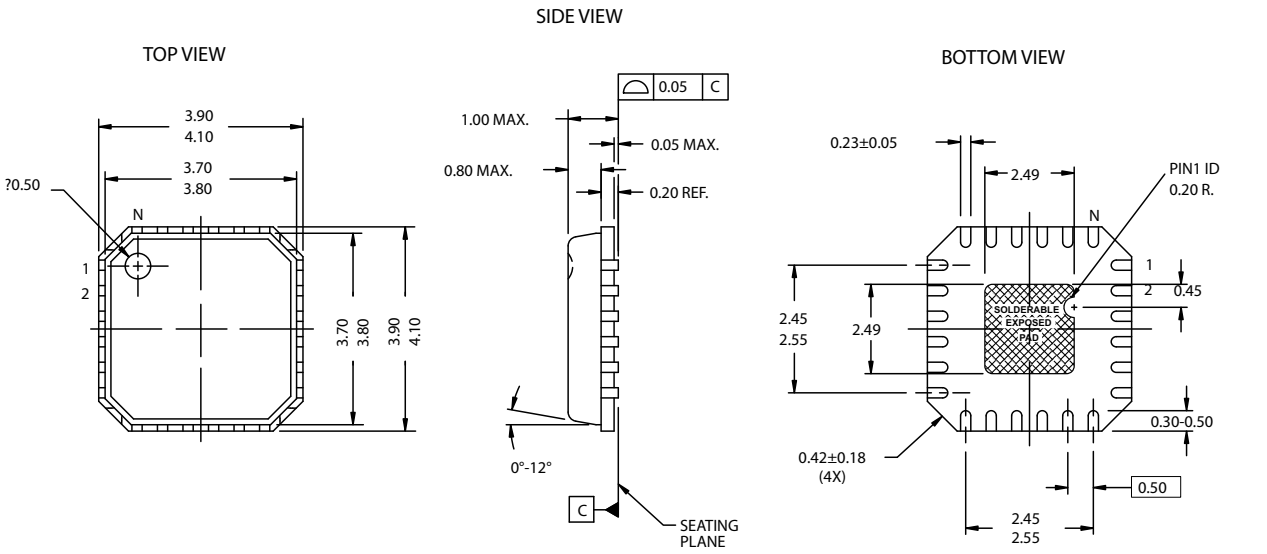
Ordering Information

Part Number[3]	Type	VDD(V)	Production Flow
Pb-free			
CY2545Cxxx	24-pin QFN	High Core Voltage, 2.5V, 3.0V or 3.3V	Commercial, 0°C to 70°C
CY2545CxxxT	24-pin QFN Tape & Reel	High Core Voltage, 2.5V, 3.0V or 3.3V	Commercial, 0°C to 70°C
CY2547Cxxx	24-pin QFN	Low Core Voltage, 1.8V	Commercial, 0°C to 70°C
CY2547CxxxT	24-pin QFN Tape & Reel	Low Core Voltage, 1.8V	Commercial, 0°C to 70°C
CY2545Ixxx	24-pin QFN	High Core Voltage, 2.5V, 3.0V or 3.3V	Industrial, –40°C to 85°C
CY2545IxxxT	24-pin QFN Tape & Reel	High Core Voltage, 2.5V, 3.0V or 3.3V	Industrial, –40°C to 85°C
CY2547Ixxx	24-pin QFN	Low Core Voltage, 1.8V	Industrial, –40°C to 85°C
CY2547IxxxT	24-pin QFN Tape & Reel	Low Core Voltage, 1.8V	Industrial, –40°C to 85°C

Note
3. xxx indicates Factory Programmable and are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Drawing and Dimensions

Figure 11. 24-LD QFN 4x4 mm (Subcon Punch Type Pkg with 2.49x2.49 EPAD) LF24A/LY24A



NOTES:

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.042g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF24A	STANDARD
LY24A	LEAD FREE

51-85203-*A

Document History Page

Document Title: CY2545/CY2547 Quad PLL Programmable Spread Spectrum Clock Generator with Serial I²C Interface Document Number: 001-13196				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	870780	See ECN	RGL/AESA	New Data Sheet