GENERAL DESCRIPTION

bw1254x is a CMOS 14bit analog-to-digital converter (ADC). It converts the analog input signal into 14bit binary digital codes at a maximum sampling rate of 10MHz.

The device is a monolithic ADC with an on-chip, high-performance, sample-and-hold Amplifier (SHA) and current reference and voltage reference. The structure allows both differential and single-ended input.

TYPICAL APPLICATIONS

— Imaging (Copiers, Scanners, Cameras)

— Medical Instruments

— Digital Communication Systems

— uADSL System

FEATURES

— Resolution : 14bit

— Maximum Conversion Rate : 10MHz

— Package Type : 48TSSOP

— Power Supply : 3.3V

— Power Consumption : 120mW (typical)

— Reference Voltage : Internal reference or 2V, 1V (dual reference)

— Input Range : 0.5V ~ 2.5V ($2.0V_{P-P}$)

— Differential Linearity Error : ±0.7 LSB

— Integral Linearity Error : ±1.5 LSB

— Signal to Noise & Distortion Ratio : 72dB

— Total Harmonic Distortion : 80dB

— Out of Range Indicator

— Digital Output : CMOS Level

— Operating Temperature Range : 0°C ~ 70°C
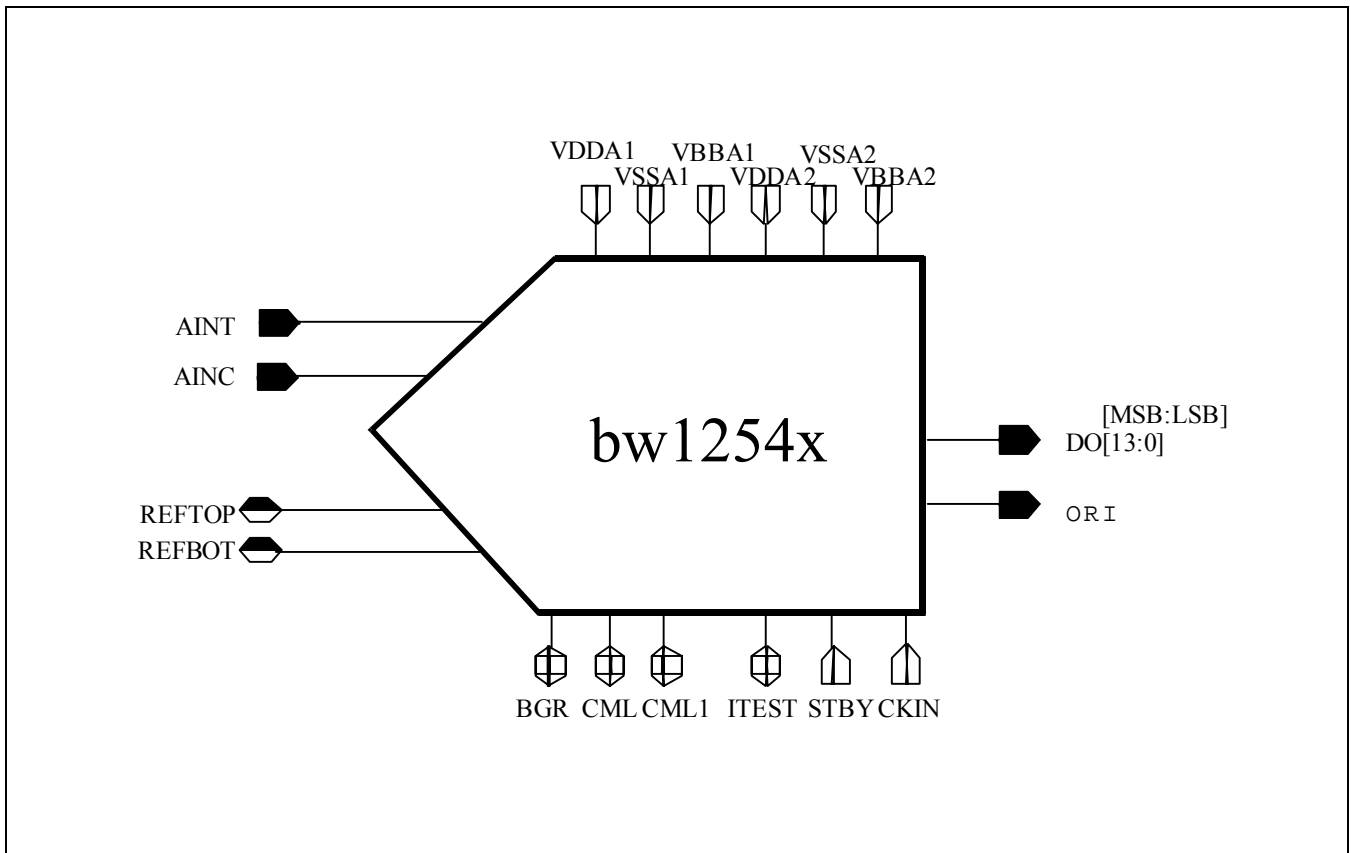
FUNCTIONAL BLOCK DIAGRAM

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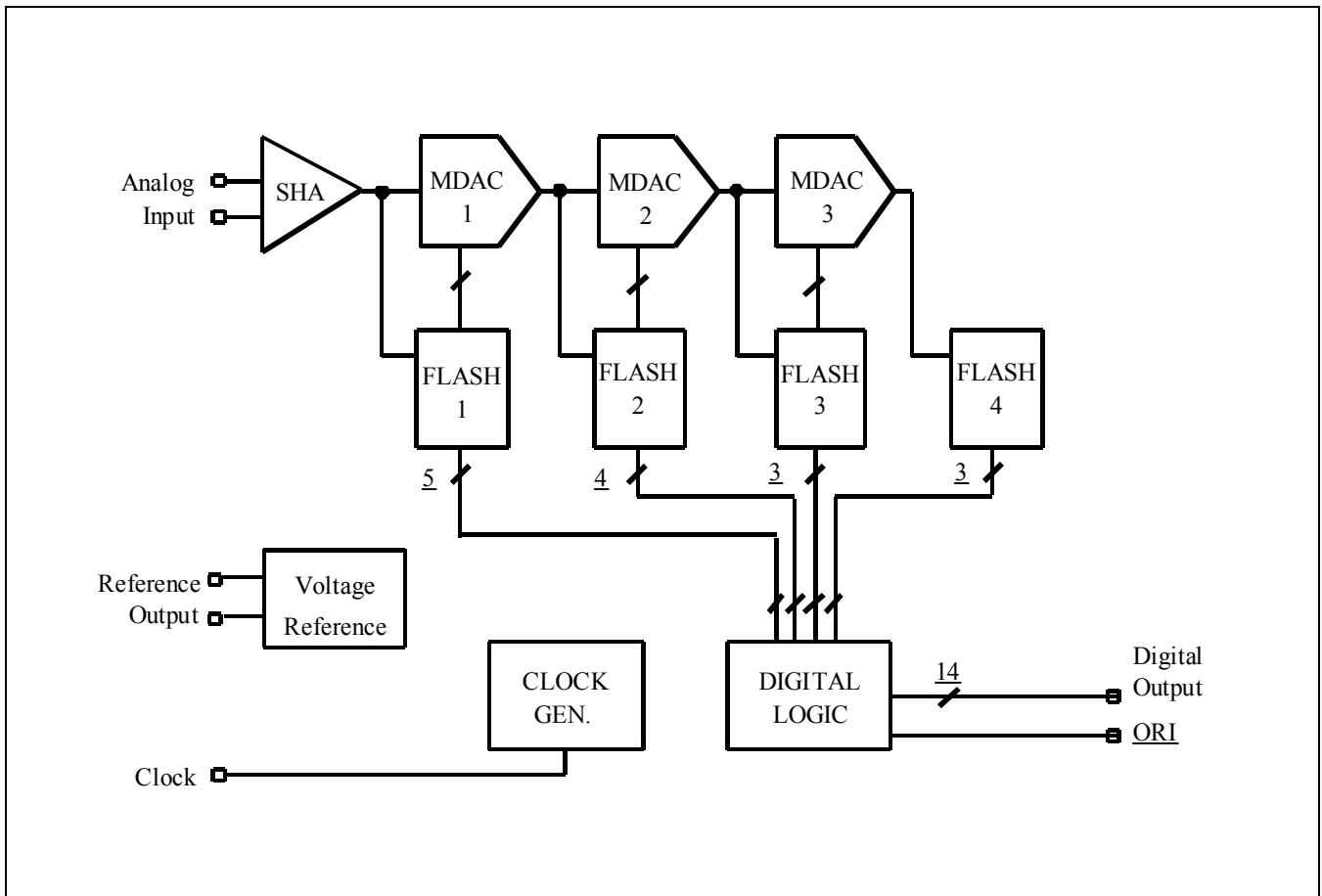
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
REFTOP	AB	piar10_bb	Reference Top Output/Force (2.0V)
REFBOT	AB	piar10_bb	Reference Bottom Output/Force (1.0V)
BGR	AB	piar10_bb	BGR output (1.23V)
CML	AB	piar10_bb	Internal Bias
CML1	AB	piar10_bb	Internal Bias
VDDA1	AP	vdda	Analog Power (3.3V)
VBBA1	AG	vbba	Analog Sub Bias
VSSA1	AG	vssa	Analog Ground
AINT	AI	piar10_bb	Analog Input + (Input Range : 1.0V ~ 2.0V)
AINC	AI	piar10_bb	Analog Input - (Input Range : 1.0V ~ 2.0V)
ITEST	AB	pia_bb	open=use internal bias point
STBY	DI	picc_bb	VDD=power saving (standby), GND=normal
CKIN	DI	picc_bb	Sampling Clock Input
D[13:0]	DO	poa_bb	Digital Output
ORI	DO	poa_bb	Out of Range Indicator
VBBA2	DG	vbba	Digital Sub Bias
VSSA2	DG	vssd	Digital GND
VDDA2	DP	vddd	Digital Power (3.3V)

I/O Type Abbr.

— AI: Analog Input

— DI: Digital Input

— AO: Analog Output

— DO: Digital Output

— AP: Analog Power

— AG: Analog Ground

— DP: Digital Power

— DG: Digital Ground

— AB: Analog Bidirectional

— DB: Digital Bidirectional

CORE CONFIGURATION

VDDA1　VBBA1　VSSA2
VSSA1　VDDA2　VBBA2

AINT

AINC

bw1254x

[MSB:LSB]
DO[13:0]

ORI

REFTOP
REFBOT

BGR CML CML1 ITEST STBY CKIN

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	4.5	V
Analog Input Voltage	AINT/AINC	VSS to VDD	V
Digital Input Voltage	CLK	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 150	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTE:

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently.
    Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability.
    Each condition value is applied with the other values kept within the following operating conditions and function
    operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA1 VDDA2 VDDA3	3.15	3.3	3.45	V
Analog Input Voltage	AINT AINC	0.5	– 1.5	2.5	V
Operating Temperature	Toper	0	–	70	°C

NOTE: It is strongly recommended that all the supply pins (VDDA1, VDDA2, VDDA3) be powered from the same source
to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Differential Nonlinearity	DNL	–	±0.7	±1	LSB	Internal Voltage Reference REFTOP=2V REFBOT=1V
Integral Nonlinearity	INL	–	±1.5	–	LSB	Internal Voltage Reference REFTOP=2V REFBOT=1V
Offset Voltage	OFF	–	10	–	mV	REFTOP=2V REFBOT=1V

NOTE: Converter Specifications : VDDA1=VDDA2=VDDA3=3.3V, VSSA1=VSSA2=VSSA3=0V, Toper=25°C, REFTOP=2V, REFBOT=1V unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Maximum Conversion Rate	fc	–	10	–	MHz	AIN=AINT-AINC
Dynamic Supply Current	IVDD	–	36	–	mA	fc=10MHz (without system load)
Signal-to-Noise & Distortion Ratio	SNDR	–	72	–	dB	AIN=1MHz, Differential Input
Total Harmonic Distortion	THD	–	80	–	dB	AIN=1MHz, Differential Input

NOTE: It is strongly recommended that all the supply pins (VDDA1, VDDA2, VDDA3) be powered from the same source to avoid power latch-up.

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I/O CHART

Index	AINT Input (V)	Digital Output	
0	~ 0.00081	0000 0000 0000	1LSB=0.806mV
1	0.00081 ~ 0.00161	0000 0000 0001	VREF=3.3V
2	0.00161 ~ 0.00242	0000 0000 0010	AGND=0.0V
~	~	~	
2047	1.64919 ~ 1.65000	0111 1111 1111	
2048	1.65000 ~ 1.65081	1000 0000 0000	
2049	1.65081 ~ 1.65161	1000 0000 0001	
~	~	~	
4093	3.29758 ~ 3.29839	1111 1111 1101	
4094	3.29839 ~ 3.29919	1111 1111 1110	
4095	3.29919 ~	1111 1111 1111	

TIMING DIAGRAM
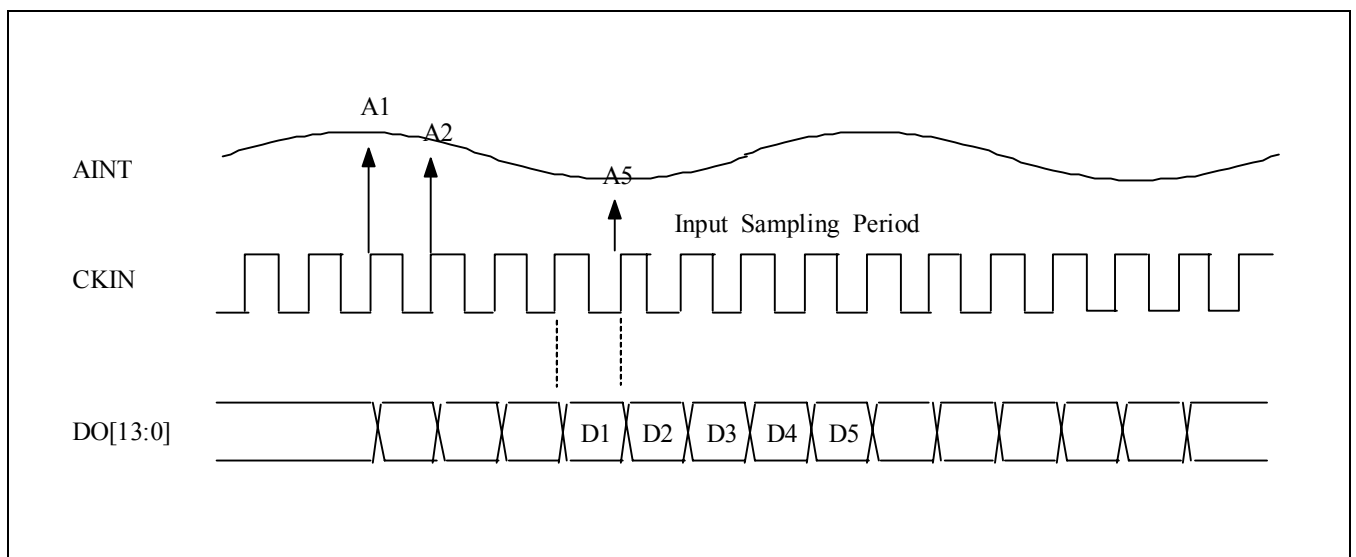
FUNCTIONAL DESCRIPTION

1. The BW1254X is a CMOS four step pipelined Analog-to-Digital Converter. It contains 5-bit flash A/D Converters, 4bit, two 3bit flash A/D converters and three multiplying D/A Convertors. The N-bit flash ADC is composed of 2N-1 latched comparators, and multiplying DAC is composed of 2*(2N+1) capacitors and two fully-differential amplifiers.

2. The BW1254X operates as follows. During the first "L" cycle of external clock the analog input data is sampled, and the input is held from the rising edge of the external clock, which is fed to the first 5-bit flash ADC, and the first multiplying DAC. Multiplying DAC reconstructs a voltage corresponding to the first 5-bit ADC's output, and finally amplifies a residue voltage by 24. The second and third flash ADC, and MDAC are worked as same manner. Finally amplified residue voltage at the third multiplying DAC is fed to the last 3-bit flash ADC decides final 3-bit digital digital code.

3. BW1254X has the error correction scheme, which handles the output from mismatch in the first, second, third and fourth flash ADC.

MAIN BLOCK DESCRIPTION

1. SHA
   SHA (Sample-and-Hold Amplifier) is the circuit that samples the analog input signal and hold that value until next sample-time. It is good as small as its different value between analog input signal and output signal. SHA amp gain is higher than 70dB at 10MHz conversion rate, its settling-time must be shorten than 38ns with less than 1/2 LSB error voltage at 14bit resolution. This SHA is consist of fully differential op amp, switching tr. and sampling capacitor. The sampling clock is non-overlapping clock (Q1, Q2) and sampling capacitor value is about 4pF. SHA uses independent bias to protect interruption of any other circuit. SHA amp is designed that open-loop dc gain is higher than 70dB, phase margin is higher than 60 degrees. Its input block is designed to be the rail-to-rail architecture using complementary different pair.

2. FLASH
   The 5-bit flash converters compare analog signal (SAH output) with reference voltage, and that results transfer to MDAC and digital correction logic block. It is realized fully differential comparators of 31EA. Considering self-offset, dynamic feed through error, it should distinguish 40mV at least. First, the comparators charge the reference voltage at the sampling capacitors before transferred SHA output.That operation is performed on the phase of Q2, and discharging on the phase of Q1. That is, the comparators compare relative different values dual input voltage with dual reference voltage. Its output during Q1 operation is stored at the pre-latch block by Q1P.

3. MDAC
   MDAC is the most important block at this ADC and it decides the characteristics. MDAC is consist of two stage op amp, selection logic and capacitor array (c_array). c_array's compositions are the capacitors to charge the analog input and and the reference voltage, switches to control the path. Selection logic controls the c_array internal switches. If Q1 is high, selection's output are all low, the switches of tsw1 are off, the switches of tsw2 are all on. Therefore the capacitors of c_array can charge analog input values held at SHA.

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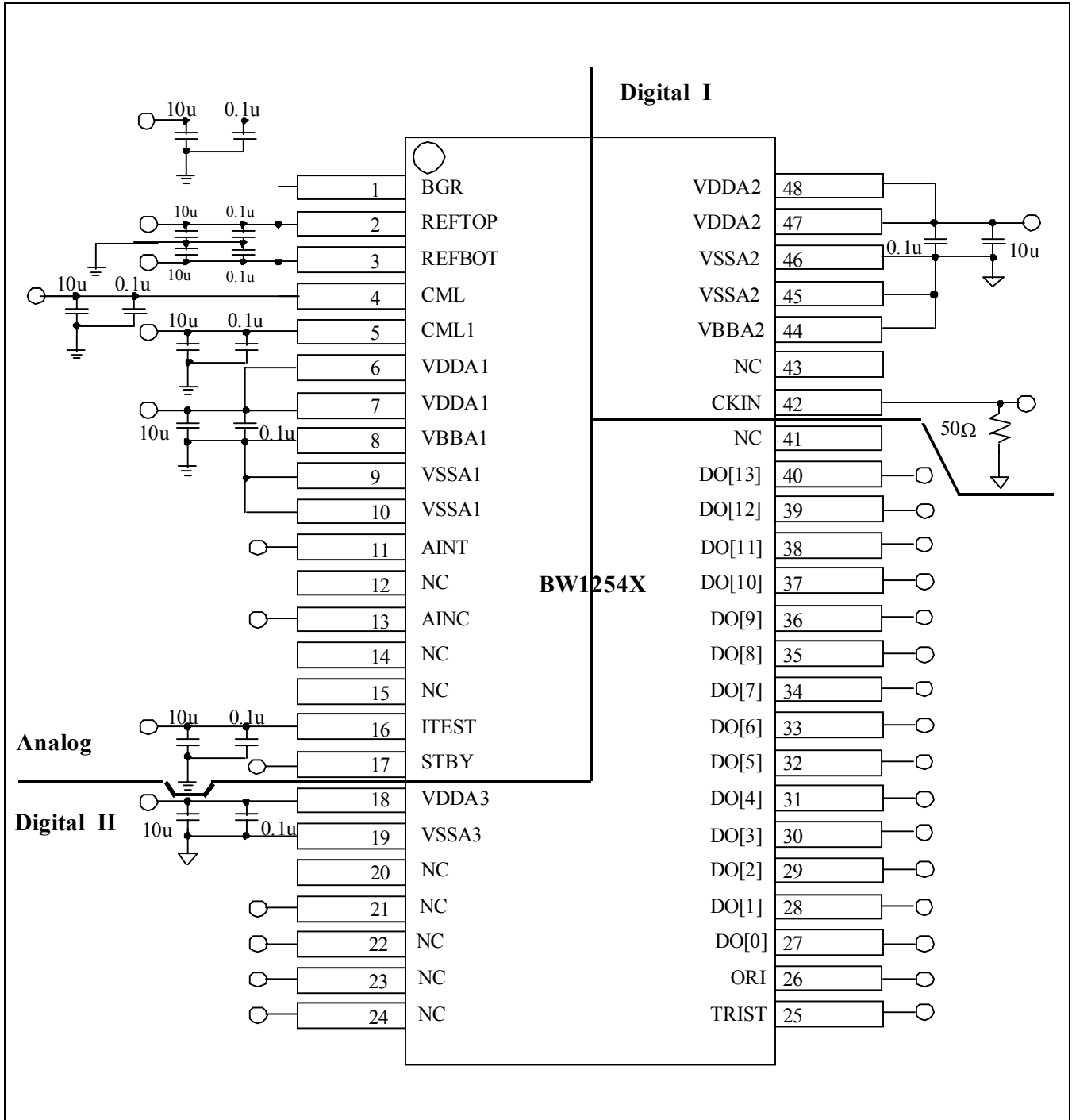## CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.

2. If User want the specific analog input range, the reference voltages may be forced.
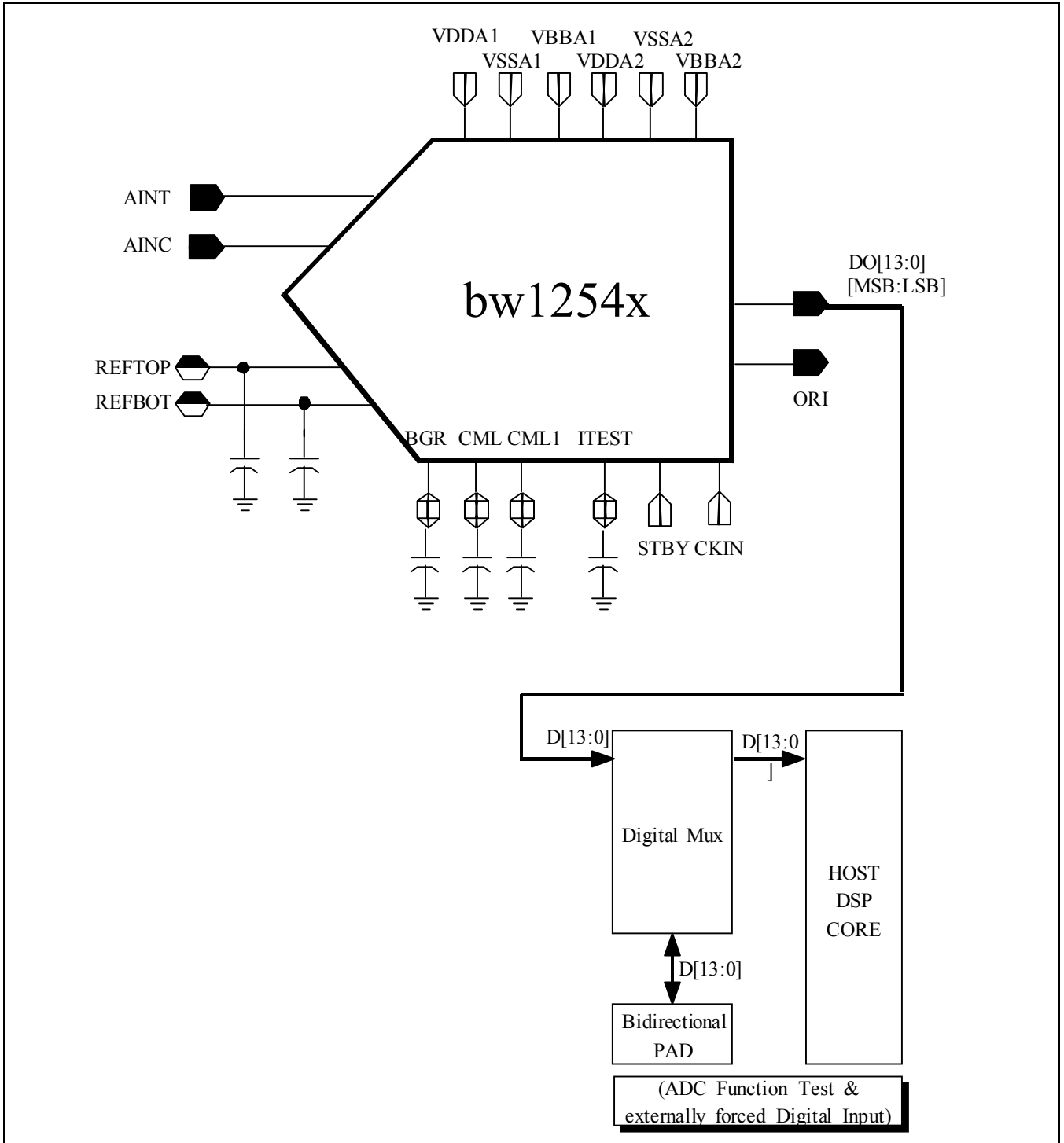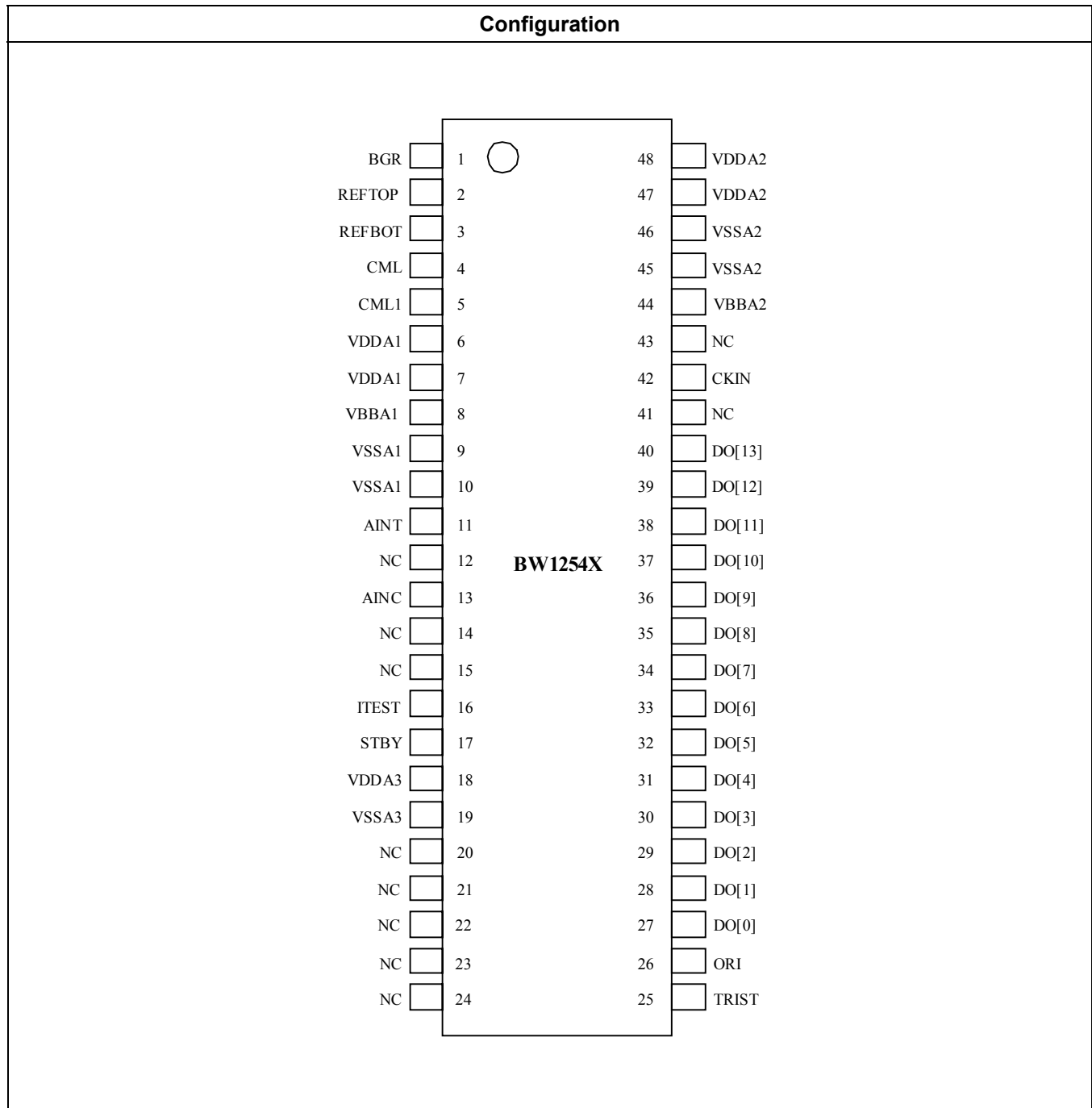
PACKAGE CONFIGURATION

NOTE: NC denotes "No Connection".

PACKAGE PIN DESCRIPTION

Pin No.	Name	I/O Type	Pin Description
1	BGR	AB	Reference Voltage Output
2	REFTOP	AB	Reference Top Output/Force
3	REFBOT	AB	Reference bottom Output/Force
4	CML	AB	Internal Bias
5	CML1	AB	Internal Bias
6, 7	VDDA1	AP	Analog Power (3.3V)
8	VBBA1	AG	Analog Sub Bias
9, 10	VSSA1	AG	Analog Ground
11	AINT	AI	Analog Input +
13	AINC	AI	Analog Input -
16	ITEST	AB	open=use internal bias circuit
17	STBY	DI	VDDA=Power saving (Standby), GNP=Normal
18	VDDA3	PP	PAD Power (3.3V)
19	VSSA3	PG	PAD Ground
25	TRIST	DI	Tri-state Buffer Input VDD=High Impedance, GND=Normal
26	ORI	DO	Out of Range Indicator Normal='Low' Out of Range='High'
27	DO[0]	DO	Digital Output (LSB)
28~39	DO[1:12]	DO	Digital Output
40	DO[13]	DO	Digital Output (MSB)
42	CKIN	DI	Sampling Clock Input
44	VBBA2	DG	Digital Sub Bias
45, 46	VSSA2	DG	Digital GND
47, 48	VDDA2	DP	Digital Power (3.3V)

NOTE: I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.

PACKAGE PIN DESCRIPTION (Continued)

Configuration

BGR	1		48	VDDA2
REFTOP	2		47	VDDA2
REFBOT	3		46	VSSA2
CML	4		45	VSSA2
CML1	5		44	VBBA2
VDDA1	6		43	NC
VDDA1	7		42	CKIN
VBBA1	8		41	NC
VSSA1	9		40	DO[13]
VSSA1	10		39	DO[12]
AINT	11		38	DO[11]
NC	12	**BW1254X**	37	DO[10]
AINC	13		36	DO[9]
NC	14		35	DO[8]
NC	15		34	DO[7]
ITEST	16		33	DO[6]
STBY	17		32	DO[5]
VDDA3	18		31	DO[4]
VSSA3	19		30	DO[3]
NC	20		29	DO[2]
NC	21		28	DO[1]
NC	22		27	DO[0]
NC	23		26	ORI
NC	24		25	TRIST

USER GUIDE

1. Input Range

    —   If you want to using the single-ended input, you should use he input range as below.
        AINT: 0.5V ~ 2.5V,
        AINC: 1.5V.

    —   If you want to using the differential input, you should use the input range as below.
        AINT: 1.0V ~ 2.0V,
        AINC: 1.0V ~ 2.0V.
        AIN: AINT - AINC

    —   If you want to changing input range (AIN span), you can force reference voltages.
        AIN span = -REF ~ +REF
        REF = REFTOP - REFBOT

2. Power Consumption/Speed Optimization
    Yon can optimize the power consumption, as control the ITEST voltage level precisely .
    You can optimize the ADC's speed also, as control the ITEST voltage level.

PHANTOM CELL INFORMATION

— Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.

PHANTOM CELL INFORMATION (Continued)

Pin Name	Pin Usage	Pin Layout Guide
VDDA	External	- Maintain the large width of lines as far as the pads.
VSSA	External	- place the port positions to minimize the length of power lines.
VBBA	External	- Do not merge the analog powers with anoter power from other
VDDD	External	blocks.
VSSD	External	- Use good power and ground source on board.
VBBD	External	
AINT	External/Internal	- Do not overlap with digtal lines. - Maintain the shotest path to pads.
AINC	External/Internal	
CKIN	External/Internal	- Separate from all other analog signals
REFTOP	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
REFBOT	External/Internal	
CML	External/Internal	- Separate from all other digital lines.
CML1	External/Internal	
BGR	External/Internal	
ITEST	External/Internal	
STBY	External/Internal	
ORI	External/Internal	- Separated from the analog clean signals if possible. - Do not exceed the length by 1,000um.
DO[13]	External/Internal	
DO[12]	External/Internal	
DO[11]	External/Internal	
DO[10]	External/Internal	
DO[9]	External/Internal	
DO[8]	External/Internal	
DO[7]	External/Internal	
DO[6]	External/Internal	
DO[5]	External/Internal	
DO[4]	External/Internal	
DO[3]	External/Internal	
DO[2]	External/Internal	
DO[1]	External/Internal	
DO[0]	External/Internal	

FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic checking table and fill out the additional questions.

We appreciate your interest in our products. Thank you very much.

Characteristic	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Bit Resolution				Bit	
Reference Input Voltage				V	
Analog Input Voltage				Vpp	
Operating Temperature				°C	
Integral Non-linearity Error				LSB	
Differential Non-linearity Error				LSB	
Bottom Offset Voltage Error				mV	
Top Offset Voltage Error				mV	
Maximum Conversion Rate				MSPS	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Signal-to-noise Ratio				dB	
Pipeline Delay				CLK	
Digital Output Format (Provide detailed description & timing diagram)					

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?

2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.

3. Freely list those functions you want to be implemented in our ADC, if you have any.

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HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0	99.6.	Original version published (formal)	
ver 1.1	02.4.16	Phantom information added and the datasheet format changed	

NOTES