APPLICATIONS

- Home Automation and Security
- Automatic Meter Reading
- Factory Automation and Motor Control
- Medical Patient Monitoring
- Voice Applications
- Replacement for legacy wired UART
- Energy Management
- Remote Keyless Entry w/ Acknowledgement
- Toys
- PC peripherals

KEY FEATURES

- **Embedded** 8051 Compatible **Microprocessor** with 96KB Embedded Flash Memory for Program Space plus 8KB of Data Memory
- **Scalable Data Rate**: 250kbps for ZigBee, 500kbps and 1Mbps for custom applications.
- **Voice Codec** Support: µ-law/a-law/ADPCM
- High RF **RX Sensitivity**: –98dBm @1.5V
- High RF **TX Power**: +8dBm @1.5V
- 4 Level **Power Management** Scheme with Deep Sleep Mode (0.3µA)
- **Single Voltage** operation: 1.9 to 3.3V using an internal regulator (1.5V core)
- Software **Tools and Libraries** for the Development of Custom Applications

DESCRIPTION:

ZIC2410 is a true single-chip solution, compliant with ZigBee specifications and IEEE802.15.4, a complete wireless solution for all ZigBee applications. The *ZIC2410* consists of an RF transceiver with baseband modem, a hardwired MAC and an embedded 8051 microcontroller with internal flash memory. The device provides numerous general-purpose I/O pins,

peripheral functions such as timers and UART and is one of the first devices to provide an embedded Voice CODEC. This chip is ideal for very low power applications.

The *ZIC2410* is available in two industry standard packages: a 48-pin QFN (7x7mm) or a 72-pin VFBGA (5x5mm) package.

CEL provides its customers with the *CEL ZigBee Stack*, software in a compiled library, as well as all the hardware & software tools required to develop custom applications. User application software can be compiled using any popular C-language compiler such as Keil.
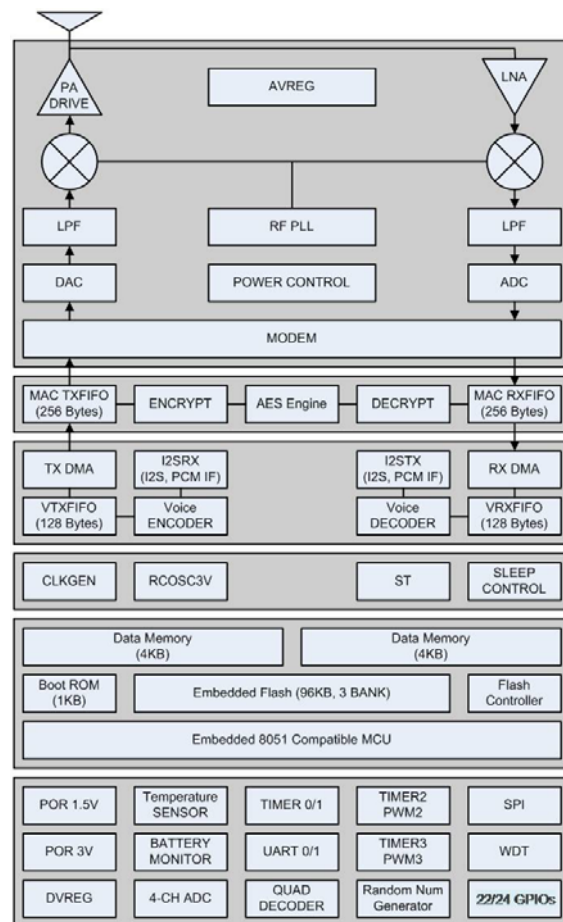
FEATURES

RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Programmable Output Power up to +8dBm@1.5V
- High Sensitivity of –98dBm@1.5V
- Scalable Data Rate: 250Kbps for ZigBee, 500Kbps and 1Mbps for custom application
- On-chip VCO, LNA, and PA
- Low Operating Voltage of 1.5V
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- RSSI Measurement
- Compliant to IEEE802.15.4
- No External T/R Switch or Filter needed

Hardwired MAC

- Two 256-byte circular FIFOs
- FIFO management
- AES Encryption/Decryption Engine (128bit)
- CRC-16 Computation and Check

8051-Compatible Microcontroller

- 8051 Compatible (single cycle execution)
- 96KB Embedded Flash Memory
- 8KB Data Memory
- 128-byte CPU dedicated Memory
- 1KB Boot ROM
- Dual DPTR Support
- Multi-Bank Support for 96KB Program Memory (3Banks of 32KB)
- I2S/PCM Interface with two128-byte FIFOs
- µ-law/a-law/ADPCM Voice Codec
- Two High-Speed UARTs with Two 16-byte FIFOs (up to 1Mbps)
- 4 Timers/2 PWMs
- Watchdog Timer
- Sleep Timer
- Quadrature Signal Decoder
- 24 General Purpose I/Os
- Internal RC oscillator for Sleep Timer
- On-chip Power-on-Reset

- 4-channel 8-bit ADC
- SPI Master/Slave Interface
- ISP (In System Programming)
- Internal Temperature Sensor

Clock Inputs

- 16MHz Crystal for System Clock (optional 19.2MHz)
- 32.768KHz Crystal for Sleep Timer (optional)

Power

- Internal Regulator for Single Voltage Operation w/ a large input voltage range (1.9~3.3V)
- 4-Level Power Management Scheme with Deep Sleep Mode (0.3µA)
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Battery Monitoring Support

Included Software

- Application Framework
- Software Tools
- IEEE and ZigBee Compliant Libraries

Package Options

- Lead-Free 48-pin QFN Package (shown below) (7mm x 7mm x 0.9mm)
- Lead-Free 72-pin VFBGA Package (5mm × 5mm x 0.9mm)

ORDERING INFORMATION

| Ordering Part Number	Description	Minimum Order Quantity (MOQ)
ZIC2410QN48R	48-pin QFN Package (T/R)	Tape & Reel (2500 per reel)
ZIC2410FG72R	72-pin VFBGA Package (T/R)	Tape & Reel (2500 per reel)
ZIC2410-EDK-1	Demonstration Kit	1

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1 FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram of ZIC2410. The ZIC2410 consists of a 2.4GHz RF, Modem (PHY Layer), a MAC hardware engine, a Voice CODEC block, Clocks, Peripherals, and a memory and Microcontroller (MCU) block.
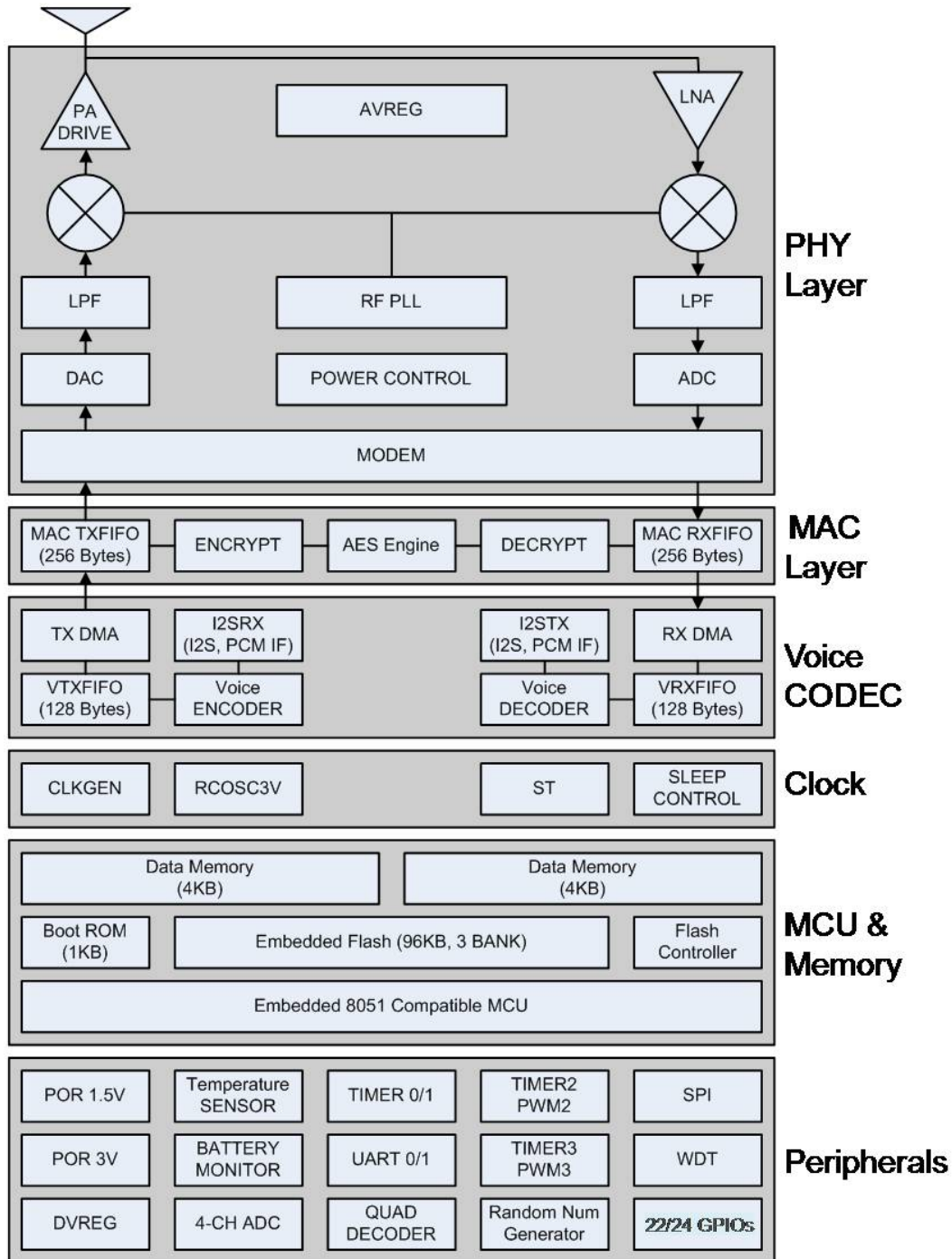
Figure 1 – Functional Block Diagram of ZIC2410
Note: The ZIC2410QN48 has 22 GPIOs; the ZIC2410FG72 has 24.

1.1 FUNCTIONAL OVERVIEW

In the receive mode, the received RF signal is amplified by the Low Noise Amplifier (LNA), down-converted to a quadrature signal and then to baseband. The baseband signal is filtered, amplified, converted to a digital signal by the ADC and transferred to a modem. The data, which is the result of signal processing such as dispreading, is transferred to the MAC block.

In transmit mode, the buffered data at the MAC is transferred to a baseband modem which, after signal processing such as spreading and pulse shaping, outputs a signal through the DAC. The Analog baseband signal is filtered by the low-pass filter, converted to RF signal by the up-conversion mixer, is amplified by PA, and finally applied to the antenna.

The MAC block provides IEEE802.15.4 compliant hardware and it is located between microprocessor and a baseband modem. MAC block includes FIFOs for transmitting/receiving packet, AES engine for security operation, CRC and related control circuit. In addition, it supports automatic CRC check and address decoding.

ZIC2410 integrates a high performance embedded microcontroller, compatible to an Intel i8051 microcontroller in an instruction level. This embedded microcontroller has 8-bit operation architecture sufficient for controller applications. The embedded microcontroller has 4-stage pipeline architecture to improve the performance over previous compatible chips making it capable of executing simple instructions during a single cycle.

The memory organization of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detailed explanation, refer to the data memory section (1.2.2.)

The ZIC2410 includes 22 GPIO for the QN48 packaged device and 24 GPIO for the FG72 packaged part and various peripheral circuits to aid in the development of an application circuit with an interrupt handler to control the peripherals. ZIC2410 uses 16MHz crystal oscillator for RF PLL and 8MHz clock generated from 16MHz in clock generator is used for microcontroller, MAC, and the clock of a baseband modem.

The ZIC2410 supports a voice function as follows. The data generated by an external ADC is input to the voice block via I2S interface. After the data is received via I2S it is compressed by the voice codec, and stored in Voice TXFIFO. The data in Voice TXFIFO is transferred to the MAC TXFIFO and then transmitted via PHY. In contrast, the received data in MAC RXFIFO is transferred to voice RXFIFO via DMA operation. The data in voice RXFIFO is decompressed by the internal voice codec. The decompressed data is then transferred to the external DAC via I2S interface.

1.2   MEMORY ORGANIZATION

1.2.1   PROGRAM MEMORY

The address space of the program memory is 64KB (0x0000~0XFFFF). Basically, the lower 63KB of program memory is implemented by Non-volatile memory. The upper 1KB from 0XFC00 to 0XFFFF is implemented by both Non-volatile memory and ROM. As shown in Figure 2 below, there are two types of memory in the same address space. The address space, which is implemented by Non-volatile memory, is used as general program memory and the address space, which is implemented by ROM, is used for ISP (In-System Programming).

As shown in (a) of Figure 2 below, when Power is turned on, the upper 1KB of program memory is mapped to ROM. As shown in (b) of Figure 2, if this program area (1KB) is used as non-volatile program memory, ENROM should be set to '0'. See the SFR section (1.2.4) for ENROM.

(a)

0xFFFF

0xFC00

BOOT LOADER
(1KB)

0xFBFF

PROGRAM MEMORY
(63KB)

0x0000

ENROM = 1 (AFTER RESET)

(b)

0xFFFF

BOOT LOADER
(1KB)

0xFC00

0xFBFF

PROGRAM MEMORY
(64KB)

0x0000

ENROM = 0
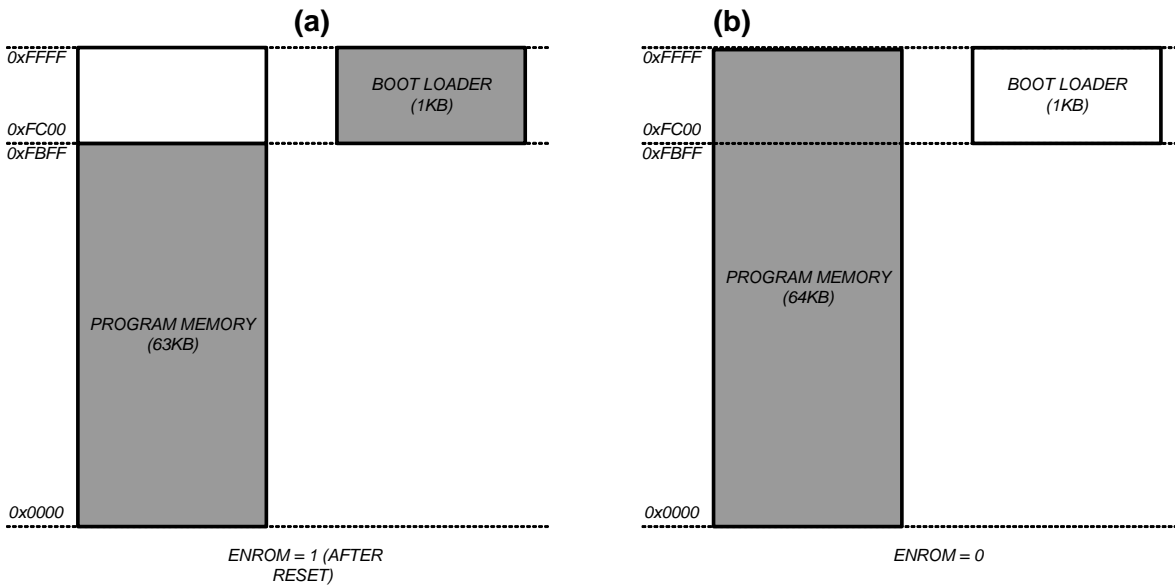
Figure 2 – Address Map of Program Memory

ZIC2410 includes non-volatile memory of 96KB. However, as described already, program memory area is 64KB. Therefore, if necessary, the upper 64KB of physical 96KB non-volatile memory is separated into two 32KB memory banks. Each bank is logically mapped to the program memory. When FBANK value is '0', lower 64KB of non-volatile memory is used as shown in (a) of Figure 3. When FBANK value is '1', lower 32 KB and upper 32KB of non-volatile memory are used as shown in (b) of Figure 3. See the SFR section (1.2.4) for FBANK.

(a)   **(b)**
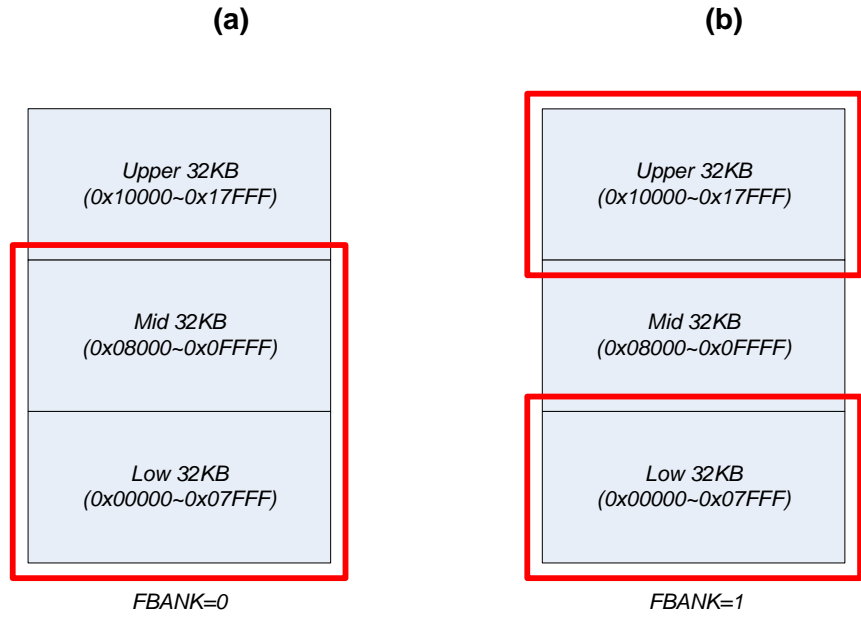
Figure 3 – Bank Selection of Program Memory

1.2.2   DATA MEMORY

ZIC2410 reserves 64 KB of data memory address space. This address space can be accessed
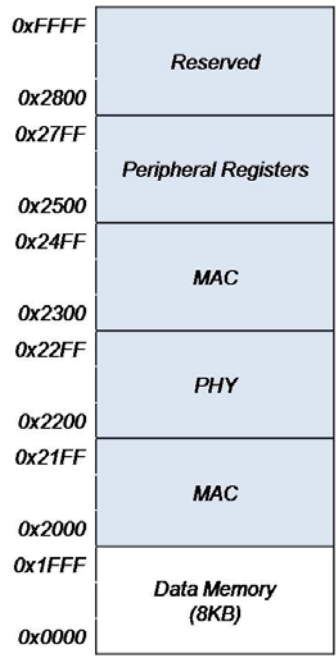
by the MOVX command.

Figure 4 shows the address map of this data memory.
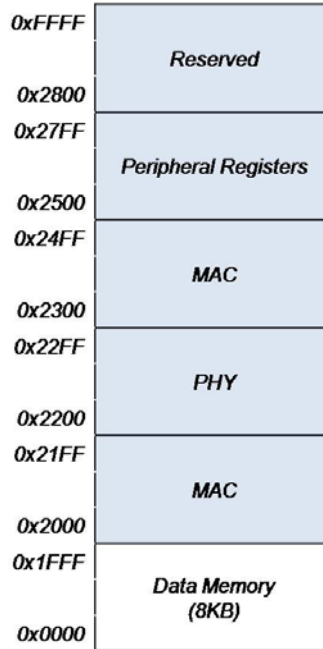
Figure 4 – Address Map of Data Memory

The data memory used in the application programs resides in the address range 0x0000-0x1FFF.

The registers and memory used in the MAC block reside in the address range 0x2000-0x21FF and 0x2300-0x24FF respectively. The registers to control or report the status of the PHY block reside in the address range 0x2200-0x22FF.

Registers related to the numberous peripheral functions of the embedded microprocessor reside in the address range of 0x2500-0x27FF.

1.2.3   GENERAL PURPOSE REGISTERS (GPR)
Figure 5 describes the address map of the General Purpose Registers (GPRs). GPRs can be addressed either directly or indirectly. As shown in the lower address space of Figure 5, a bank consists of 8 registers.

The address space above the bank area is the bit addressable area, which is used as a flag by software or by a bit operation. The address space above the bit addressable area includes registers used as a general purpose of a byte unit. For the detailed information, refer to the paragraphs following Figure 5 below.
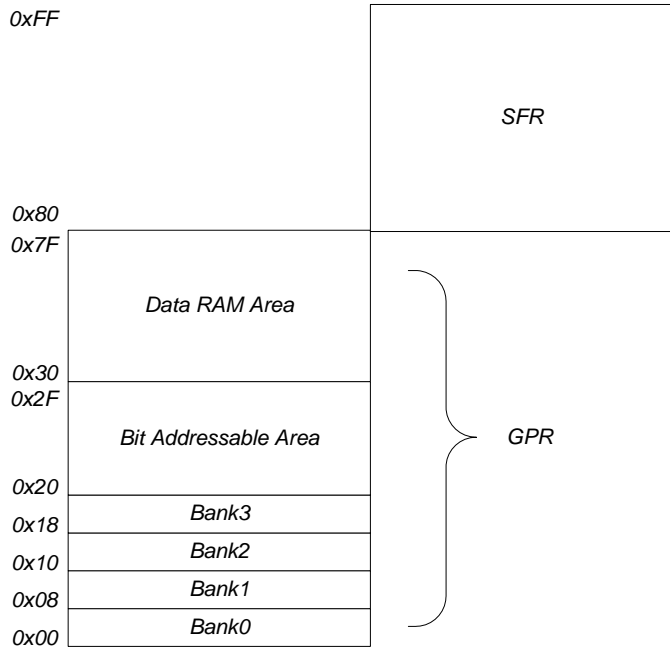
Figure 5 – GPRs Address Map

Register Bank 0-3: It is located from 0x00 to 0x1F (32 bytes). One bank consists of each 8 registers out of 32 registers. Therefore, there are total 4 banks. Each bank should be selected by software as referring the RS field in PSW register. The bank (8 registers) selected by RS value can be accessed by a name (R0-R7) by software. After reset, the default value is set to bank0.

Bit Addressable Area: The address is assigned to each bit of 16 bytes (0x20~0x2F) and registers, which is the multiple of 8, in SFR. Each bit can be accessed by the address which is assigned to these bits. 128 bits (16 bytes, 0x20~0x2F) can be accessed by direct addressing for each bit (0~127) and by a byte unit as using the address from 0x20~0x2F.

Data RAM Area: A user can use registers (0x30~0x7F) as a general purpose.

1.2.4   SPECIAL FUNCTION REGISTERS (SFR)

Generally, a register is used to store the data. MCU needs the memory to control the embedded hardware or the memory to show the hardware status. Special Function Registers (SFRs) process the functions described above. SFRs include the status or control of the I/O ports, the timer registers, the stack pointers and so on. Table 1 shows the address to all SFRs in ZIC2410.

All SFRs are accessed by a byte unit. However, when SFR address is a multiple of 8, it can be accessed by a bit unit.

Table 1 – Special Function Register (SFR) Map

Register Name	SFR Address	B7	B6	B5	B4	B3	B2	B1	B0	Initial Value
EIP	0xF8		VCEIP	SPIIP	RTCIP	T3IP	AESIP	T2IP	RFIP	0x00
B	0xF0									0x00
EIE	0xE8		VCEIE	SPIIE	RTCIE	T3IE	AESIE	T2IE	RFIE	0x00

Register Name	SFR Address	B7	B6	B5	B4	B3	B2	B1	B0	Initial Value
ACC	0xE0									0x00
EICON	0xD8					RTCIF				0x00
WDT	0xD2				WDTWE	WDTEN	WDTCLR	WDTPRE		0x0B
PSW	0xD0	CY	AC	F0	RS		OV	F1	P	0x00
WCON	0xC0						ISPMODE	ENROM		0x00
P3REN	0xBC									0xFF
P1REN	0xBA									0xFF
P0REN	0xB9									0xFF
IP	0xB8		PS1		PS0	PT1	PX1	PT0	PX0	0x00
P3OEN	0xB4									0x00
P1OEN	0xB2									0x00
P0OEN	0xB1									0x00
P3	0xB0									0x3F
TL3	0xAD									0x00
TL2	0xAC									0x00
TH3	0xAB									0x00
TH2	0xAA									0x00
T23CON	0xA9					TR3	M3	TR2	M2	0x00
IE	0xA8	EA	ES1		ES0	ET1	EX1	ET0	EX0	0x00
AUXR1	0xA2								DPS	0x00
FBANK	0xA1	RAM1	RAM0					FBANK		0x00
EXIF	0x91	T3IF	AESIF	T2IF	RFIF					0x00
P1	0x90									0xFF
TH1	0x8D									0x00
TH0	0x8C									0x00
TL1	0x8B									0x00
TL0	0x8A									0x00
TMOD	0x89	GATE1	CT1	M1		GATE0	CT0	M0		0x00
TCON	0x88	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0x00
PCON	0x87							PD	IDLE	0x00
P0SEL	0x85							ExNoEdge	P0AndSEL	0x00
P0MSK	0x84									0xFF
DPH	0x83									0x00
DPL	0x82									0x00
SP	0x81									0x07
P0	0x80									0xFF

The following section describes each SFR related to microprocessor.

Table 2 – Register Bit Conventions

Symbol	Access Mode
RW	Read/write
RO	Read Only

Table 3 – Special Function Registers

Bit	Name	Descriptions	R/W	Reset Value
WCON (WRITE CONTROL REGISTER, 0xC0) This register can control the upper 1KB of program memory.				
7:3		Reserved		0
2	**ISPMODE**	**ISP Mode Indication**: When MS [1:0], an external pin, is '3', this field is set to 1 by hardware. It notifies the MCU whether ISPMODE or not.	RO	-
1	**ENROM**	When this field is '1', the upper 1KB (0xFC00~0xFFFF) is mapped to ROM. When this field is '0', the upper 1KB (0xFC00~0xFFFF) is mapped to non-volatile memory.	R/W	1
0		Reserved		0
FBANK (PROGRAM MEMORY BANK SELECTION REGISTER, 0xA1)				
7:1		Reserved		0x00

0	**FBANK**	Program Memory Bank Select.
		    0: Bank0 (Default)
		    1: Bank1
		    2: Not Used
		    3: Not Used
			R/W	0

ACCUMULATOR (0xE0) This register is marked as A or ACC and it is related to all the operations.				
7:0	**A**	Accumulator	R/W	0x00
B REGISTER (0xF0) This register is used for a special purpose when multiplication and division are processed. For other instructions, it can be used as a general-purpose register. After multiplication is processed, this register contains the MSB data and 'A register' contains LSB data for the multiplication result. In division operation, this register stores the value before division (dividend) and the remainder after division. At this time, before division, the divisor should be stored in 'A register' and result value (quotient) is stored in it after division**.**				
7:0	**B**	B register. Used in MUL/DIV instructions.	R/W	0x00
PROGRAM STATUS WORD (PSW, 0xD0) This register stores the status of the program. The explanation for each bit is as follows.				
7	**CY**	Carry flag	R/W	0
6	**AC**	Auxiliary carry flag	R/W	0
5	**F0**	Flag0. User-defined	R/W	0

4:3	**RS**	Register bank select.
		    0: Bank0
		    1: Bank1
		    2: Bank2
		    3: Bank3
			R/W	0

2	**OV**	Overflow flag	R/W	0
1	**F1**	Flag1. User-defined	R/W	0
0	**P**	Parity flag. Set to 1 when the value in accumulator has odd number of '1' bits.	R/W	0
STACK POINTER (0x81) When PUSH and CALL commands are executed, some data (like the parameters by function call) are stored in stack to inform the values. In the embedded MCU, the data memory area which can be used for a general purpose (0x08~0x7F) is used as a stack area. This register value is increased before the data is stored and the register value is decreased after the data is read when the data of stack is disappeared by POP and RET command. The default value is 0x07.				
7:0	**SP**	Stack Pointer	R/W	0x07

Bit	Name	Descriptions	R/W	Reset Value
		**DATA POINTER (DPH: 0x83, DPL: 0x82)** Data pointer consists of a high byte (DPH) and a low byte (DPL) to support 16-bit address. It can be accessed by 16-bit register or by two 8-bit registers respectively.		
7:0	**DPH**	Data pointer, high byte	R/W	0x00
7:0	**DPL**	Data pointer, low byte	R/W	0x00
		AUXR1 (AUXILIARY CONTROL REGISTER, 0xA2) This register is used to implement Dual DPTR functions. Physically, DPTR consists of DPTR0 and DPTR1. However, DPTR0 and DPTR1 can be accessed depending on the DPS value of AUXR1 respectively. In other words, they cannot be accessed at the same time.		
7:1		Reserved		0x00
0	**DPS**	**Dual DPTR Select**: Used to select either DPTR0 or DPTR1. When DSP is '0', DPTR0 is selected. When DSP is '1', DPTR1 is selected.	R/W	0
		P3 (0xB0) This port register can be used as other functions besides general purpose I/O.		
7	**P3.7**	This port register is used as a general purpose I/O port (12mA Drive).	R/W	0
	/PWM3	When Timer3 is operated as a PWM mode, it outputs PWM wave (PWM3) of Timer3.		
	/CTS1	When port register is used as UART1, it is used as a CTS signal (CTS1) of UART1.		
	/SPICSN	When used as a Master mode, SPI Slave Select signal is outputted. When used as a Slave mode, this port register receives SPI Slave Select signal. This signal activate in low		
6	**P3.6**	This port register is used as a general purpose I/O port (12mA Drive)	R/W	0
	/PWM2	When Timer2 is operated as a PWM mode, it outputs PWM wave (PWM2) of Timer2.		
	/RTS1	When port register is used as UART1, it is used as a RTS signal (RTS1) of UART1.		
	/SPICLK	When used as a Master mode, SPI clock is outputted. When used as a Slave mode, this port register receives SPI clock.		
5	**P3.5**	This port register is used as a general purpose I/O port.	R/W	1
	/T1	When Timer1 is operated as a COUNTER mode, it is operated as a counter input signal (T1) of Timer1.		
	/CTS0	When port register is used as UART0, it is used as a CTS signal (CTS0) of UART0.		
	/SPIDO	In a Master mode or a Slave mode, this port register is used for outputting SPI data.		
	/QUADYB	When port register is used as QUAD function, it is used as the input signal of YB value.		
4	**P3.4**	This port register is used as a general purpose I/O port.	R/W	1
	/T0	When Timer0 is operated as a COUNTER mode, it is operated as a counter input signal (T0) of Timer0.		
	/RTS0	When port register is used as UART0, it is used as a RTS signal (RTS0) of UART0.		

Bit	Name	Descriptions	R/W	Reset Value
	/SPIDI	In a Master mode or a Slave mode, this port register is used for receiving SPI data.		
	/QUADYA	When port register is used as QUAD function, it is used as the input signal of YA value.		
3	P3.3	This port register is used as a general purpose I/O port.	R/W	1
	/INT1	When port register is used as an input signal, it can receive an external interrupt (INT1).		
2	P3.2	This port register is used as a general purpose I/O port.	R/W	1
	/INT0	When port register is used as an input signal, it can receive an external interrupt (INT0).		
1	P3.1	This port register is used as a general purpose I/O port.	R/W	1
	/TXD0	When port register is used as UART0, it is used as a UART0 data output (TXD0).		
	/QUADXB	When port register is used as QUAD function, it is used as the input signal of XB value.		
0	P3.0	This port register is used as a general purpose I/O port.	R/W	1
	/RXD0	When port register is used as UART0, it is used as a UART0 data input (RXD0).		
	/QUADXA	When port register is used as QUAD function, it is used as the input signal of XA value.		
P1 (0x90) This port register can be used as other functions besides general purpose I/O.				
7	P1.7	This port register is used as a general purpose I/O port.	R/W	1
	/P0AND	When P0AndSel value in P0SEL register is set to '1', P1.7 outputs the result of bit-wise AND operation of (P0 OR P0MSK).		
	/TRSW	It can be used as TRSW (RF TX/RX Indication signal) signal by setting the PHY register.		
6	P1.6	This port register is used as a general purpose I/O port.	R/W	1
	/TRSWB	It can be used as TRSWB (TRSW Inversion) signal by setting the PHY register.		
5	P1.5	This port register is used as a general purpose I/O port.	R/W	1
4	P1.4	This port register is used as a general purpose I/O port.	R/W	1
	/QUADZB	When this port register is used as QUAD function, it is used as the input signal of ZB value.		
	/RTXTALI	This port register is used for connecting to the external crystal (32.768KHz), which is used in the Sleep Timer, by setting the PHY register.		
3	P1.3	This port register is used as a general purpose I/O port.	R/W	1
	/QUADZA	When this port register is used as QUAD function, it is used as the input signal of ZA value.		

Bit	Name	Descriptions	R/W	Reset Value
	/RTXTALO	This port register is used for connecting to the external crystal (32.768KHz), which is used in the Sleep Timer, by setting the PHY register.		
	/RTCLKO	This port register is used to output the internal RCOSC by setting the PHY register.		
2	**P1.2**	This port register is used as a general purpose I/O port.	R/W	1
1	**P1.1**	This port register is used as a general purpose I/O port.	R/W	1
	/TXD1	When this port register is used as UART1, it is used as UART1 data output (TXD1).		
0	**P1.0**	This port register is used as a general purpose I/O port.	R/W	1
	/RXD1	When this port register is used as UART1, it is used as UART1 data input (RXD1).		
P0 (0x80) This port register can be used as other functions besides general purpose I/O.				
7	**P0.7**	This port register is used as a general purpose I/O port.	R/W	1
	/I2STXMCL K	When this port register is used as I2S, it is operated as TX Master clock of I2S interface.		
6	**P0.6**	This port register is used as a general purpose I/O port.	R/W	1
	/I2STXBCL K	When this port register is used as I2S, it is operated as TX Bit clock of I2S interface.		
5	**P0.5**	This port register is used as a general purpose I/O port.	R/W	1
	/I2STXLRC K	When this port register is used as I2S, it is operated as TX LR clock of I2S interface.		
4	**P0.4**	This port register is used as a general purpose I/O port.	R/W	1
	/I2STXDO	When this port register is used as I2S, it is operated as TX data output of I2S interface.		
3	**P0.3**	This port register is used as a general purpose I/O port.	R/W	1
	/I2SRXMCL K	When this port register is used as I2S, it is operated as RX Master clock of I2S interface.		
2	**P0.2**	This port register is used as a general purpose I/O port.	R/W	1
	/I2SRXBCL K	When this port register is used as I2S, it is operated as RX Bit clock of I2S interface.		
1	**P0.1**	This port register is used as a general purpose I/O port.	R/W	1
	/I2SRXLRC K	When this port register is used as I2S, it is operated as the RX LR clock of the I2S interface.		
0	**P0.0**	This port register is used as a general purpose I/O port.	R/W	1
	/I2SRXDI	When this port register is used as I2S, it is operated as the RX data input of the I2S interface.		
P0OEN/P1OEN/P3OEN (0xB1, 0xB2, 0xB4) P0OEN, P1OEN and P3OEN enable the output of port0, 1 and 3. When each bit is cleared to '0', the output of the corresponding port is enabled. For example, when 4th bit of P1OEN is set to low, the output of port1.3 is enabled.				
7		Reserved		0

Bit	Name	Descriptions	R/W	Reset Value
7:0	**P3OEN**	It controls the TX buffer function for each pin in Port3. When each bit field is set to '0', the TX buffer of the corresponding pin outputs the value.	R/W	0x00
6:0	**P1OEN**	It controls the TX buffer function for each pin in Port1. When each bit field is set to '0', the TX buffer of the corresponding pin outputs the value. P1.7 only acts as output.	R/W	0x00
7:0	**P0OEN**	It controls the TX buffer function for each pin in Port0. When each bit field is set to '0', the TX buffer of the corresponding pin outputs the value.	R/W	0x00
P0REN/P1REN/P3REN (0xB9, 0xBA, 0xBC) P0REN, P1REN, P3REN enable Pull-up of port 0, 1 and 3. When each bit area is cleared to '0', the Pull-up of the corresponding port is enabled.				
7		Reserved		1
7:0	**P3REN**	It controls the Pull-up function for each pin in Port3. When each bit field is set to '0', the Pull-up function of the corresponding pin is operated.	R/W	0xFF
6:0	**P1REN**	It controls the Pull-up function for each pin in Port1. When each bit field is set to '0', the Pull-up function of the corresponding pin is operated. *P1.7 doesn't have a control field because it is operated as an output.*	R/W	0x7F
7:0	**P0REN**	It controls the Pull-up function for each pin in Port0. When each bit field is set to '0', the Pull-up function of the corresponding pin is operated.	R/W	0xFF
P0MSK (P0 INPUT MASK REGISTER, 0x84)				
7:0	**P0MSK**	This register is used for masking the input of P0 pin (Refer to P0AndSel in P0SEL register).	R/W	0xFF
P0SEL (P0 INPUT SELECTION REGISTER, 0x85)				
7:2		Reserved		0
1	**ExNoEdge**	Controls the wake up of the MCU by an external interrupt when in the power-down mode. When this field is '0', the MCU wakes up when INT0 or INT1 signal is high (This is the normal case in the MCU.) When this field is '1', the MCU is woken up by the wakeup signal of the SleepTimer. Remote control function can be implemented by the interrupt service routine of the MCU when the WAKEUP signal occurs by adjusting the RTDLY value in the Sleep Timer while either INT0 or INT1 is low.	R/W	0
0	**P0AndSel**	When this field is set to '1', P0 and P0MSK are ORed per bit. The bits of the result value are to be ANed and then output to P1.7. This function is used to implement remote control function.	R/W	0

1.3 RESET

The ZIC2410 should be reset to be operated. There are three kinds of reset sources. The first one is to use an external reset pin (RESET#). When applying a low signal to this pin for more than 1ms, ZIC2410 is reset. Second, ZIC2410 can be reset by an internal POR when it is powered up as using the internal Power-On-Reset (POR) block. Third, as a reset by the watchdog timer, a reset signal is generated when the internal counter of watchdog timer reaches a pre-set value.

Table 4 – Power-On-Reset Specifications

Parameter	MIN	TYP	MAX	UNIT
1.5V POR Release		1.18		V
1.5V POR Hysteresis		0.11		V

NOTE
Reference circuit of ZIC2410 is as follows. When the ZIC2410 is operated below minimum operating voltage, a reset error will occur because of the unstable voltage. It is recommended to use an external reset IC to improve stability in low voltage conditions.

[Application Circuit by adjusting RESET-IC]
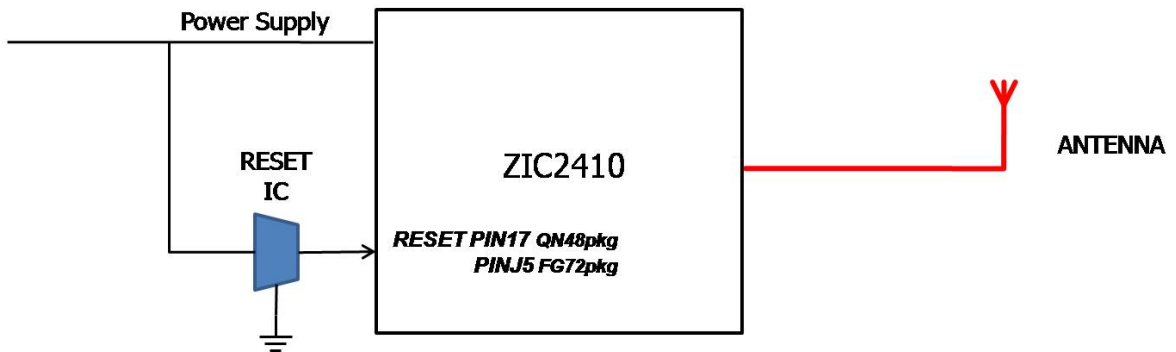
Figure 6 – Reset Circuit
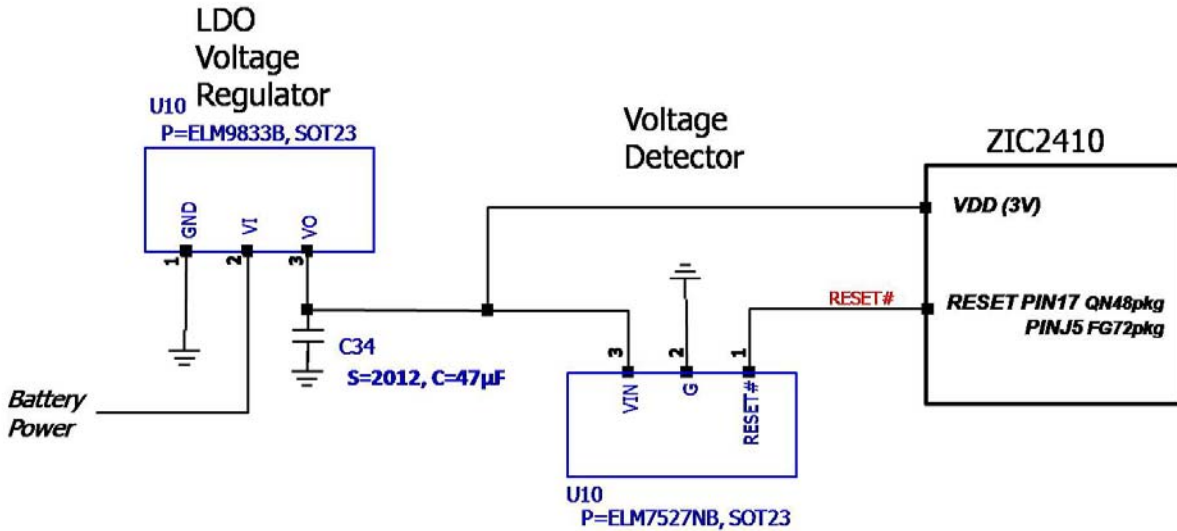
[Reset Circuit by adjusting ELM7527NB]

Figure 7 – Reset Circuit Using ELM7527NB

Checking the RESET-IC Circuit

1. In the application circuit of ZIC2410, please connect RESET# PIN to Pull-up register and should not connect it to capacitor.
2. When applying RESET-IC, detection voltage should be set over 1.9V.
3. The interval (T_reset) until from the time which reset signal by Reset IC has been adjusted to the time which the voltage of VDD (3.0) is dropped to 1.6V should be longer than 1ms.
4. T_reset time is adjusted when modifying capacitor value connected to VDD (3.0).
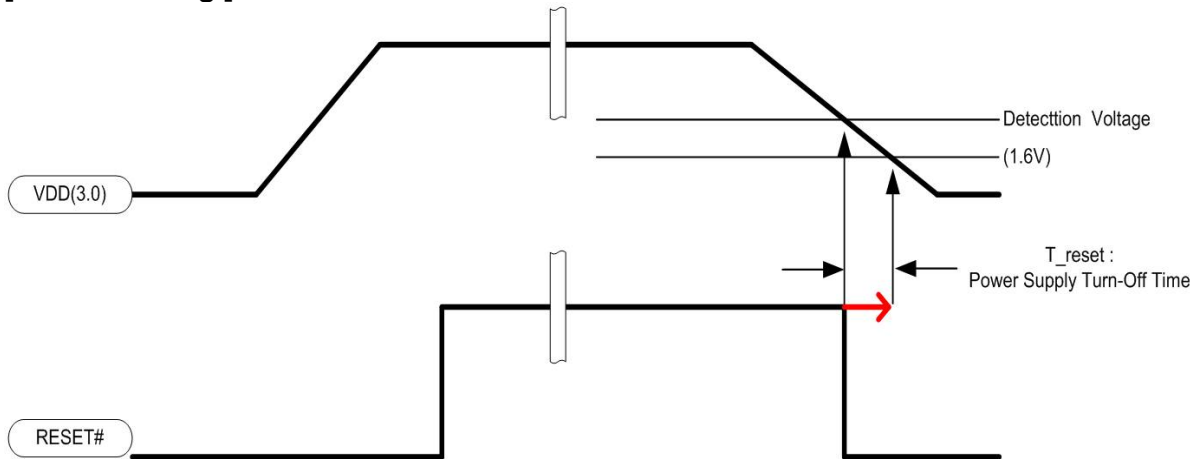
[RESET Timing]

Figure 8 – Reset Timing Diagram

1.4 CLOCK SOURCE

The ZIC2410 can use either a 16MHz or a 19.2MHz crystal as the system clock source. An external 32.768 KHz crystal or the internal clock generated from internal the RCOSC is used for the Sleep Timer clock.

For the internal 8051 MCU Clock in the ZIC2410, either 8MHz or 16MHz can be used. When selecting the 8051 MCU Clock (8MHz, 16MHz), the CLKDIV0 register should be set as follows.

Please note the crystal oscillator input (XOSCI) can also be driven by a CMOS clock source.

CLKDIV0 (OPERATING FREQUENCY CONTROL REGISTER, 0x22C3)

Table 5 – Clock Registers

Bit	Name	Descriptions	R/W	Reset Value
7:0	CLKDIV0	This register is used to control the clock of the internal 8051 MCU. When this register is set to 0xFF, the clock is set to 8MHz; when set to 0x00, the clock is set to 16MHz. All other values except 0xFF and 0x00 are reserved.	R/W	0xFF

1.5 INTERRUPT SCHEMES

The program interrupt functions of the embedded MCU are similar to other microprocessors. When an interrupt occurs, the interrupt service routine at the corresponding vector address is executed. When the interrupt service routine process is completed, the program is resumed from the point of time at which the interrupt occurred. Interrupts can be initiated from the internal operation of the embedded microprocessor (e.g. the overflow of the timer count) or from an external signal.

The ZIC2410 has 13 interrupt sources. Table 6 describes the detailed information for each of the interrupt sources. The 'Interrupt Address' indicates the address where the interrupt service routine is located. The 'Interrupt Flag' is the bit that notifies the MCU that the corresponding interrupt has occurred. 'Interrupt Enable' is the bit which decides whether each interrupt has been enabled. 'Interrupt Priority' is the bit which decides the priority of the interrupt. The 'Interrupt Number' is the interrupt priority fixed by the hardware. That is, when two or more interrupts having the same 'Interrupt Priority' value, occur simultaneously, the lower 'Interrupt Number' is processed first.

Table 6 – Interrupt Descriptions

Interrupt Number	Interrupt Type	Interrupt Address	Interrupt Flag	Interrupt Enable	Interrupt Priority
0	External Interrupt0	0003H	TCON.IE0	IE.EX0	IP.PX0
1	Timer0 Interrupt	000BH	TCON.TF0	IE.ET0	IP.PT0
2	External Interrupt1	0013H	TCON.IE1	IE.EX1	IP.PX1
3	Timer1 Interrupt	001BH	TCON.TF1	IE.ET1	IP.PT1
4	UART0 Interrupt (TX) UART0 Interrupt (RX)	0023H	***Note 1***	IE.ES0	IP.PS0
7	UART1Interrupt (TX) UART1 Interrupt (RX)	003BH	***Note 1***	IE.ES1	IP.PS1
8	PHY Interrupt	0043H	EXIF.PHYIF	EIE.RFIE	EIP.RFIP
9	Timer2 Interrupt	004BH	EXIF.T2IF	EIE.T2IE	EIP.T2IP
10	AES Interrupt	0053H	EXIF.AESIF	EIE.AESIE	EIP.AESIP
11	Timer3 Interrupt	005BH	EXIF.T3IF	EIE.T3IE	EIP.T3IP
12	Sleep Timer Interrupt	0063H	EICON.RTCIF	EIE.RTCIE	EIP.RTCIP
13	SPI Interrupt	0068H	***Note 2***	EIE.SPIIE	EIP.SPIIP
14	Voice Interrupt	0073H	***Note 3***	EIE.VCEIE	EIP.VCEIP

Note 1: *In the case of a UART Interrupt, bit [0] of the IIR register (0x2502, 0x2512) in the UART block is used as a flag. Also, the Tx, Rx, Timeout, Line Status and Modem Status interrupts can be distinguished by bit [3:1] value. For more detailed information, refer to the UART0/1 description in Section 1.7.6.*

Note 2: *In the case of an SPI interrupt, there is another interrupt enable bit in the SPI register besides EIE.SPIIE. In order to enable an SPI interrupt, both SPIE in the SPCR (0x2540) register and EIE.SPIIE should be set to '1. SPIF in the SPSR (0x2541) register acts as an interrupt flag.*

Note 3: *In case of a Voice interrupt, there are interrupt enable registers and interrupt flag registers in the voice block. The interrupt enable register are VTFINTENA (0x2770), VRFINTENA (0x2771) and VDMINTENA (0x2772). The interrupt flag register are VTFINTVAL (0x2776), VRFINTVAL (0x2777), and VDMINTVAL (0x2778). There are 24 interrupt sources. When both an interrupt enable signal and an interrupt flag signal are set to '1,' voice interrupt is enabled.*

Table 7 – INTERRUPT Registers

Bit	Name	Descriptions	R/W	Reset Value
		**IE (INTERRUPT ENABLE REGISTER, 0xA8)** The EA bit in the IE register is the global interrupt enable signal for all interrupts. In addition, each interrupt is masked by each interrupt enable bit. Therefore, in order to use an interrupt, both EA and the specific interrupt enable bit should be set to '1'. When the bit for each interrupt is '0', that interrupt is disabled. When the bit for each interrupt is '1', that interrupt is enabled.		
7	EA	Global interrupt enable 　0: No interrupt will be acknowledged. 　1: Each interrupt source is individually enabled or 　　 disabled by setting its corresponding enable bit.	R/W	0
6	ES1	UART1 interrupt enable 1: interrupt enabled.	R/W	0
5		Reserved		0
4	ES0	UART0 interrupt enable 1: interrupt enabled.	R/W	0
3	ET1	Timer1 interrupt enable 1: interrupt enabled.	R/W	0
2	EX1	External interrupt1 enable 1: interrupt enabled.	R/W	0
1	ET0	Timer0 interrupt enable 1: interrupt enabled.	R/W	0
0	EX0	External interrupt0 enable 1: interrupt enabled.	R/W	0
		IP (INTERRUPT PRIORITY REGISTER, 0xB8) If a bit corresponding to each interrupt is '0', the corresponding interrupt has lower priority and if a bit is '1', the corresponding interrupt has higher priority.		
7		Reserved		0
6	PS1	UART1 interrupt priority 1: UART1 interrupt has higher priority.	R/W	0
5		Reserved		0
4	PS0	UART 0 interrupt priority 1: UART0 interrupt has higher priority.	R/W	0
3	PT1	Timer1 interrupt priority 1: Timer1 interrupt has higher priority.	R/W	0
2	PX1	External interrupt1 interrupt priority 1: External interrupt1interrupt has higher priority.	R/W	0
1	PT0	Timer0 interrupt priority 1: Timer0 interrupt has higher priority.	R/W	0
0	PX0	External interrupt0 interrupt priority 1: External interrupt0 interrupt has higher priority.	R/W	0
		EIE (EXTENDED INTERRUPT ENABLE REGISTER, 0xE8) If a bit is '0', corresponding interrupt is disabled and if a bit is '1', corresponding interrupt is enabled. Refer to the following table.		
7		Reserved	R/W	0
6	VCEIE	Voice Interrupt Enable. 　0: Interrupt disabled 　1: Interrupt enabled	R/W	0
5	SPIIE	SPI Interrupt Enable 　0: Interrupt disabled 　1: Interrupt enabled	R/W	0
4	RTCIE	Sleep Timer Interrupt Enable 　0: Interrupt disabled 　1: Interrupt enabled	R/W	0
3	T3IE	Timer3 Interrupt Enable 　0: Interrupt disabled 　1: Interrupt enabled	R/W	0
2	AESIE	AES Interrupt Enable 　0: Interrupt disabled 　1: Interrupt enabled	R/W	0

Bit	Name	Descriptions	R/W	Reset Value

1	**T2IE**	Timer2 Interrupt Enable
		    0: Interrupt disabled
		    1: Interrupt enabled
			R/W	0

0	**RFIE**	RF Interrupt Enable
		    0: Interrupt disabled
		    1: Interrupt enabled
			R/W	0

EIP (EXTENDED INTERRUPT PRIORITY REGISTER, 0xF8)
If a bit is '0', the corresponding interrupt has lower priority. If a bit is '1', the corresponding interrupt has higher priority.

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved		0

6	**VCEIP**	Voice Interrupt Priority
		    1: Voice interrupt has higher priority.
		    0: Voice interrupt has lower priority.
			R/W	0

5	**SPIIP**	SPI Interrupt Priority
		    1:SPI interrupt has higher priority.
		    0:SPI interrupt has lower priority.
			R/W	0

4	**RTCIP**	Sleep Timer Interrupt Priority
		    1: Sleep Timer interrupt has higher priority.
		    0: Sleep Timer interrupt has lower priority.
			R/W	0

3	**T3IP**	Timer3 Interrupt Priority
		    1: Timer3 interrupt has higher priority.
		    0: Timer3 interrupt has lower priority.
			R/W	0

2	**AESIP**	AES Interrupt Priority
		    1: AES interrupt has higher priority.
		    0: AES interrupt has lower priority.
			R/W	0

1	**T2IP**	Timer2 Interrupt Priority
		    1: Timer2 interrupt has higher priority.
		    0: Timer2 interrupt has lower priority.
			R/W	0

0	**RFIP**	RF Interrupt Priority
		    1: RF interrupt has higher priority.
		    0: RF interrupt has lower priority.
			R/W	0

EXIF (EXTENDED INTERRUPT FLAG REGISTER, 0x91)
This register stores the interrupt state corresponding to each bit. When the interrupt corresponding to a bit is triggered, the flag is set to '1'.

Bit	Name	Descriptions	R/W	Reset Value
7	**T3IF**	Timer3 Interrupt Flag. 1: Interrupt pending	R/W	0
6	**AESIF**	AES Interrupt Flag. 1: Interrupt pending	R/W	0
5	**T2IF**	Timer2 Interrupt Flag. 1: Interrupt pending	R/W	0
4	**RFIF**	RF Interrupt Flag. 1: Interrupt pending	R/W	0
3:0		Reserved		0

EICON (EXTENDED INTERRUPT CONTROL REGISTER, 0xD8)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6:4		Reserved		0
3	**RTCIF**	Sleep Timer Interrupt Flag. 1: Interrupt pending	R/W	0
2:0		Reserved		0

1.6 POWER MANAGEMENT

There are three Power-Down modes in the ZIC2410. Each mode can be set by PDMODE [1:0] bits in PDCON (0x22F1) register and Power-Down mode can be started by setting PDSTART bit to 1. Each mode has a different current consumption and different wake-up sources. Table 8 describes the three Power-Down modes.

Table 8 – Power Down Modes

PDMODE [1:0]	Description	Wake-Up Source	Regulator for Digital block	Current
0	No power-down	-	-	-
1	PM1 mode	Hardware Reset, Sleep Timer interrupt, External interrupt	ON	25μA
2	PM2 mode	Hardware Reset, Sleep Timer interrupt, External interrupt	OFF (After wake-up, register configuration is required)	<2μA
3	PM3 mode	Hardware Reset, External interrupt	OFF (After wake-up, register configuration is required)	0.3μA

The following describes the time it takes from Power-Down mode to system operation for each of the wake-up sources.

① Hardware Reset Wake Up

Hardware Reset Wake Up time in PM1, PM2 and PM3 is around 1001μsec. For more detailed information, refer to the Figure 35.

② Sleep Timer Interrupt Wake Up

The following shows the timing of the Sleep Timer Interrupt Wake Up. As shown in Figure 9 below, the time of Power Down mode is set by register RTINT and register RTDLY should be set at greater than or equal to '0x11' in order to stabilize the crystal. In the case of PM1 and PM2,the minimum time until the system is operating after going into the Power Down mode, is around 534μsec (RTINT:0x01, RTDLY:0x11).
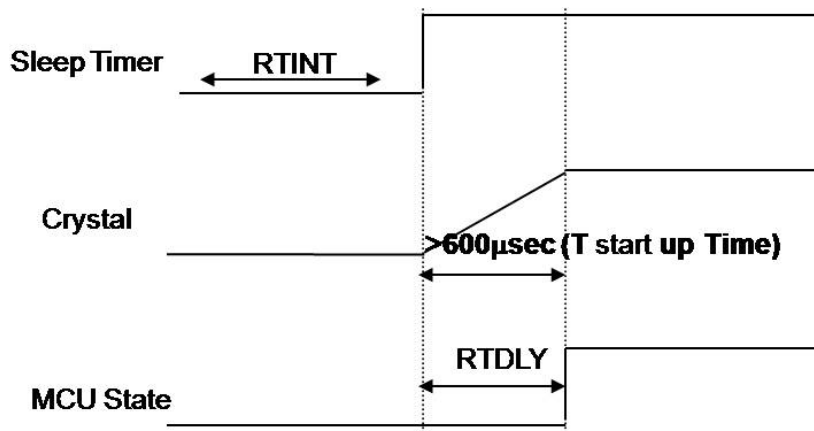
Figure 9 – Sleep Timer Interrupt: Wake Up Times

Based on the CEL' reference circuit.

③ External interrupt Wake Up

The following shows the time of External Interrupt Wake Up. The time, until system is operated, is different based on the releasing time of external interrupt. For example, external interrupt can be released before RTDLY minimum time or after RTDLY minimum time. By considering these two causes, it is recommended to set RTDLY to over 600μsec at least. In addition, Register RTDLY should be set over '0x11' at least to stabilize crystal.
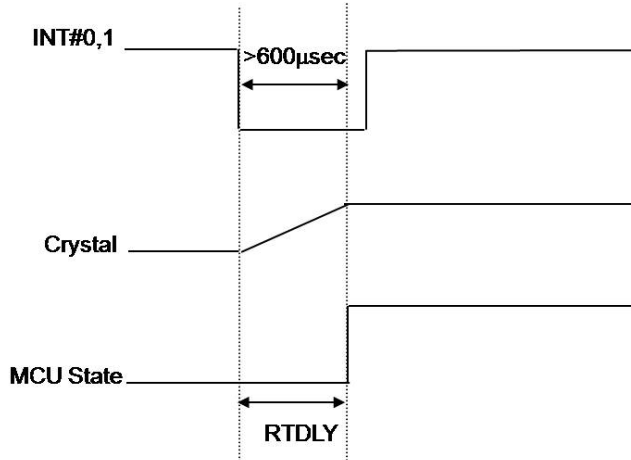

Figure 10 – External Timer Interrupt: Wake Up Times

Based on the CEL' reference circuit.

The following table describes the status of voltage regulator, oscillator, and sleep timer in normal mode (PM0) and each Power-Down mode.

Table 9 – Status in Power-Down Modes

Power Mode	AVREG	DVREG	Main OSC	Sleep Timer
PM0	ON	ON	ON	ON
PM1	OFF	ON	OFF	ON
PM2	OFF	OFF	OFF	ON
PM3	OFF	OFF	OFF	OFF

When exiting from a Power-Down mode initiated by a Sleep Timer interrupt, RTDLY (0x22F4) register specifies the delay time for oscillator stabilization. If the delay time is too short, the oscillator can become unstable and cause a problem of fetching a wrong instruction command in the MCU.

In addition, there are two Power-Down modes that can be only used in the MCU. One is PD (Power-Down) mode and the other is IDLE mode. PD (Power-Down) mode of MCU is enabled by setting PD in PCON register to '1'. In PD (Power-Down) mode, all the clocks of MCU are stopped and current consumption is minimized. When interrupt, which is allowed for wake-up, occurs, it exits from PD mode. After exiting, first, the corresponding interrupt service routine is executed. And then, the next instruction after the instruction for setting PD to '1' is executed.

In IDLE mode, clocks of all the blocks in the MCU except the peripherals are stopped. The current consumption is 2.7mA. When an interrupt occurs (except a timer interrupt or an external interrupt) the IDLE bit is cleared and the device exits from the IDLE mode. The required interrupt service routine is then executed and the next instruction (after the instruction setting IDLE to '1') is executed.

Table 10 – Power Control Registers

Bit	Name	Descriptions	R/W	Reset Value
PCON (POWER CONTROL REGISTER, 0x87)				
7:2		Reserved		0
1	**PD**	Power-down Mode. When this field is set to '1', all the clocks in MCU are stopped.	R/W	0
0	**IDLE**	Idle Mode. When this field is set to '1', all the clocks in MCU except peripherals are stopped. Only peripherals operate normally.	R/W	0

When ZIC2410 goes into Power-Down mode by setting PDSTART field of PDM register, PD bit of PCON register should also be set. To go into PD (Power-Down) mode, PDMODE field should be set as 1, 2, or 3. After that, PD bit of PCON register should be set to 1 by the following instruction that set PDMODE. For more detailed information, please refer to the Figure 11.
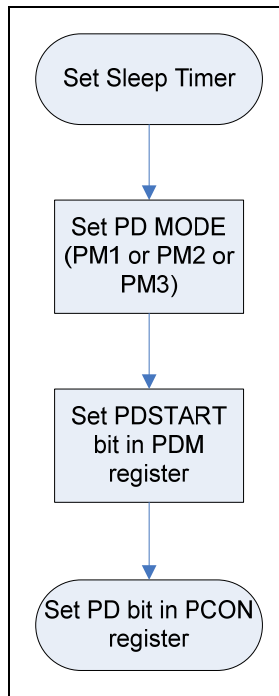
Figure 11 – Power-Down mode setting procedure

1.7 ON-CHIP PERIPHERALS

On-chips peripherals in ZIC2410 are as follows.

- TIMER 0/1   1.7.1
- TIMER 2/3,PWM 2/3   1.7.2
- Watch-dog timer   1.7.3
- Sleep Timer   1.7.4
- Internal RC Oscillator for Sleep Timer   1.7.5
- Two High-Speed UARTs with Two 16-byte FIFOs (up to 1Mbps)   1.7.6
- SPI Master/Slave Interface   1.7.7
- I2S/PCM Interface with two128-byte FIFOs   1.7.8.1
- µ-law / a-law / ADPCM Voice Codec   1.7.8.2
- Random Number Generator   1.7.9
- Quad Decoder   1.7.10
- Internal Voltage Regulator   1.7.11
- 4-channel 8-bit sensor ADC   1.7.12
- On-chip Power-on-Reset   1.7.13
- Temperature Sensor   1.7.14
- Battery Monitoring   1.7.15

1.7.1 TIMER 0/1

The Embedded MCU has two 16-bit timers which are compatible with Intel 8051 MCU (Timer0, Timer1). These timers have 2 modes: one is operated as a timer and the other is operated as a counter. When it is operated as a timer, there are 4 operating modes.

Each timer is a 16-bit timer and consists of two 8-bit register. Therefore, the counter can be either 8-bit or 16-bit set by the operating mode.

In counter mode, the input signal T0 (P3.4) and T1 (P3.5) are sampled once every 12 cycles of the system clock. If the sampled value is changed from '1' to '0', the internal counter is incremented. In this time, the duty cycle of T0 and T1 doesn't affect the increment. Timer0 and Timer1 are accessed by using 6 SFR's.

These registers are used to control each timer function and monitor each timer status.

The following table describes timer registers and modes.

Table 11 – Timer and Timer Mode Registers

Bit	Name	Descriptions	R/W	Reset Value
TCON (TIMER CONTROL REGISTER, 0x88)				
7	TF1	**Timer1 Overflow Flag**: When this field is '1', a Timer1 interrupt occurs. After the Timer1 interrupt service routine is executed, this field value is cleared by the hardware.	R/W	0
6	TR1	**Timer1 Run Control**: When this bit is set to '1', Timer1 is enabled.	R/W	0
5	TF0	**Timer0 Interrupt Flag**: When this field is '1': Interrupt is pending After Timer0 interrupt service routine is executed, this field is cleared by hardware.	R/W	0
4	TR0	**Timer0 Run**: When this bit is set to '1', Timer0 is enabled.	R/W	0
3	IE1	**External Interrupt1 Edge Flag**: When this field is '1', External interrupt1 is pending. After the interrupt service routine is executed, this field is cleared by hardware.	R/W	0

Bit	Name	Descriptions	R/W	Reset Value

2	IT1	**External Interrupt1 Type Control**: This field specifies the type of External interrupt1.
		  1 = **Edge type**. When the falling edge of INT1 is detected, the interrupt occurs.
		  0 = **Level type**. When INT1 is low, the interrupt occurs.
			R/W	0

1	IE0	**External Interrupt0 Edge Flag**: When this field is '1', External interrupt0 is pending. After the interrupt service routine is executed, this field is cleared by hardware.	R/W	0

0	IT0	**External Interrupt0 Type Control**: This field specifies the type of External interrupt1.
		  1 = **Edge type**. When the falling edge of INT1 is detected, the interrupt occurs.
		  0 = **Level type**. When INT0 is low, the interrupt occurs.
			R/W	0

TMOD (TIMER MODE CONTROL REGISTER, 0x89)

Bit	Name	Descriptions	R/W	Reset Value
7	GATE1	**Timer Gate Control**: When TR1 is set to '1' and GATE1 is '1', Timer1 is enabled while INT1 pin is in high. When GATE1 is set to '0' and TR1 is set to '1', Timer1 is enabled	R/W	0
6	CT1	**Timer1 Counter Mode Select**: When this field is set to '1', Timer1 is enabled as counter mode.	R/W	0

5:4	M1	**Timer1 mode select**:.
		  0: Mode0, 12-bit Timer
		  1: Mode1, 16-bit Timer
		  2: Mode2, 8-bit Timer with auto-load
		  3: Mode3, two 8-bit Timer
			R/W	0

3	GATE0	**Timer0 Gate Control**: When TR0 is set to '1' and GATE0 is '1', Timer0 is enabled while INT0 pin is in high. When GATE1 is set to '0' and TR1 is set to '1', Timer0 is enabled	R/W	0
2	CT0	When this field is set to '1', Timer0 is enabled as counter mode.	R/W	0

1:0	M0	**Timer0 Mode Select**:
		  0: Mode0, 12-bit Timer
		  1: Mode1, 16-bit Timer
		  2: Mode2, 8-bit Timer with auto-load
		  3: Mode3, two 8-bit Timer
			R/W	0

TL0/TL1/TH0/TH1 (TIMER REGISTERS, 0x8A, 0x8B, 0x8C, 0x8D)
Two pairs of registers, (TH0, TL0) and (TH1, TL1), can be used as 16-bit timer register for Timer0 and Timer1 or can be used as 8-bit register respectively.

Bit	Name	Descriptions	R/W	Reset Value
7:0	TH0	Timer0 High Byte Data	R/W	0x00
7:0	TL0	Timer0 Low Byte Data	R/W	0x00
7:0	TH1	Timer1 High Byte Data	R/W	0x00
7:0	TL1	Timer1 Low Byte Data	R/W	0x00

In mode0, the 12-bit register of timer0 consists of 7-bit of TH0 and the lower 5-bit of TL0. The higher 1-bit of TH0 and higher 3-bit of TL0 are disregarded. When this 12-bit register is overflowed, set TF0 to '1'. The operation of timer1 is same as that of timer0.
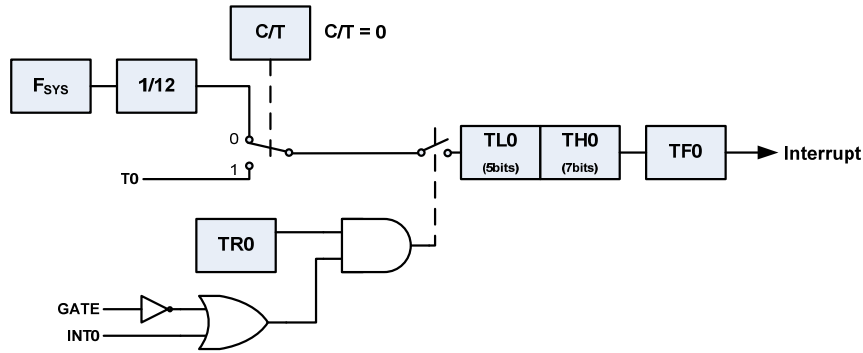
Figure 12 – Timer0 Mode0

In Mode1, the operation is same as it of Mode0 except all timer registers are enabled as a 16-bit counter.
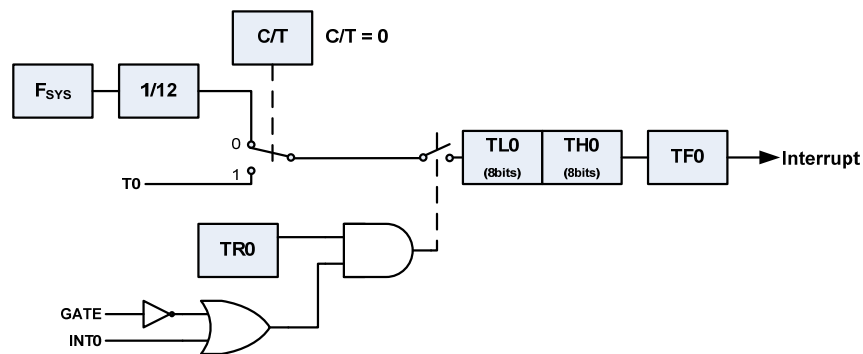

Figure 13 – Timer0 Mode1

In mode2, TL0 of Timer0 is enabled as an 8-bit counter and TH0 reloads TL0 automatically.

TF0 is set to '1' by overflowing of TL0. TH0 value retains the previous value regardless of the reloading. The operation of Timer1 is same as that of Timer0.
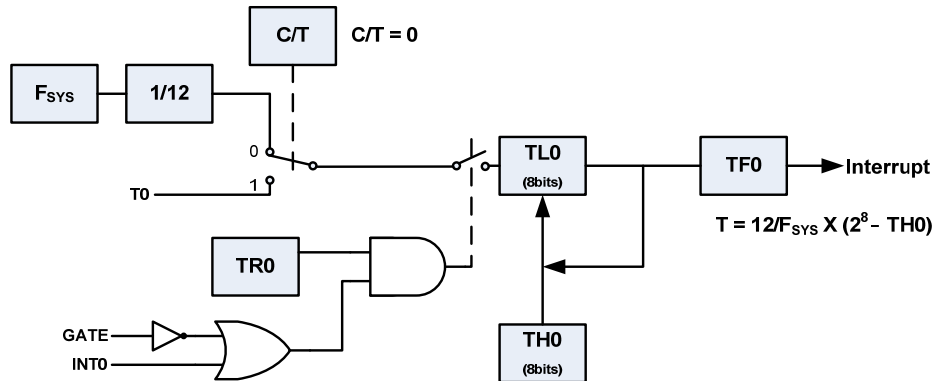

$$T = 12/F_{SYS} \times (2^8 - TH0)$$

Figure 14 – Timer0 Mode2

In Mode3, Timer0 uses TL0 and TH0 as an 8-bit timer respectively. In other words, it uses two counters. TL0 controls as the control signals of Timer0. TH0 is always used as a timer function and it controls as TR1 of Timer1. The overflow is stored in TF1. At this time, Timer1 is disabled and it retains the previous value.
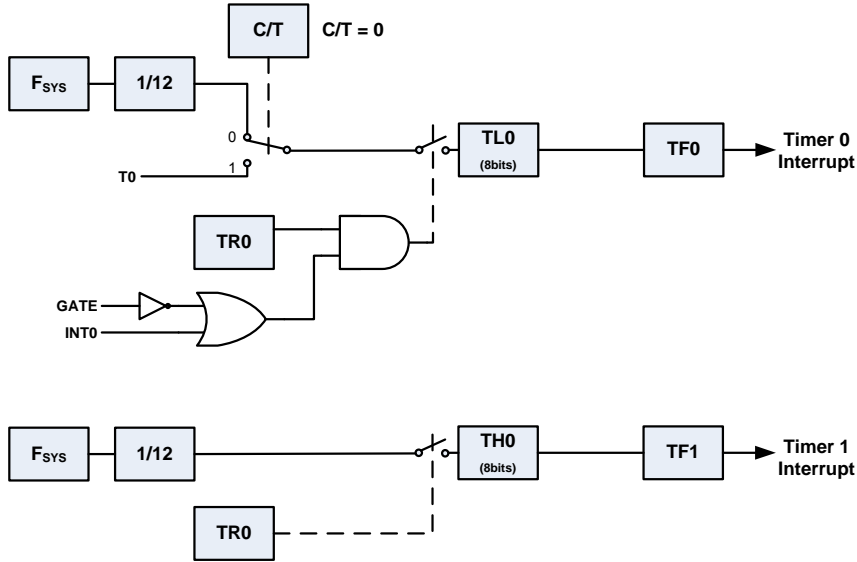
Figure 15 – Timer0Mode3

1.7.2 TIMER 2/3, Pulse Width Modulator (PWM) 2/3

TIMER 2/3

The embedded MCU includes two 16-bit timers (Timer 2 and Timer 3).

Table 12 – Timer 2 and Timer 3 Registers

<u>Bit</u>	<u>Name</u>	<u>Descriptions</u>	<u>R/W</u>	<u>Reset Value</u>
T23CON (TIMER2/3 CONTROL REGISTER, 0xA9)				
This register is used to control Timer2 and Time3.				
7:4		Reserved	R/W	0
3	TR3	**Timer3 Run**: When this field is set to '1', Timer3 is operational.	R/W	0
2	M3	**Timer3 PWM Mode**: When this field is set to '1', Timer3 is put into PWM mode.	R/W	0
1	TR2	**Timer2 Run**: When this field is set to '1', Timer2 is operational.	R/W	0
0	M2	**Timer2 PWM Mode**: When this field is set to '1', Timer2 is put into PWM mode.	R/W	0
TL2/TL3/TH2/TH3 (TIMER2/3 TIMER REGISTER, 0xAC, 0xAD, 0xAA, 0xAB)				
Register (TH2, TL2) and (TH3, TL3) are 16-bit timer counter register for Timer2 and Timer3.				
7:0	TH2	Timer2 High Byte Data	R/W	0x00
7:0	TL2	Timer2 Low Byte Data	R/W	0x00
7:0	TH3	Timer3 High Byte Data	R/W	0x00
7:0	TL3	Timer3 Low Byte Data	R/W	0x00

Timer2 acts as a general 16-bit timer. Time-out period is calculated by Equation 1.

Equation 1 – Time-out Period Calculation (Timer2)

$$T_2 = \frac{8 \times (256 \times TH2 + TL2 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupts will occur causing abnormal operation of the system. It is recommended to set a sufficient time-out period for Timer2 (> 100µs).

Timer3 acts as a general 16-bit timer. Time-out period of Timer3 is calculated by Equation 2.

Equation 2 – Time-out Period Calculation (Timer3)

$$T_3 = \frac{3 \times (256 \times TH3 + TL3 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupts will occur causing abnormal operation of the system. It is recommended to set a sufficient time-out period for Timer3.

PWM 2/3
TIMER 2/3 can be used as Pulse Width Modulators, PWM2 and PWM3 respectively based on setting the M2, M3 bits in T23CON register. P 3.6 outputs PWM2 signal and P3.7 outputs PWM3 signal

The following table describes the frequency and High Level Duty Rate in PWM mode.

Table 13 – Frequency and Duty Rate in PWM Mode

Channel	Frequency (Hz)	High Level Duty Rate (%)
PWM2	$\dfrac{fsystem}{256 \times (TH2+1)}$	$\dfrac{TL2}{256} \times 100$
PWM3	$\dfrac{fsystem}{256 \times (TH3+1)}$	$\dfrac{TL3}{256} \times 100$

Note: This equation does not apply for TH values of 0, and 1. For these values the frequency should be as follows: TH=0: 15.625 KHz; TH=1: 7.812 KHz.

1.7.3 WATCHDOG TIMER

The Watchdog Timer (WDT) monitors whether the MCU is or is not operating normally. If a problem occurs, the WDT will immediately reset the MCU.

In fact, when the system does not clear the WDT counter value, WDT considers that a problem has occurred, and therefore, resets the MCU automatically. The WDT is used when a program is not completed normally because a software error has been caused by the environment such as electrical noise, unstable power or static electricity.

When Powered-up, the internal counter value of WDT is set to '0' and watchdog timer is operated. If overflow is caused in the internal counter, a system reset is initiated with a timeout period is about 0.5 second. A user may reset the WDT by clearing WDTEN bit of WDTCON. When WDT is operating, an application program must clear the WDT periodically to prevent the system from being reset unwantedly.

Table 14 – Watchdog Timer Register

Bit	Name	Descriptions	R/W	Reset Value
WDTCON (WATCHDOG TIMER CONTROL REGISTER, 0xD2)				
7:5		Reserved	R/W	0
4	**WDTWE**	**WDT Write Enable**: To set WDTEN to '1', this field should be set to '1'.	R/W	0
3	**WDTEN**	**WDT Enable**: To use WDT, this bit should be set to '1'.	R/W	0
2	**WDTCLR**	**WDT Clear**: Watchdog Timer resets a system when the internal counter value is reached to the defined value by WDTPRE value. This field does not allow system to be reset by clearing the internal counter. When this field is set to '1', this field value is cleared automatically.	R/W	0
1:0	**WDTPRE**	**Watchdog Timer Prescaler**: Sets the prescaler value of WDT.	R/W	0

Reset interval of WDT is calculated by the Equation 3. For example, when WDTPRE value is '0' and system clock of MCU is 8MHz, reset interval of WDT is 65.536ms.

Equation 3 – Watchdog Reset Interval Calculation

$$\text{Watchdog Reset Interval} = \frac{256 \times 2^{(11+WDTPRE)}}{f_{system}}$$

1.7.4 SLEEP TIMER

The Sleep Timer can generate time interval such as 1 or 2 seconds with a 32.768 KHz clock source. The Sleep Timer (ST) is used to exit from the Power-Down mode.

The clock source desired can be generated from an external crystal or the internal RC oscillator.

ST is activated as setting RTEN bit to '1' and the interrupt interval can be programmed by setting RTCON [6:0], RTINT1 and RTINT0 register.

Table 15 – Sleep Timer Registers

Bit	Name	Descriptions	R/W	Reset Value
RTCON (SLEEP TIMER CONTROL REGISTER, 0x22F5)				
7	**RTCSEL**	**Sleep Timer Select**: When this field is set to '1', internal RCOSC is used as a clock source. When this field is set to '0', external 32.768KHz crystal is used as a clock source. When this field is set to '0' and external crystal is not turned on, ST does not act.	R/W	1
6:0	**RTINT [22:16]**	This field determines ST interrupt interval with RTINT0 and RTINT1	R/W	0x00
RTINT1 (SLEEP TIMER INTERRUPT INTERVAL 1, 0x22F6)				
7:0	**RTINT [15:8]**	This field determines the ST interrupt interval with RTINT0 and RTCON [6:0]	R/W	0x00
RTINT0 (SLEEP TIMER INTERRUPT INTERVAL 0, 0x22F7)				
7:0	**RTINT [7:0]**	This field determines ST interrupt interval with RTINT1 and RTCON [6:0]	R/W	0x08

Sleep Timer Interrupt Interval

RTCON [6:0], RTINT1 and RTINT0 register represent RTINT [22:0] (23-bit) and the timer interval is determined by this value. If ST clock source acts as 32.786KHz, one ST cycle is 1/32768 second and the timer interval is RTINT * (1/32768) second. Therefore, ST interrupt occurs per (RTINT * 30.5) µs and maximum is 256 second.

RTDLY (SLEEP TIMER DELAY REGISTER, 0x22F4)

This register is used when the MCU exits from a power-down state initiated by the ST interrupt.

RTDLY specifies the delay time for oscillator stabilization. When the MCU exits from power-down mode, the MCU executes the next instruction after the delay time.

Table 16 – Sleep Timer Delay Registers

Bit	Name	Descriptions	R/W	Reset Value
7:0	**RTDLY**	Delay Time = RTDLY $\times$ 4 / 32.768KHz when ST clock source is 32.768KHz. The value of RTDLY should be greater than 2.	R/W	0x11

1.7.5 INTERNAL RC OSCILLATOR

An Internal RC oscillator generates the internal clock and provides the clock to Sleep Timer block in the embedded MCU. The Internal RC oscillator can be controlled by the 3rd bit in the PDCON (0x22F1) register. When this bit is set to '1', internal RC Oscillator is enabled. The default value is '1'.
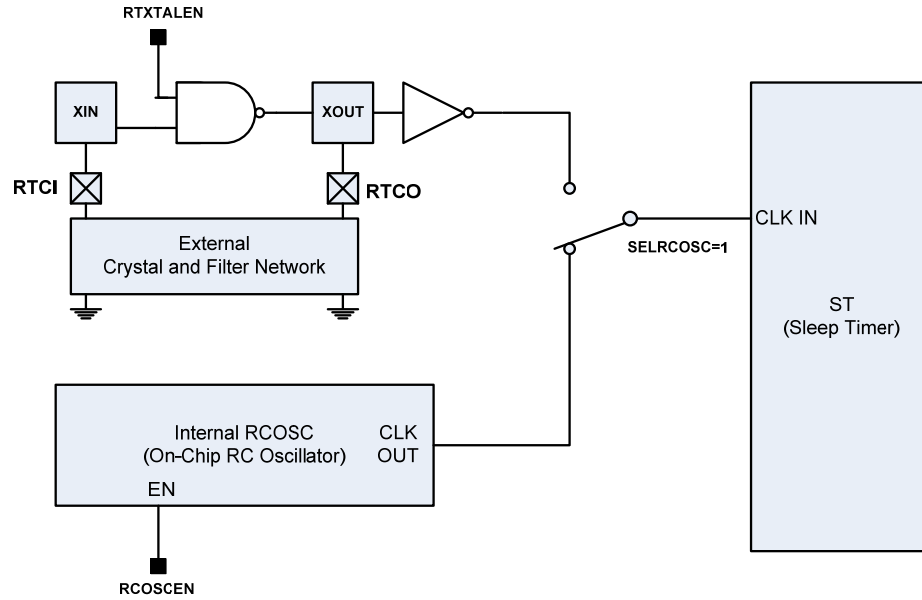
Figure 16 – Selecting the Clock Oscillator

1.7.6 UART0/1

Serial communication is categorized as synchronous mode or asynchronous mode in terms of its data transmission method.

The embedded MCU has both UART0 and UART1 to enable two-way communication.

These devices support asynchronous mode. The following registers are used to control UART.

Table 17 – UART0 Registers

Bit	Name	Descriptions	R/W	Reset Value
RBR (UART0 RECEIVE BUFFER REGISTER, 0x2500)
7:0	**RBR**	Read the received data	R/O	0x00
THR (UART0 TRANSMITTER HOLDING REGISTER, 0x2500)
7:0	**THR**	This register stores the data to be transmitted. The address is the same as the RBR register. When accessing this address, received data (RBR) is read and the data to be transmitted is stored.	W/O	0x00
DLL (UART0 DIVISOR LSB REGISTER, 0x2500)
7:0	**DLL**	This register can be accessed only when the DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLM register (below) occupying the lower 8 bits. This full 16-bit register is used to divide the clock.	R/W	0x00
*Note: After the data is written to the DLM register, it should be written in this register. When the data is written to DLL register, the clock divisor begins. Baud rate is calculated by the following equation.*   Baud rate = clock_speed / (7 × divisor_latch_value)
IER (UART0 INTERRUPT ENABLE REGISTER, 0x2501)
7:4		Reserved		0
3	**EDSSI**	Enable MODEM Status Interrupt. When this field is set to '1', Modem status interrupt is enabled.	R/W	0
2	**ELSI**	Enable Receiver Line Status Interrupt.	R/W	0
1	**ETBEI**	Enable Transmitter Holding Register Empty Interrupt	R/W	0
0	**ERBEI**	Enable Received Data Available Interrupt	R/W	0
DLM (UART0 DIVISOR LATCH MSB REGISTER, 0x2501)
7:0	**DLM**	This register can be accessed only when the DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLL register (above) occupying the higher 8 bits. This full 16-bit register is used to divide the clock.	R/W	0x00
IIR (UART0 INTERRUPT IDENTIFICATION REGISTER, 0x2502)
7:4		Reserved	R/O	0
3:1	**INTID**	Interrupt Identification. Refer to the Table 18.	R/O	0
0	**PENDING**	Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending.	R/O	1
*Note: IIR register uses the same address as FCR register in Table 19 below. IIR register is read-only and FCR register is write-only.*

Table 18 – UART0 Interrupt Lists

INTID	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
011	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the LSR (Line Status Register).
010	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
110	2nd	Timeout Indication	There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times.	Reading from the FIFO (Receiver Buffer Register)
001	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR
000	4th	Modem Status	CTS, DSR, RI or DCD	Reading the Modem status register

Table 19 – UART0 Control Registers

Bit	Name	Descriptions	R/W	Reset Value
FCR (UART0 FIFO CONTROL REGISTER, 0x2502)				
Note: FCR register uses the same address as IIR register in Table 17 above. IIR register is read-only and FCR register is write-only.				
7:6	URXFTRIG	**Trigger Level of Receiver FIFO**. Interrupt occurs when FIFO receives the the number of data bytes based on this field's value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 bytes. 0: 1byte 1: 4 bytes 2: 8 bytes 3: 14 bytes	W/O	3
5:3		Reserved	W/O	0
2	UTXFRST	When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset.	W/O	0
1	URXFRST	When this field is set to '1', Receiver FIFO is cleared and the circuits related to it are reset.	W/O	0
0		Reserved	W/O	0
LCR (UART0 LINE CONTROL REGISTER, 0x2503)				
7	DLAB	**Divisor Latch Access Enable**. When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed.	R/W	0
6	SB	**Set Break**. When this field is set to '1', serial output is forced to be '0' (break state)	R/W	0
5	SP	**Stick Parity**. When PEN and EPS are '1' with this field set to '1', a parity of '0' is transmitted. In reception mode, it checks whether parity value is '0' or not. When PEN is '1' and EPS is '0' with this field is to '1', parity of '1', is transmitted. In reception mode, it checks whether parity value is '1' or not.	R/W	0
4	EPS	**Even Parity Enable**. When this field is set to '1', parity value is even. When set to '0', parity value is odd.	R/W	0
3	PEN	**Parity Enable**. When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated.	R/W	0

Bit	Name	Descriptions	R/W	Reset Value
2	STB	**Number of Stop Bits**. When this field is set to '1', 2 stop bit is used. When transmitting a word (character) of 5 bit length, 1.5 stop bit is used. When this field is '0', 1 stop bit is used.	R/W	0
1:0	WLS	**Word Length Select**. 0: 5bit Word 1: 6bit Word 2: 7bit Word 3: 8bit Word	R/W	3

There are more registers such as the Modem Control Register, the Line Status Register, the Modem Status Register and the Port Enable Register in the UART0 block. This document doesn't include these registers because they are not commonly used. For more detailed information on their use, please contact CEL.

The following registers are to control UART1.

Table 20 – UART1 Registers

Bit	Name	Descriptions	R/W	Reset Value
RBR (UART1 RECEIVE BUFFER REGISTER, 0x2510)				
7:0	RBR	Read the received data	R/O	0x00
THR (UART1 TRANSMITTER HOLDING REGISTER, 0x2510)				
7:0	THR	This register stores the data to be transmitted. The address is the same as the RBR register. When accessing this address, received data (RBR) is read and the data to be transmitted is stored.	W/O	0x00
DLL (UART1 DIVISOR LSB REGISTER, 0x2510)				
7:0	DLL	This register can be accessed only when the DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLM register (below) occupying the lower 8 bits. This full 16-bit register is used to divide the clock.	R/W	0x00
Note: After the data is written to the DLM register, it should be written in this register. When the data is written to DLL register, the clock divisor begins. Baud rate is calculated by the following equation. Baud rate = clock_speed / (7 × divisor_latch_value)				
IER (UART1 INTERRUPT ENABLE REGISTER, 0x2511)				
7:4		Reserved		0
3	EDSSI	Enable MODEM Status Interrupt. When this field is set to '1', Modem status interrupt is enabled.	R/W	0
2	ELSI	Enable Receiver Line Status Interrupt.	R/W	0
1	ETBEI	Enable Transmitter Holding Register Empty Interrupt	R/W	0
0	ERBEI	Enable Received Data Available Interrupt	R/W	0
DLM (UART1 DIVISOR LATCH MSB REGISTER, 0x2511)				
7:0	DLM	This register can be accessed only when the DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLL register (above) occupying the higher 8 bits. This full 16-bit register is used to divide the clock.	R/W	0x00
IIR (UART1 INTERRUPT IDENTIFICATION REGISTER, 0x2512)				
7:4		Reserved	R/O	0
3:1	INTID	Interrupt Identification. Refer to the Table 21.	R/O	0
0	PENDING	Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending.	R/O	1
Note: IIR register uses the same address as FCR register in Table 22 *below. IIR register is read-only and FCR register is write-only.*				

Table 21 – UART1 Interrupt Lists

INTID	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
011	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the LSR (Line Status Register).
010	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
110	2nd	Timeout Indication	There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times.	Reading from the FIFO (Receiver Buffer Register)
001	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR
000	4th	Modem Status	CTS, DSR, RI or DCD	Reading the Modem status register

Table 22 – UART1 Control Registers

Bit	Name	Descriptions	R/W	Reset Value
FCR (UART1 FIFO CONTROL REGISTER, 0x2512)				
Note: FCR register uses the same address as IIR register in Table 20 above. IIR register is read-only and FCR register is write-only.				
7:6	URXFTRIG	**Trigger Level of Receiver FIFO**. Interrupt occurs when FIFO receives the the number of data bytes based on this field's value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 bytes. 　　0: 1byte 　　1: 4 bytes 　　2: 8 bytes 　　3: 14 bytes	W/O	3
5:3		Reserved	W/O	0
2	UTXFRST	When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset.	W/O	0
1	URXFRST	When this field is set to '1', Receiver FIFO is cleared and the circuits related to it are reset.	W/O	0
0		Reserved	W/O	0
LCR (UART1 LINE CONTROL REGISTER, 0x2513)				
7	DLAB	**Divisor Latch Access Enable**. When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed.	R/W	0
6	SB	**Set Break**. When this field is set to '1', serial output is forced to be '0' (break state)	R/W	0
5	SP	**Stick Parity**. When PEN and EPS are '1' with this field set to '1', a parity of '0' is transmitted. In reception mode, it checks whether parity value is '0' or not. When PEN is '1' and EPS is '0' with this field is to '1', parity of '1', is transmitted. In reception mode, it checks whether parity value is '1' or not.	R/W	0
4	EPS	**Even Parity Enable**. When this field is set to '1', parity value is even. When set to '0', parity value is odd.	R/W	0
3	PEN	**Parity Enable**. When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated.	R/W	0
2	STB	**Number of Stop Bits**. When this field is set to '1', 2 stop bit is used. When transmitting a word (character) of 5 bit length, 1.5 stop bit is used. When this field is '0', 1 stop bit is used.	R/W	0

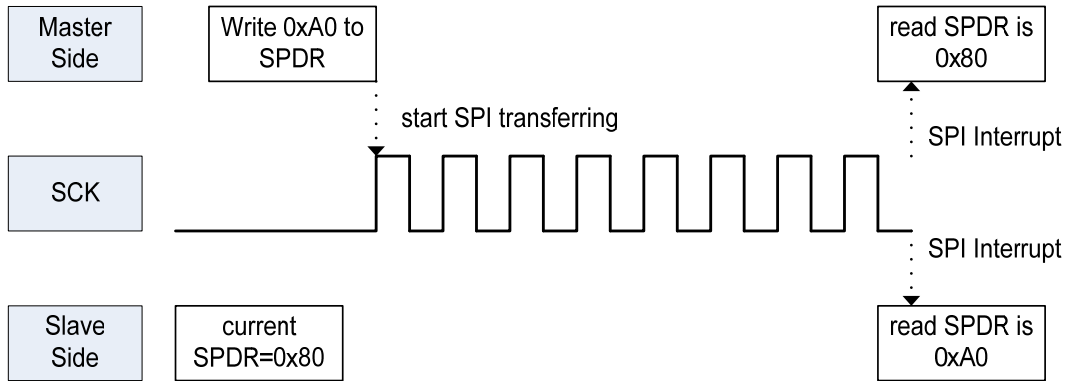| Bit	Name	Descriptions	R/W	Reset Value
1:0	**WLS**	**Word Length Select**. 0: 5bit Word 1: 6bit Word 2: 7bit Word 3: 8bit Word	R/W	3

There are more registers such as the Modem Control Register, the Line Status Register, the Modem Status Register and the Port Enable Register in the UART1 block. This document doesn't include these registers because they are not used commonly. For more detailed information on their use, please contact CEL.

1.7.7   SPI MASTER/SLAVE

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The operation is different in either Master mode or Slave mode

In the Master mode, the data transmission is done by writing to the SPDR (SPI Data Register, 0x2542). After transmission, data reception is initiated by a byte transmitted to the Slave device from the Master SPI clock. When the SPI interrupt occurs, the value of the SPDR register becomes the received data from the SPI slave device. Even though the SPDR TX and RX have the same address, no data collision occurs because the processes of writing and reading data happen sequentially.

In the Slave mode, the data must be ready in the SPDR when the Master calls for it. Data transmission is accomplished by writing to the SPDR before the SPI clock is generated by the Master. When the Master generates the SPI clock, the data in the SPDR of the Slave is transferred to the Master. If the SPDR in the Slave is empty, no data exchange occurs. Data reception is done by reading the SPDR when the next SPI interrupt occurs.

Figure 17 – SPI Data Transfer

Table 23 – SPI Control Registers

Bit	Name	Descriptions	R/W	Reset Value
SPCR (SPI CONTROL REGISTER, 0x2540)				
7	SPIE	**SPI Interrupt Enable**. When this field is set to '1', SPI interrupt is enabled.	R/W	0
6	SPE	**SPI Enable**. When this field is set to '1', SPI is enabled.	R/W	0
5		Reserved		0
4	MSTR	**Master Mode Select**. When this field is set to '1', a Master mode is selected.	R/W	1
3	CPOL	**Clock Polarity**. If there is no data transmission while this field is set to '0', SCK pin retains '0'. If there is no data transmission while this field is set to '1', SCK pin retains '1'. This field is used to set the clock and data between a Master and Slave with CPHA field. Refer to information below for a more detailed explanation.	R/W	0
2	CPHA	**Clock Phase**. Used to set the clock and data between a Master and Slave with CPOL field. See details below.	R/W	0
1:0	SPR	**SPI Clock Rate Select**. With ESPR field in SPER register (0x2543), selects SPI clock (SCK) rate when the device is configured as a Master. Refer to the ESPR field in Table 25.	R/W	0

There are four methods of data transfer based on the settings of CPOL and CPHA. Polarity of SPI serial clock (SCK) is determined by CPOL value and it determines whether SCK activates high or low.

If CPOL value is '0', SCK pin retains '0' during no data transmission. If CPOL value is '1', SCK pin retains '1' during no data transmission. CPHA field determines the format of data to be transmitted.

Table 24 describes the clock polarity and the data transition timing.

Table 24 – Clock Polarity and Data Transition Timing

CPOL	CPHA	SCK when idle	Data Transition Timing
0	0	Low	Falling Edge of SCK
0	1	Low	Rising Edge of SCK
1	0	High	Rising Edge of SCK
1	1	High	Falling Edge of SCK

Figure 18, Figure 19, Figure 20, and Figure 21 describe this block when slave mode is selected. When the values of CPOL and CPHA are the same, (a) and (d) below, output data is changed at the falling edge of SCK. Input data is captured at the rising edge of SCK. When the CPOL and CPHA values are different, (b) and (c) below, output data is changed at the rising edge of received SCK. Input data is captured at the falling edge of SCK.
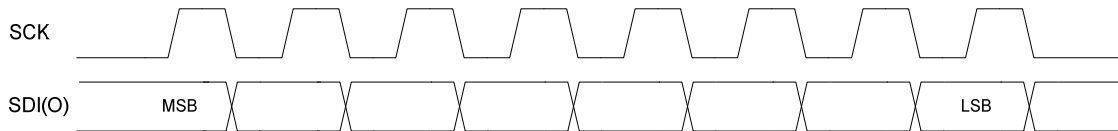
Figure 18 – (a) CPOL=0, CPHA=0
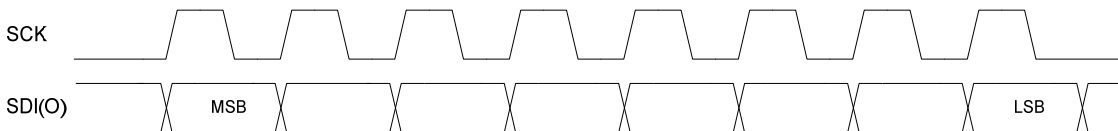
Figure 19 – (b) CPOL=0, CPHA=1
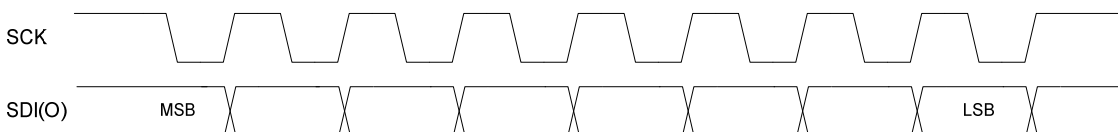
Figure 20 – (c) CPOL=1, CPHA=0
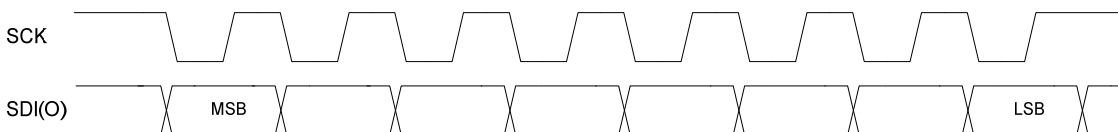
Figure 21 – (d) CPOL=1, CPHA=1

Table 25 – SPI Registers

Bit	Name	Descriptions	R/W	Reset Value
SPSR (SPI STATUS REGISTER, 0x2541)				
7	SPIF	**SPI Interrupt Flag:** When SPI interrupt occurs, this field is set to '1'. Set whenever data transmission is finished and it can be cleared by software.	R/W	0

Bit	Name	Descriptions	R/W	Reset Value
6	WCOL	**Write Collision:** Set to '1' when writing data to the SPDR register while SPITX FIFO is full. It can be cleared by software.	R/W	0
5:4		Reserved		0
3	WFFUL	**Write FIFO Full**: Set to '1' when Write FIFO is full. This field is read only.	R/O	0
2	WFEMPTY	**Write FIFO Empty**: Set to '1' when Write FIFO is cleared. This field is read only.	R/O	1
1	RFFUL	**Read FIFO Full**: Set to '1' when Read FIFO is full. This field is read only.	R/O	0
0	RFEMPTY	**Read FIFO Empty**: Set to '1' when Read FIFO is cleared. This field is read only.	R/O	1
SPDR (SPI DATA REGISTER, 0x2542)				
7:0	SPDR	This register is read/write buffer.	R/W	-
SPER (SPI E REGISTER, 0x2541)				
7:6	ICNT	**Interrupt Count.** Indicates the number of byte to transmit. SPIF bit is set to '1' whenever each byte is transmitted.	R/W	0
5:2		Reserved		0
1:0	ESPR	**Extended SPI Clock Rate Select**. With SPR field in SPCR Register (0x2540), this field selects SPI clock (SCK) rate when a device is configured as a Master. {ESPR, SPR} / (System Clock Divider): 0000 — Reserved 0001 — Reserved 0010 — 8 0011 — 32 0100 — 64 0101 — 16 0110 — 128 0111 — 256 1000 — 512 1001 — 1024 1010 — 2048 1011 — 4096 * ESPR field : high bit SPR field: low bit	R/W	2

The value of ESPR and SPR is used to divide system clock to generate SPI clock (SCK).

For example, if the value of ESPR and SPR is '0010' and system clock is 8MHz, SPI clock (SCK) is 1MHz.

1.7.8   VOICE

A voice function includes the following:

- ■ I2S Interface   1.7.8.1
- ■ Voice CODEC (u-law / a-law / ADPCM)   1.7.8.2
- ■ Voice FIFO   1.7.8.3
- ■ DMA   1.7.8.3

The data generated through an external ADC is input to the voice block in the ZIC2410 via an I2S interface. Data received via I2S is compressed at the voice codec, and stored in the Voice TXFIFO. The data is then transferred to the MAC TX FIFO through DMA operation and finally transmitted through the PHY layer.

By contrast, received data in the MAC RX FIFO is transferred to the Voice RXFIFO and decompressed in the voice codec. It is finally transferred to an external DAC via I2S interface.

I2S is commonly used for transferring/receiving voice data. Voice data can be transferred or received via SPI or UART interface as well.

Voice codec supports u-law, a-law and ADPCM methods.

If the voice codec function is not needed, it can be bypassed.

1.7.8.1   I2S

In I2S interface, data is transferred MSB first from the left channel, and then from the right channel. There are two ways to send data via I2S TX: writing data to the register either by software, or by hardware. This is enabled by using the POP field in STXMODE (0x252d). Similarly, there are two ways to receive data via I2S RX: the first is reading the register by software, and the other is by the PUSH field in SRXMODE (0x253d)

There are four modes in I2S interface as follows.

- • I2S mode
- • Left Justified mode
- • Right Justified mode
- • DSP mode

In I2S mode, left channel data is transferred in order. When left channel data is transferred, LRCK value is '0' and when right channel data is transferred, LRCK value is 0. Transferred data and LECK is changed at the falling edge. Refer to Figure 22 (a) below.

In Left Justified mode, left channel data is transferred whenever LRCK=1 and right channel data is transferred, whenever LRCK =0. LRCK is changed at the falling edge of BLCK and Transferred data is changed at the rising edge of BCLK. Refer to Figure 23 (b) below.

In Right Justified mode, left channel data allows last LSB to be output before LRCK value goes to '0' and right channel data allows last LSB to be output before LRCK value goes to '1'.

LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to Figure 24 (c) below.

In DSP mode, after LRCK outputs to '1' for one period of BCLK, it goes to '0'. After that, left channel data is outputted and then right channel data is outputted. LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to Figure 25 (d) below.

Figure 22, Figure 23, Figure 24, and Figure 25 show the interface method for each mode and I2S TX block is selected as Master. The setting of register is as follows. MS field in STXAIC

(0x2528) register is set to '1'. WL field is set to '0' (The data of left and right channel represents 16-bit). Other fields are set to '0'. In ISP mode, BPOL field in STXMODE (0x252D) register is set to '0'. In other modes, BPOL field in STXMODE (0x252D) register is set to '0' or '1' respectively.
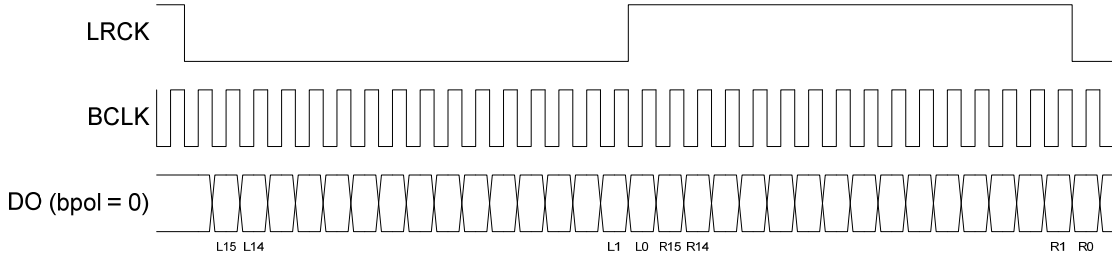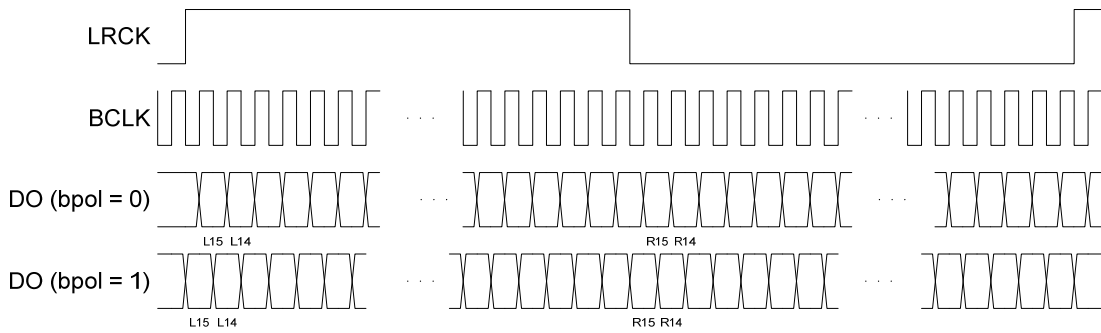
Figure 22 – (a) I2S Mode
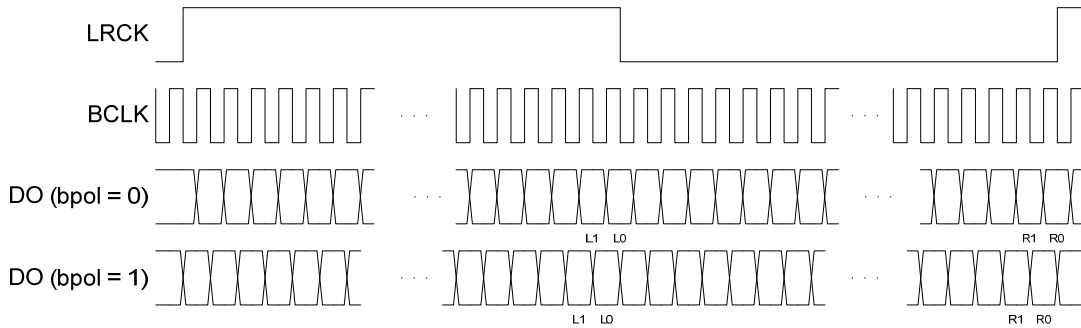
Figure 23 – (b) Left Justified Mode

Figure 24 – (c) Right Justified Mode
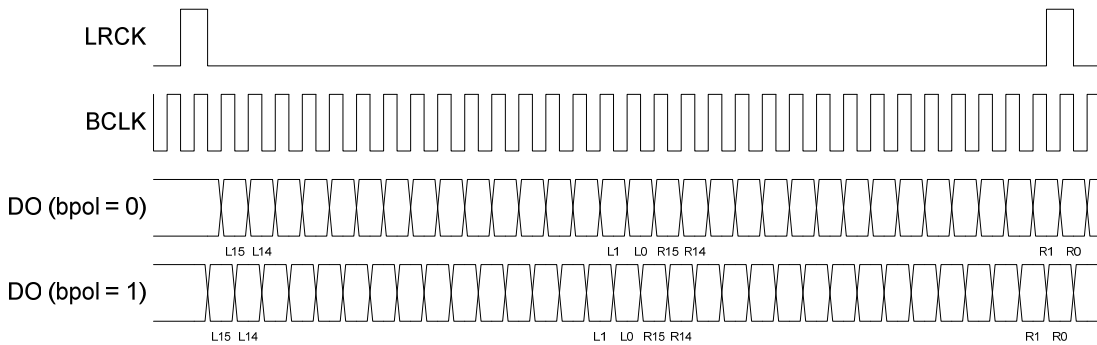
Figure 25 – (d) DSP Mode

Table 26 – I2S Registers

Bit	Name	Descriptions	R/W	Reset Value
STXAIC (I2S TX INTERFACE CONTROL REGISTER, 0x2528)				
7	**MS**	When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured. Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input.	R/W	1

6:5	**FMT**	**Four modes of operation** determined by the value of this field.
		    0: I2S mode
		    1: Left Justified mode
		    2: Right Justified mode
		    3: DSP mode
			R/W	2

4:3	**WL**	**Word Length**. Indicates the number of bits per channel.
		    0: 16 bit
		    1: 20 bit
		    2: 24 bit
		    3: 32 bit
			R/W	0

2	**LRSWAP**	**Left/Right Swap**. When this field is set to '1', the order of the channel for transmitting data is changed. In other words, the data in a right channel is transmitted first.	R/W	0
1	**FRAMEP**	When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode, the left channel data is outputted when LRCK=1 and the right channel data is outputted when LRCK=0. However, when this field is set to '1', the right channel data is outputted when LRCK=1 and the left channel data is outputted when LRCK=0.	R/W	0
0	**BCP**	When this field is set to '1', the polarity of BCLK (Bit Clock) is changed. Clock edge, which allows the data change, is changed.	R/W	0
STXSDIV (I2S TX SYSTEM CLOCK DIVISOR REGISTER, 0x252A)				
7:0	**STXSDIV**	Sets the value for dividing a system clock to generate MCLK. The equation is as follows: $MCLK = System\ Clock/(2 \times STXSDIV)$ When this field is '0', MCLK is not generated.	R/O	0x00
STXMDIV (I2S TX MCLK DIVISOR REGISTER, 0x252B)				
7:0	**STXMDIV**	Sets the value for dividing MCLK to generate BCLK. When STXSDIV register value is '1', BCLK = MCLK/STXMDIV. When STXSDIV register value is greater than 2, BCLK = MCLK/($2 \times STXMDIV$). When this register is '0', BCLK is not generated.	R/O	0x00
STXBDIV (I2S TX BCLK DIVISOR REGISTER, 0x252C)				
7:0	**STXBDIV**	Sets the value for dividing BCLK to generate LRCK. When FMT field in STXAIC(0x2528) register is '0','1','2', LRCK = BCLK/($2 \times STXBDIV$). When FMT field in STXAIC (0x2528) register is '3', LRCK = BCLK/STXBDIV. When this register value is '0', LRCK is not generated.	R/W	0x00
STXMODE (I2S TX MODE REGISTER, 0x252D)				
7	**CSHR**	This field is meaningful when I2STX block acts in a Slave mode. When this field is set to '1', the I2S TX block shares the clock of the I2S RX block. In other words, the MCLK of the I2S RX block is input to the MCLK of the I2S TX block, the BCLK of the I2S RX block is input to the BCLK of the I2S TX block, and the LRCK of the I2S RX block is input to the LRCK of the I2S TX block.	R/W	1
6	**MPOL**	Ddetermines the polarity of MCLK. When this field is '0', MCLK signal retains '1'. When this field is '1', MCLK signal retains '0'.	R/W	1

Bit	Name	Descriptions	R/W	Reset Value
5	BPOL	Indicates the relationship between BCLK and LRCK. When this field is set to '0', LRCK value is changed at the falling edge of BCLK. When this field is set to '1', LRCK value is changed at the rising edge of BCLK.	R/W	1
4	B16	Determines bit width to transfer data in voice block to I2S block. When this field is set to '1', data is transferred by 16-bit data format to I2S block. When this field is set to '0', data is transferred by 8-bit data format to I2S block.	R/W	1
3	POP	When this field is set to '1', data is transferred to I2S block. When this field is set to '0', data is not transferred to I2S block.	R/W	1
2:1	MODE	Sets the mode of transferred data. 0: BLK Mode. Transfer a '0'. 1: MRT Mode. Only the data in Right channel is transferred. ('0' is transferred in Left channel) 2: MLT Mode. Only the data in Left channel is transferred. ('0' is transferred in Right channel) 3: STR Mode. All data in Left or Right channel are transferred.	R/W	3
0	CLKENA	**Clock Enable**. When this field is set to '1', I2S TX is enabled.	R/W	0
SRXAIC (I2S RX INTERFACE CONTROL REGISTER, 0x2538)				
7	MS	When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured. Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input.	R/W	1
6:5	FMT	**Four modes** determined by the value of this field. 0: I2S mode 1: Left Justified mode 2: Right Justified mode 3: DSP mode	R/W	2
4:3	WL	**Word Length**. Indicates the number of bit per each channel. 0: 16 bit 1: 20 bit 2: 24 bit 3: 32 bit	R/W	0
2	LRSWAP	**Left/Right Swap**. When this field is set to '1', the order of the channel for transmitting data is changed. In other words, the data in a right channel is transmitted first.	R/W	0
1	FRAMEP	When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode (FMT=1), data is stored in the left channel when LRCK=1 and data is stored in the right channel when LRCK=0. However, when this field is set to '1', data is stored in the right channel when LRCK=1 and the data is stored in the left channel when LRCK=0.	R/W	0
0	BCP	When this field is set to '1', the polarity of BCLK (Bit Clock) is changed. Clock edge, which allows the data change, is changed.	R/W	0
SRXSDIV (I2S RX SYSTEM CLOCK DIVISOR REGISTER, 0x253A)				
7:0	SRXSDIV	Sets the value for dividing a system clock to generate MCLK. The equation is as follows: $MCLK = System\ Clock/(2 \times SRXSDIV)$ When this field is '0', MCLK is not generated.	R/W	0x00
SRXMDIV (I2S RX MCLK DIVISOR REGISTER, 0x253B)				

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRXMDIV	Sets the value for dividing MCLK to generate BCLK. When SRXSDIV register value is '1', BCLK = MCLK/SRXMDIV. When SRXSDIV register value is greater than 2, BCLK = MCLK/(2×SRXMDIV). When this register value is '0', BCLK is not generated.	R/W	0x00
SRXBDIV (I2S RX BCLK DIVISOR REGISTER, 0x253C)				
7:0	SRXBDIV	Sets the value for dividing BCLK to generate LRCK. When FMT field in SRXAIC(0x2528) register is '0','1','2', LRCK = BCLK/(2(SRXBDIV). When FMT field in SRXAIC (0x2528) register is '3', LRCK = BCLK/SRXBDIV. When this register value is '0', LRCK is not generated.	R/W	0x00
SRXMODE (I2S RX MODE REGISTER, 0x253D)				
7	CSHR	This field is meaningful when I2SRX block acts in a Slave mode. When this field is set to '1', the I2S RX block shares the clock of the I2S TX block. In other words, the MCLK of the I2S TX block is input to the MCLK of the I2S RX block, the BCLK of the I2S TX block is input to the BCLK of the I2S RX block, and the LRCK of the I2S TX block is input to the LRCK of the I2S RX block.	R/W	0
6	MPOL	Determines the polarity of MCLK. When this field is '0', MCLK signal retains '1'. When this field is '1', MCLK signal retains '0'.	R/W	1
5	BPOL	Indicates the relationship between BCLK and LRCK. When this field is set to '0', LRCK value is changed at the falling edge of BCLK. When this field is set to '1', LRCK value is changed at the rising edge of BCLK.	R/W	1
4	B16	Determines bit width to transfer data received from external ADC via I2S interface to voice block. When this field is set to '1', data is transferred by 16-bit data format to voice block. When this field is set to '0', data is transferred by 8-bit data format to voice block.	R/W	1
3	PUSH	When this field is set to '1', data received from external ADC via I2S interface is transferred to voice block. When this field is set to '0', data received from external ADC via I2S interface is not transferred to voice block.	R/W	1
2:1	MODE	Sets the mode of transferred data. 0: **BLK Mode**. Transfer a '0'. 1: **MRT Mode**. Only the data in Right channel is transferred.('0' is transferred in Left channel) 2: **MLT Mode**. Only the data in Left channel is transferred.('0' is transferred in Right channel) 3: **STR Mode**. All data in Left or Right channel are transferred.	R/W	3
0	CLKENA	Clock Enable. When this field is set to '1', I2S RX is enabled.	R/W	0

1.7.8.2 VOICE CODEC

ZIC2410 includes three voice codec algorithms.

- µ-law
- a-law
- ADPCM

The µ-law algorithm is a companding algorithm primarily used in the digital telecommunication systems of North America and Japan. As with other companding algorithms, its purpose is to reduce the dynamic range of an audio signal. In the analog domain this can increase the signal-to-noise ratio (SNR) achieved during transmission and in the digital domain, it can reduce the

quantization error (hence increasing signal to quantization noise ratio). These SNR improvements can be traded for reduced bandwidth and equivalent SNR instead.

The a-law algorithm is a standard companding algorithm used in European digital communications systems to optimize/modify the dynamic range of an analog signal for digitizing.

The a-law algorithm provides a slightly larger dynamic range than the µ-law at the cost of worse proportional distortion for small signals.

Adaptive DPCM (ADPCM) is a variant of DPCM (Differential (or Delta) pulse-code modulation) that varies the size of the quantization step, to allow further reduction of the required bandwidth for a given signal-to-noise ratio. DPCM encodes the PCM values as differences between the current and the previous value. For audio this type of encoding reduces the number of bits required per sample by about 25% compared to PCM.

In order to control voice codec, there are several registers. This section describes the major commonly used registers. For more detailed information, please contact CEL.

Table 27 – VODEC Registers

Bit	Name	Descriptions	R/W	Reset Value
ENCCTL (VOICE ENCODER CONTROL REGISTER, 0x2745)				
7:6		Reserved	R/W	0
5	**B16**	When the bit width of data received to voice encoder is 16-bit, set this field to '1'. When it is 8-bit, set this field to '0'.	R/W	0
4	**MUT**	**Mute Enable**. When this field is set to '1', the Mute function is enabled. ENCMUT1 and ENCMUT0 values are input to the voice encoder block.	R/W	0

3:2	**SEL**	**Encoder Select**. Selects voice encoder algorithm.
		    0: No Encoding
		    1: µ-law
		    2: a-law
		    3: ADPCM
			R/W	0

1	**INI**	**Encoder Initialize.** When this field is set to '1', the pointer in voice encoder is initialized. This field cannot be read.	W	0
0	**ENA**	**Encoder Enable**. When this field is set to '1', voice encoder acts.	R/W	0
DECCTL (VOICE DECODER CONTROL REGISTER, 0x274D)				
7	**LPB**	**Loopback Test**. When this field is set to '1', Loopback test mode is selected. In this case, the output of voice encoder is connected to the input of voice decoder.	R/W	0
6		Reserved	R/W	0
5	**B16**	The bit width of data which is output from voice decoder is 16-bit, set this field to '1'. When this field is set to '0', the bit width of data which is output from voice decoder is 8-bit.	R/W	0
4	**MUT**	**Mute Enable**. When this field is set to '1', Mute function is enabled. DECMUT1 and DECMUT0 values are transferred from voice decoder.	R/W	0

3:2	**SEL**	**Decoder Select**. Select voice decoder.
		    0: No Decoding
		    1: µ-law
		    2: a-law
		    3: ADPCM
			R/W	0

1	**INI**	When this field is set to '1', the pointer in voice decoder is initialized. This field cannot be read.	W	0
0	**ENA**	**Decoder Enable**.	R/W	0

Bit	Name	Descriptions	R/W	Reset Value
		When this field is set to '1', voice decoder is enabled.		

1.7.8.3 VOICE FIFO / DMA

Data received via I2S interface is compressed by the voice codec; compressed data is stored in Voice TXFIFO (0x2600~0x267F). The size of Voice TXFIFO is 128 byte.

Data in the MAC RXFIFO is processed by DMA operation, and stored in Voice RX FIFO (0x2680~0x26FF). Data in Voice RXFIFO is decompressed by the voice codec and transmitted to an external component via I2S. The size of Voice RXFIFO is 128 byte.

1.7.8.4 VOICE TX FIFO / DMA CONTROL
Table 28 – Voice TX Registers

Bit	Name	Descriptions	R/W	Reset Value
VTFDAT (VOICE TX FIFO DATA REGISTER, 0x2750)				
7:0	**VTFDAT**	When writing data to this register, data is stored in Voice TX FIFO in order. When reading this register, data stored in Voice TX FIFO can be read.	R/W	0x00
VTFMUT (VOICE TX FIFO MUTE DATA REGISTER, 0x2751)				
7:0	**VTFMUT**	When MUT field in VTFCTL register is set to '1', data in this register is transferred instead of data in Voice TX FIFO. When INI field in VTFCTL register is set to '1', data in Voice TX FIFO is initialized by data in VTFMUT.	R/W	0x00
VTFCTL (VOICE TX FIFO CONTROL REGISTER, 0x2752)				
7:4		Reserved		0
3	**VTDENA**	**Voice TX DMA Enable**. When this field is set to '1', Voice TX DMA is enabled. This field value is cleared automatically.	W/O	0
2	**MUT**	When this field is set to '1', data in VTFMUT register is transferred instead of data in Voice TX FIFO. This field can be read.	R/W	0
1	**CLR**	When this field is set to '1', Write pointer and Read pointer of Voice TX FIFO are initialized. The status value of underflow and overflow is initialized.	W/O	0
0	**INI**	When this field is set to '1', all data in Voice TXFIFO is replaced by the value in VTFMUT register.	W/O	0
VTFRP (VOICE TX FIFO READ POINTER REGISTER, 0x2753)				
7:0	**VTFRP**	Indicates the address of Voice TXFIFO to be read next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00
VTFWP (VOICE TX FIFO WRITE POINTER REGISTER, 0x2754)				
7:0	**VTFWP**	Indicates the address of Voice TXFIFO to be written next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00
VTFSTS (VOICE TX FIFO STATUS REGISTER, 0x275A)				
7:5		Reserved		0
4	**ZERO**	When INI field in VTFCTL register is set to '1', data in Voice TX FIFO is initialized by data in VTFMUT register. During this initialization is processed, this field is set to '1'. After initialization is finished, this field is set to '0'.	R/O	0
3	**PSH**	Set to '1' while pushing data into Voice TX FIFO.	R/O	0
2	**POP**	Set to '1' while popping data on Voice TX FIFO.	R/O	0
1:0		Reserved		0
VTDSIZE (VOICE TX DMA SIZE REGISTER (VOICE TX FIFO->MAC TX FIFO), 0x275B)				
7:0	**VTDSIZE**	Set the data size for DMA operation.	R/W	0x00

1.7.8.5   VOICE RX FIFO / DMA CONTROL
Table 29– Voice RX Registers

Bit	Name	Descriptions	R/W	Reset Value
VRFDAT (VOICE RX FIFO DATA REGISTER, 0x2760)				
7:0	VRFDAT	When writing data to this register, data is stored in Voice RX FIFO in order. When reading this register, data stored in Voice RX FIFO can be read.	R/W	0x00
VRFMUT (VOICE RX FIFO MUTE DATA REGISTER, 0x2761)				
7:0	VRFMUT	When MUT field in VRFCTL register is set to '1', data in this register is transferred instead of data in Voice RX FIFO. When INI field in VRFCTL register is set to '1', data in Voice RX FIFO is initialized by data in VTFMUT.	R/W	0x00
VRFCTL (VOICE RX FIFO CONTROL REGISTER, 0x2762)				
7:4		Reserved		0
3	VRDENA	**Voice RX DMA Enable:** When this field is set to '1', the Voice RX DMA is enabled. This field value is cleared automatically.	W/O	0
2	MUT	When this field is set to '1', data in the VRFMUT register is transferred instead of data in the Voice RX FIFO.	R/W	0
1	CLR	When this field is set to '1', the Write pointer and Read pointer of the Voice RX FIFO are initialized. The status value of the underflow and overflow are initialized.	W/O	0
0	INI	When this field is set to '1', all data in the Voice RXFIFO is replaced by the values in the VRFMUT register.	W/O	0
VRFRP (VOICE RX FIFO READ POINTER REGISTER, 0x2763)				
7:0	VRFRP	This register indicates the address of the Voice RXFIFO to be read next. Since the size of the FIFO is 128 byte, the LSB is used to test wrap-around.	R/W	0x00
VRFWP (VOICE RX FIFO WRITE POINTER REGISTER, 0x2764)				
7:0	VRFWP	This register indicates the address of the Voice RXFIFO to be written next. Since the size of the FIFO is 128 byte, the LSB is used to test wrap-around	R/W	0x00
VRFSTS (VOICE RX FIFO STATUS REGISTER, 0x276A)				
7:5		Reserved		0
4	ZERO	When INI field in the VRFCTL register is set to '1', data in the Voice TX FIFO is initialized by the data in the VRFMUT register. During the processiong of this initialization, this field is set to '1', and set to '0' when initialization is finished.	R/O	0
3	PSH	Set to '1' while pushing data into the Voice RX FIFO.	R/O	0
2	POP	Set to '1' while popping data on the Voice RX FIFO.	R/O	0
1:0		Reserved		0
VRDSIZE (VOICE RX DMA SIZE REGISTER (MAC RX FIFO->VOICE RX FIFO), 0x276B)				
7:0	VRDSIZE	Sets the data size for DMA.	R/W	0x00

1.7.8.6 VOICE INTERFACE CONTROL

Table 30– Voice Interrupt Registers

Bit	Name	Descriptions	R/W	Reset Value
VTFINTENA (VOICE TX FIFO INTERRUPT ENABLE REGISTER, 0x2770)				
7	**EMPTY**	Voice TX FIFO Empty Interrupt Enable	R/W	0
6	**FULL**	Voice TX FIFO Full Interrupt Enable	R/W	0
5:0		Should be set as '0'.		0
VRFINTENA (VOICE RX FIFO INTERRUPT ENABLE REGISTER, 0x2771)				
7	**EMPTY**	Voice RX FIFO Empty Interrupt Enable	R/W	0
6	**FULL**	Voice RX FIFO Full Interrupt Enable	R/W	0
5:0		Should be set as '0'.		0
VDMINTENA (VOICE DMA CONTROLLER INTERRUPT ENABLE REGISTER, 0x2772)				
7:5		Should be set as '0'.		0
4	**VTDDONE**	Voice TX DMA Done Interrupt Enable	R/W	0
3:1		Should be set as '0'.		0
0	**VRDDONE**	Voice RX DMA Done Interrupt Enable	R/W	0
VTFINTSRC (VOICE TX FIFO INTERRUPT SOURCE REGISTER, 0x2773)				
7	**EMPTY**	Voice TX FIFO Empty Interrupt Source. When EMPTY field in VTFINTENA register is set to '1' and EMPTY field in VTFINTVAL register is set to '1', this field is set to '1'. Cleared by software.	R/W	0
6	**FULL**	Voice TX FIFO Full Interrupt Source	R/W	0
5:0		Reserved		0
VRFINTSRC (VOICE RX FIFO INTERRUPT SOURCE REGISTER, 0x2774)				
7	**EMPTY**	Voice RX FIFO Empty Interrupt Source	R/W	0
6	**FULL**	Voice RX FIFO Full Interrupt Source	R/W	0
5:0		Reserved		0
VDMINTSRC (VOICE DMA CONTROLLER INTERRUPT SOURCE REGISTER, 0x2775)				
7:5		Should be set as '0'.		0
4	**VTDDONE**	Voice TX DMA Done Interrupt Source	R/W	0
3:1		Should be set as '0'.		0
0	**VRDDONE**	Voice RX DMA Done Interrupt Source	R/W	0
SRCCTL (VOICE SOURCE CONTROL REGISTER, 0x277A)				
7		Should be set as '0'.		0

6:5	**MUX**	Selects the specific interface to communicate between voice codec and external data.
		    0: I2S
		    1: SPI
		    2: UART0
		    3: UART1
			R/W	0

4:0		Should be set as '0'.		0
VSPCTL (VOICE SOURCE PATH CONTROL REGISTER, 0x277E)				
7		Reserved		0
6	**DECMUT**	This register is used to send mute data from voice decoder to the external interface. When this field is set to '1', VSPMUT1 and VSPMUT0 value are transferred to the external interface.	R/W	0
5	**DECINI**	When using 8-bit external interface, 16-bit data transferred from voice decoder needs to be changed to 8-bit. When this field is set to '1', corresponding control circuit is initialized.	R/W	0
4	**DECB16**	When using 8-bit external interface such as UART and so on, 16-bit data transferred from voice decoder needs to be changed to 8-bit. When this field is set to '1', high 8-bit data of 16-bit data is transferred first and then low 8-bit data is transferred.	R/W	0
3		Reserved		0

Bit	Name	Descriptions	R/W	Reset Value
2	ENCMUT	This register is used to send mute data from external interface to voice encoder. When this field is set to '1', VSPMUT1and VSPMUT0 values are transferred to voice encoder.	R/W	0
1	ENCINI	When using 8-bit external interface, 16-bit data transferred to voice encoder needs to be changed to 16-bit. When this field is set to '1', corresponding control circuit is initialized.	R/W	0
0	ENCB16	When using 8-bit external interface, 8-bit input data needs to be changed to 16-bit, which is compatible with the voice encoder. When this field is set to '1', it is changed to 16-bit.(8-bit received first: high bit; 8-bit received later: low bit)	R/W	0

1.7.9 RANDOM NUMBER GENERATOR (RNG)

Random Number Generator generates 32-bit random number with seed. Whenever ENA bit in RNGC register is set to '1', generated number is stored in RNGD3 ~ RNGD0 register.

Table 31– Random Number Generator Registers

Bit	Name	Descriptions	R/W	Reset Value
RNGD3 (RNG DATA3 REGISTER, 0x2550)				
7:0	RNGD3	This register stores MSB (RNG [31:24]) of 32-bit random number.	R/O	0xB7
RNGD2 (RNG DATA2 REGISTER, 0x2551)				
7:0	RNGD2	This register stores 2nd MSB (RNG [23:16]) of 32-bit random number.	R/O	0x91
RNGD1 (RNG DATA1 REGISTER, 0x2552)				
7:0	RNGD1	This register stores 3rd MSB (RNG [15:8]) of 32-bit random number.	R/O	0x91
RNGD0 (RNG DATA0 REGISTER, 0x2553)				
7:0	RNGD0	This register stores LSB (RNG [7:0]) of 32-bit random number.	R/O	0xC9
SEED3 (RNG SEED3 REGISTER, 0x2554)				
7:0	SEED3	This register stores MSB (SEED [31:24]) of required seed to generate random number.	W/O	-
SEED2 (RNG SEED2 REGISTER, 0x2555)				
7:0	SEED2	This register stores 2th MSB (SEED [23:16]) of required seed to generate random number.	W/O	0x00
SEED1 (RNG SEED1 REGISTER, 0x2556)				
7:0	SEED1	This register stores 3rdMSB (SEED [15:8]) of required seed to generate random number.	W/O	0x00
SEED0 (RNG SEED0 REGISTER, 0x2557)				
7:0	SEED0	This register stores LSB (SEED [7:0]) of required seed to generate random number.	W/O	0x00
RNGC (RNG DATA3 REGISTER, 0x2558)				
7:1		Reserved		0
0	ENA	RNG Enable. When this field is set to '1', RNG acts. This field value is changed to '0' automatically.	R/W	0

1.7.10 QUAD DECODER

The Quad Decoder block notifies the MCU of the counter value based on the direction and movement of a pointing device, such as a mouse, after receiving a Quadrature signal from the pointing device.

Quadrature signal is changed with 90° phase difference (1/4 period) between two signals as shown in Figure 26 In addition, counter value means 1/4 of one period. Since this block can receive three Quadrature signals, it can support not only the two-dimensional movement such as mouse but also the pointing device which is in three dimensions.

Figure 26, (a) shows that the XA signal is changing before the XB signal. In this case, the pointing device is moving in the down direction. Drawing (b) shows that the XB signal is changing before the XA signal. In this case, the pointing device is moving in the up direction. The rules for YA, YB, ZA and ZB are the same as described above for XA and XB.
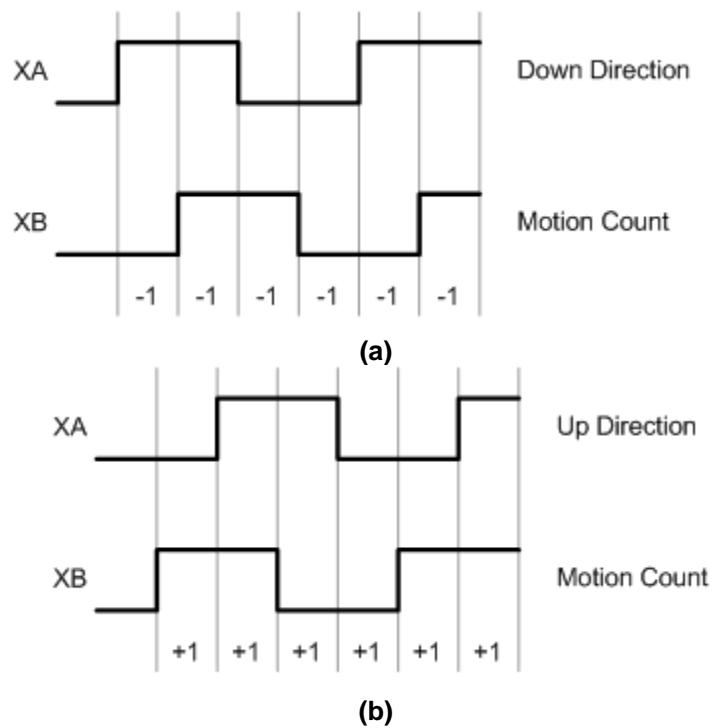
Figure 26 – Quadrature Signal Timing between XA and XB.

Table 32– Pointer and Quad Control Registers

Bit	Name	Descriptions	R/W	Reset Value
UDX (UpDown X Register, 0x2560)				
7:1		Reserved		0

0	**UPDN_X**	Notifies the MCU of movement in the **X-axis**.
		    1: Up
		    0: Down
			R/O	0

CNTX (Count X Register, 0x2561)				
7:0	**CNTX**	Notifies the MCU of the count value for movement in the **X-axis**.	R/O	0x00
UDY (UpDown Y Register, 0x2562)				
7:1		Reserved		

0	**UPDN_Y**	Notifies the MCU of movement in the **Y-axis**.
		    1: Up
		    0: Down
			R/O	0

CNTY (Count Y Register, 0x2563)				
7:0	**CNTY**	Notifies the MCU of the count value for movement in the **Y-axis**.	R/O	0x00
UDZ (UpDown Z Register, 0x2564)				
7:1		Reserved		0x00

0	**UPDN_Z**	Notifies the MCU of movement in the **Z-axis**.
		    1: Up
		    0: Down
			R/O	0

CNTZ (Count Z Register, 0x2565)				
7:0	**CNTZ**	Notifies the MCU of the count value for movement in the **Z-axis**.	R/O	0x00
QCTL (Quad Control Register, 0x2566)				
7:3		Reserved		x
2	**ENA**	**Quad Enable**. When this field is set to '1', the Quad Decoder is enabled.	R/W	
1	**INI**	**Quad Initialize**. When this field is set to '1', the internal register values of the Quad Decoder are initialized.	R/W	
0	**MODE**	**Mode Select**. When this field is set to '1', counter value is increased to the point of changing movement direction. When this field is set to '0', current counter value is decreased to the point of changing movement direction.	R/W	0

1.7.11 INTERNAL VOLTAGE REGULATOR
There are separate Analog and Digital regulators in the ZIC2410. The Analog regulator supplies power to the RF and analog blocks, while the Digital regulator supplies power to all the digital blocks. MSV, an external pin, sets the output voltage: when MSV is set to '0', 1.5V is generated and when MSV is set to '1', 1.8V is generated. AVREG3V and DVREG3V, external pins, should be connected to the 3V supply in order to operate the internal regulators.

1.7.12 4-CHANNEL 8-BIT SENSOR ADC

This block monitors external sensor output and converts the external analog signal into the corresponding digital value. The output of the sensor ADC is 8-bit wide and sampling frequency is fixed to 8KHz. For the Sensor ADC control register, refer to the SADCCON (0x22AB), SADCVALH (0x22AC), SADCVALL (0x22AD), SADCBIASH (0x22AE), and SADCBIASL (0x22AF).

Table 33– Sensor ADC Registers

Bit	Name	Descriptions			R/W	Reset Value
SADCCON (SENSOR ADC CONTROL REGISTER, 0x22AB) This register controls sensor ADC operation.						
7	**SADCEN**	Sensor ADC Enable			RW	0
6	**SADCDONE**	When the values of the SADCVALH and SADCVALL register are updated, SADCDONE is set to '1'.			RO	0
5:4	**SADCREF**	Select the reference voltage for the sensor ADC.			RW	0
		SADCREF	**Reference**	**Description**		
		00	Internal	TOP = 1.2V BOT = 0.3V VMID = 0.75V		
		01		Reserved		
		10	External	TOP = ACH2(0V~1.5V) BOT = ACH3(ACH3 < ACH2) VMID = (ACH2+ACH3)/2		
		11	Internal	TOP = VDD(1.5V) BOT = GND VMID = (VDD+GND)/2		
3:0	**SADCCH**	Select the input channel of sensor ADC			RW	0
		SSADCCH	**Input**	**Description**		
		0000	ACH0	Single input		
		0001	ACH1	Single input		
		0010	ACH2	Single input		
		0011	ACH3	Single input		
		0100	ACH0, ACH1	Differential input		
		0101	ACH2, ACH3	Differential input		
		0110	Temperature Sensor	Embedded temperature sensor		
		0111	Battery Monitor	Embedded battery monitor		
		1000	GND	Just for calibration		
		1001	VDD	Just for calibration		
		others		Reserved		
SADCVALH (SENSOR ADC OUTPUT VALUE HIGH DATA REGISTER, 0x22AC) This register stores the output value of sensor ADC (SADCVAL). SADCVAL, which is a 15bit unsigned integer value, is stored in the SADCVALH and SADCVALL register. SADCVALH stores 8 bit MSB of SADCVAL (SADCVAL [14:7]).						

Bit	Name	Descriptions	R/W	Reset Value
7:0	**SADCVALH**	SADCVAL [14:7]	RO	0x00
SADCVALL (SENSOR ADC OUTPUT VALUE LOW DATA REGISTER, 0x22AD) This register stores the output value of sensor ADC. SADCVAL, which is a 15bit unsigned integer value, outputs 15-bit data by SADCVALH and SADCVALL register. Only high 8-bit is valid. This register represents low 7-bit data (SADCVAL[6:0]) of 15-bit data.				
7:1	**SADCVALL**	SADCVAL[6:0]	RO	0x00
0		Reserved		0
SADCBIASH (SENSOR ADC DC BIAS HIGH DATA REGISTER, 0x22AE) This register is used to compensate the DC bias of the sensor ADC output. SADCBIAS, which is a 15-bit unsigned integer value, is stored in the SADCBIASH and SADCBIASL registers. SADCBIASH register stores the most significant 8bit of SADCBIAS (SADCBIAS [14:7]).				
7:0	**SADCBIASH**	SADCBIAS [14:7]	RW	0x00
SADCBIASL (SENSOR ADC DC BIAS LOW DATA REGISTER, 0x22AF) This register is used to compensate the DC bias of the sensor ADC output. SADCBIASL register stores the least significant 7bit of SADCBIAS (SADCBIAS[6:0]).				
7:1	**SADCBIASL**	SADCBIAS[6:0]	RW	0x00
0		Reserved		0

1.7.13 ON-CHIP POWER-ON RESET

This block generates the reset signal to initialize the digital block during power-up. When On-chip regulator output or external battery is used as the power of digital core block and power is provided, it outputs the internal reset signal.

1.7.14 TEMPERATURE SENSOR

The on-chip temperature sensor can be used to detect changes in the ambient temperature.

To control the functionality of this block, refer to the section 1.7.12. Whenever temperature is increased by 1°C, the output of this block is decreased by -16.5mV/°C. Figure 27 below graphs the typical output value vs. the temperature sensed. Improved accuracy can be achieved through calibration.
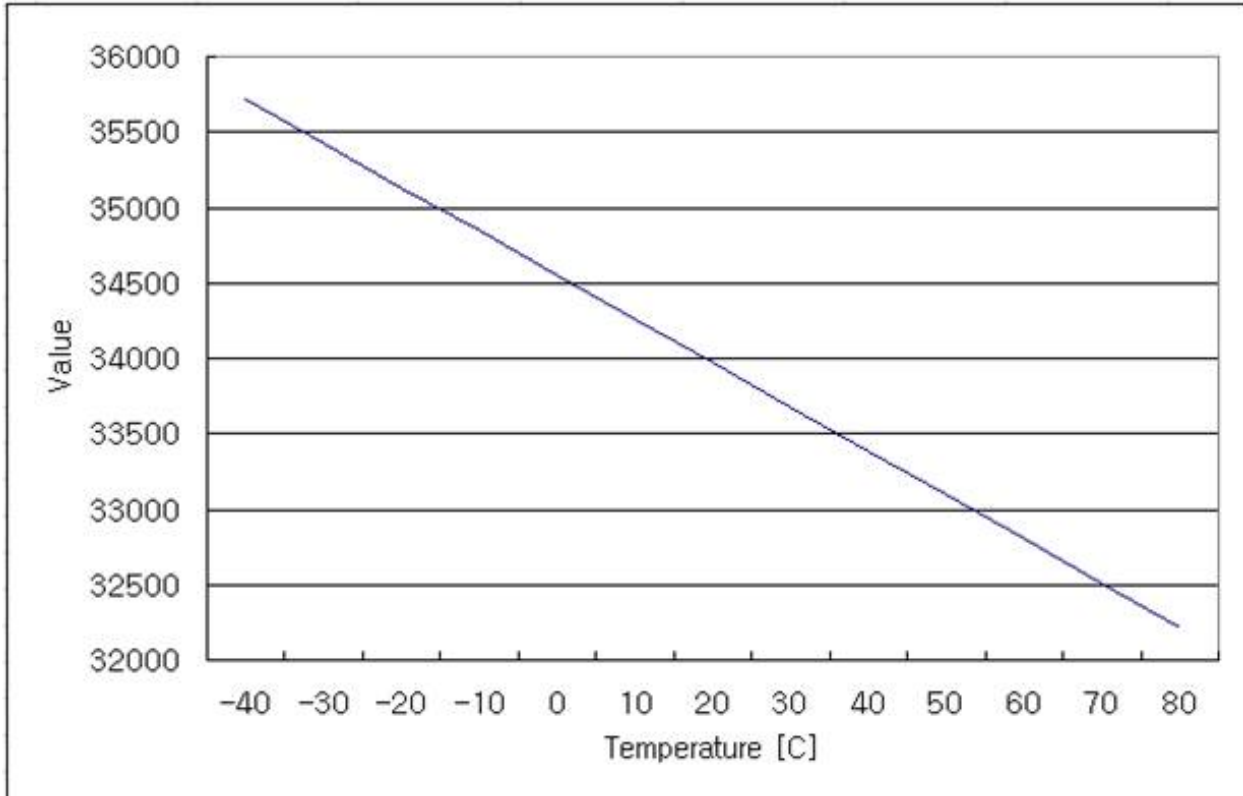
Figure 27 – Typical Temperature Sensor Characteristics

1.7.15 BATTERY MONITORING

This block can be used to monitor the voltage level of the 3V supply. To control the functionality of this block, refer to the section 1.7.12. Figure 28 below graphs the output value of the monitor vs. the input voltage.
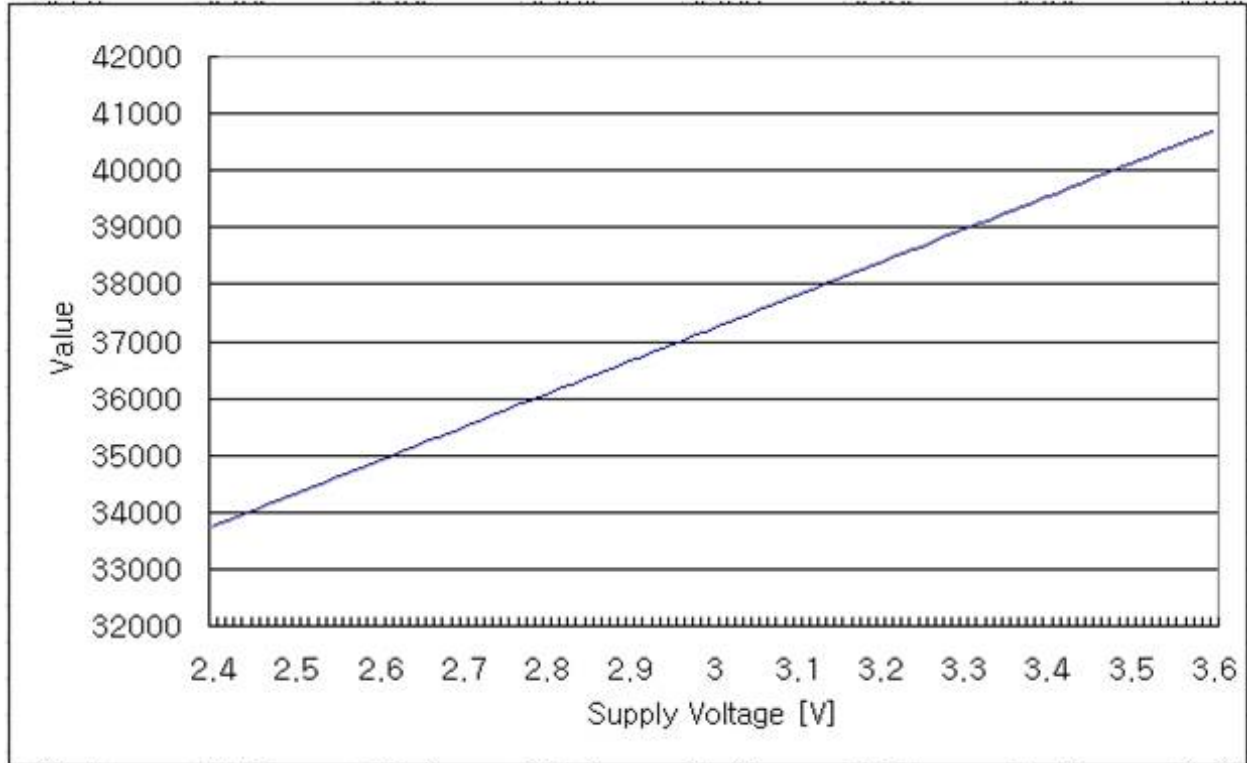
Figure 28 – Battery Monitor Characteristics

1.8 MEDIUM ACCESS CONTROL LAYER (MAC)

The Medium Access Control (MAC) block processes a command received from the high layer (MCU), transmits the data received from high layer to baseband modem, or encrypts it and then transmits to baseband modem. In addition, it indicates the status of PHY and transmits the data received from baseband modem to high layer, or transmits the decrypted data to high layer.

The function of the MAC block is to transfer the data from the higher layer to the PHY block, to send the received data from the PHY to the higher layer with or without encryption or decryption. Figure 29 shows the MAC block diagram.
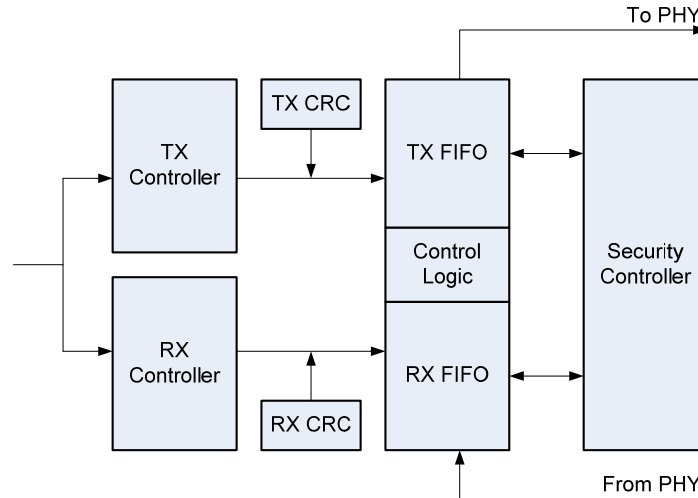
Figure 29 – MAC block diagram

IEEE802.15.4 Frame Format

IEEE802.15.4 transmits the data in packets with each packet having a specified frame format. Figure 30 shows a schematic view of the IEEE 802.15.4 frame format.

The PHY frame to be transmitted consists of preamble, start of frame delimiter (SOF), frame length and PHY Service Data Unit (PSDU) fields. The Preamble is used to adjust the gain of receiving signal and obtain synchronization at the received stage. The SOF is used to indicate the starting position of the frame and obtain exact frame timing synchronization. Frame length is 1 byte and is used to indicate the PSDU length which can vary up to a maximum of 127 bytes.

The PSDU contains the MPDU (MAC protocol data unit) as a payload.

The MPDU means the frame format generated in the MAC layer and it is consisted of frame control field, data sequence number, address information, frame payload and Frame Check Sequence (FCS) field.

The area, including a frame control field, a data sequence number field, and an address information field, is defined as the MAC header. The FCS field is defined as the MAC footer. The data which is transmitted from the higher layer is located in the MAC payload. For detailed information on frame format, refer to the IEEE802.15.4 standard.
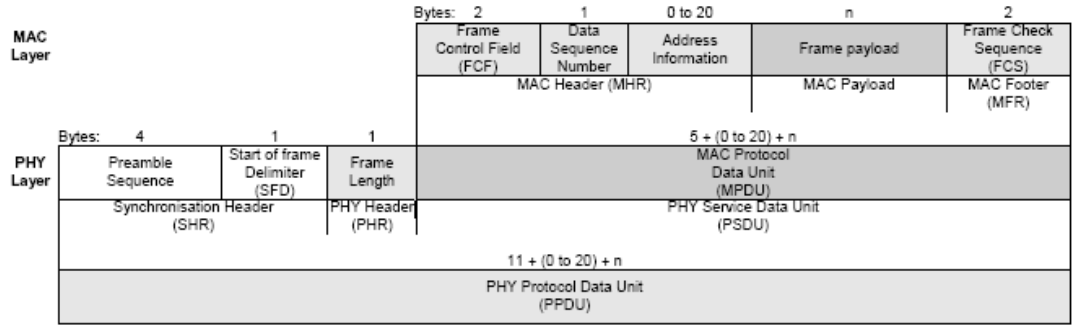
Figure 30 – IEEE 802.15.4 Frame Format

Synchronization Header (SHR)
In IEEE802.15.4 standard, a frame format includes the synchronization header (SHR) for the purpose of adjusting the gain of the receiving signal, detecting packet and obtaining synchronization.

SHR is consisted of a preamble and Start of Frame Delimiter (SFD). The Preamble is formatted by repeating the same 8 symbols ('0') in 4 bytes. 1 byte SFD is used to detect the frame start and obtain timing synchronization and it is defined as 0XA7 in IEEE802.15.4 standard.

PHY Header (PHR)
The Length field is used to define the size of the MPDU or the PSDU.

The value clarified in length field doesn't include the length field itself. However, the length of Frame Check Sequence (FCS) is included. The PHY block takes data up to the size defined by the length field in TX FIFO, and transmits that data.

MAC Header (MHR)
This field is consisted of frame control field (FCF), data sequence number (DSN) and address information. FCF includes the frame information such as frame type or addressing mode and so on. DSN means the sequence of packet. In other words, DSN is incremented after transmitting. Therefore, next packet has a different DSN. For detailed information, refer to the IEEE802.15.4 standard.

MAC Footer (MFR)
This field is called as frame check sequence (FCS) and it follows the last data of MAC payload byte. FCS polynomial is as follows.

$$x16 + x12 + x5 + 1$$

1.8.1 RECEIVED MODE
When receiving the data from the PHY block, the MAC block stores the data in the RX FIFO.

The data in the RX FIFO can be decrypted by the PCMD1 (0X2201) register or it can be read by the MRFCPOP (0x2080) register. Data decryption is implemented by the AES-128 algorithm, which supports CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4. The RX Controller controls the process described above. When decrypting the data, the received frame data length is modified and the modified value is stored in the LSB of each frame by the hardware again.

The size of the RX FIFO is 256 bytes and it is implemented by a Circular FIFO with a Write Pointer and a Read Pointer. The RX FIFO can store several frame data received from the PHY block. Since the LSB of each frame data represents the frame data length, it can be accessed by the Write pointer and the Read Pointer.

When the data is received from the PHY block, the CRC information is checked to verify data integrity.

When the AUTO_CRC control bit of the MACCTRL (0x2191) register is set to '1', CRC information is verified by the RX CRC block automatically. To check the result, refer to the CRC_OK field of the MACSTS (0x2180) register. When the value of the CRC_OK field is set to '1', there is no problem with CRC Information. When the AUTO_CRC control bit of the MACCTRL (0x2191) register is not set to '1', the CRC information should be verified by the software.

When a packet reception is completed in the PHY block, a PHY interrupt is sent to the MCU.

In addition, when decryption operation is completed, an AES interrupt is sent to the MCU.

1.8.2   TRANSMIT MODE

To transmit the data from a higher layer (MCU) to the PHY block, the device stores the data in the TX FIFO of the MAC block. When the MCU writes data in the MTFCPUSH (0x2000) register, data is stored in TX FIFO of MAC. The size of the TX FIFO is 256 byte and it is implemented by a Circular FIFO with a Write Pointer and a Read Pointer. Since each data in the TX FIFO is mapped to the memory area in the MCU, it can be written or read directly by the MCU.

The data stored in the TX FIFO can be encrypted by the PCMD1 (0x2201) register or is transmitted to the PHY block by the PCMD0 (0x2200) register. The TX Controller controls the process described above. Data encryption is implemented by the AES-128 algorithm, which supports CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4. The data length which is to be transmitted is stored in the LSB of each frame by the software when the frame data is stored in the TX FIFO by the MCU. When the data in the TX FIFO is encrypted, the data length is modified and then stored by the hardware again.

When transmitting the data in the TX FIFO, the CRC operation is processed to verify data integrity. When the AUTO_CRC control bit of the MACCTRL (0x2191) register is set to '1', CRC information is generated by TX CRC block automatically. Otherwise, the CRC operation should be operated by software.

When data encryption is completed, an AES interrupt is sent to the MCU. When the data transmission to the PHY block is completed, a PHY interrupt is sent to the MCU.

1.8.3   DATA ENCRYPTION AND DECRYPTION

Data encryption or decryption is done by the security controller block. Security Controller consists of the block for processing encryption /decryption operation and the block for controlling it.

In order to implement CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4, a 128-bit key value and a nonce are needed. ZIC2410 can have two 128-bit key values, KEY0 and KEY1. For encryption, the desired nonce value should be stored in the TX Nonce and KEY0 or KEY1 should be selected for use. For decryption, the desired nonce value should be stored in the RX Nonce and KEY0 or KEY1 should be selected for use. For more detailed information, refer to the IEEE802.15.4 standard document.

The SAES (0x218E) register is used only for AES operation. In this case, the required data for this operation should be stored in the SABUF register and KEY0 or KEY1 should be selected for use.

Table 34 describes the registers for controlling the MAC TX FIFO.

Table 34 – MAC TX FIFO Registers

Bit	Name	Descriptions	R/W	Reset Value
MTFCPUSH (TX FIFO PUSH DATA REGISTER, 0x2000)				
7:0	**MTFCPUSH**	When data is written to this register, it is stored in TX FIFO. The size of TX FIFO is 256 byte and it can be accessed by MCU or VTXDMA.	W/O	0x00
MTFCWP (TX FIFO WRITE POINTER REGISTER, 0x2001)				
7:0	**MTFCWP**	**TX FIFO Write Pointer:** Total is 9-bit with MTFCWP8 in MTFCSTS register. It is increased by '1' whenever writing data to TX FIFO.	R/W	0x00
MTFCRP (TX FIFO READ POINTER REGISTER, 0x2002)				
7:0	**MTFCRP**	**TX FIFO Read Pointer**: Total is 9-bit with MTFCRP8 in MTFCSTS register. It is increased by '1' whenever reading data from TX FIFO.	R/W	0x00
MTFCCTL (TX FIFO CONTROL REGISTER, 0x2003)				
7:3		Reserved		0x00
2	**ASA**	When this field is set to '1', it automatically sets the starting address of the packet and the length of the packet encrypted by the AES engine to the information of the packet which is to be transmitted.	RW	1
1	**ENA**	When this field is set to '1', MTXFIFO is enabled.	RW	1
0	**CLR**	When this field is set to '1', MTFCWP, MTFCRP, MTFCSTS, MTFCSIZE, MTFCRM registers are initialized.	RW	0
MTFCSTS (TX FIFO STATUS REGISTER, 0x2004)				
7	**MTFCWP8**	Total is 9-bit address with MTFCWP register. This field is the MSB and is used to detect wrap around of a circular FIFO.	R/W	0
6	**MTFCRP8**	Total is 9-bit address with MTFCRP register. This field is the MSB and is used to detect wrap around of a circular FIFO.	R/W	0
5:2		Reserved		0
1	**FULL**	Set to '1' when data size in the TX FIFO is 256 byte.	R/O	0
0	**EMPTY**	Set to '1' when data size in the TX FIFO is '0'.	R/O	0
MTFCSIZE (TX FIFO Data Size Register, 0x2005)				
7:0	**MTFCSIZE**	Represents the number of valid data bytes in theTX FIFO. This field value is valid when FIFO status is normal and is calculated by the difference between MTFCWP (0x2001) and MTFCRP (0x2002).	R/O	0x00
MTFCSBASE (TX FIFO AES ENCRYPTION DATA START POINTER REGISTER, 0x2007)				
7:0	**MTFCSBASE**	Represents the starting address of data to be encrypted by the AES engine in the TX FIFO. This field is set by the MCU or is set automatically to the starting address of a packet to be transmitted when the ASA field in the MTFCCTL register is set to '1'.	R/W	0x00
MTFCSLEN (TX FIFO AES ENCRYPTION DATA LENGTH REGISTER, 0x2008)				
7:0	**MTFCSLEN**	Represents the length of the data to be encrypted by the AES engine in the TX FIFO. This field is set by the MCU or is set automatically to the length of a packet to be transmitted when the ASA field in the MTFCCTL register is set to '1'.	R/W	0x00

Table 35 describes the registers for controlling MAC RX FIFO.

Table 35 – MAC RX FIFO Registers

Bit	Name	Descriptions	R/W	Reset Value
MRFCPOP (RX FIFO POP Data Register, 0x2080)				
7:0	**MRFCPOP**	This register can read data in RX FIFO. The size of RX FIFO is 256 byte and it can be accessed by the MCU or by VRXDMA.	W/O	0x00
MRFCWP (RX FIFO WRITER POINTER REGISTER, 0x2081)				
7:0	**MRFCWP**	**RX FIFO Write Pointer:** Total is 9-bit with MRFCWP8 in the MRFCSTS register. It is increased by '1' whenever data is written to the RX FIFO.	R/W	0x00
MRFCRP (RX FIFO READ POINTER REGISTER, 0x2082)				
7:0	**MRFCRP**	**RX FIFO Read Pointer:** Total is 9-bit with MRFCRP8 in the MRFCSTS register. It is increased by '1' whenever data is read from the RX FIFO.	R/W	0x00
MRFCCTL (RX FIFO CONTROL REGISTER, 0x2083)				
7:3		Reserved		0x00
2	**ASA**	When this field is set to '1', it automatically sets the starting address of a packet and the length of a packet decrypted by the AES engine to the information of the received packet.	RW	1
1	**ENA**	When this field is set to '1', MRXFIFO is enabled.	RW	1
0	**CLR**	When this field is set to '1', MRFCWP, MRFCRP, MRFCSTS, MRFCSIZE, MRFCRM registers are initialized.	RW	0
MRFCSTS (RX FIFO STATUS REGISTER, 0x2084)				
7	**MRFCWP8**	Total is 9-bit address with MRFCWP register. This field is the MSB, and is used to detect wrap around of a circular FIFO.	R/W	0
6	**MRFCRP8**	Total is 9-bit address with MRFCRP register. This field is the MSB, and is used to detect wrap around of a circular FIFO.	R/W	0
5:2		Reserved		0
1	**FULL**	Set to '1' when data size in the RX FIFO is 256 byte.	R/O	0
0	**EMPTY**	Set to '1' when data size in the RX FIFO is '0'.	R/O	0
MRFCSIZE (RX FIFO Data Size Register, 0x2085)				
7:0	**MRFCSIZE**	Represents the number of valid data bytes in the RX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between MRFCWP and MRFCRP.	R/O	0x00
MRFCSBASE (RX FIFO AES DECRYPTION DATA START POINTER REGISTER, 0x2087)				
7:0	**MRFCSBASE**	Represents the starting address of the data to be decrypted by the AES engine in the RX FIFO. This field is set by the MCU or is set automatically to the starting address of the received packet when the ASA field in the MRFCCTL register is set to '1'.	R/W	0x00
MRFCSLEN (RX FIFO AES DECRYPTION DATA LENGTH REGISTER, 0x2088)				
7:0	**MRFCSLEN**	Represents the length of the data to be decrypted by the AES engine in the RX FIFO. This field is set by the MCU or is set automatically to the length of the received packet when the ASA field in the MRFCCTL register is set to '1'.	R/W	0x00

Table 36 describes the registers for data transmission /reception and security.

Table 36 – Data Transmission/Reception and Security Registers

Bit	Name	Descriptions	R/W	Reset Value
KEY0 (ENCRYPTION KEY0 REGISTERS, 0x2100~0x210F)				
7:0	**KEY0**	This register is the 16-byte key used in the AES operation. **0x210F**: the MSB of the KEY value **0x2100**: the LSB of the KEY value	R/W	0x00
RXNONCE (RX NONCE REGISTERS, 0x2110~0x211C)				
7:0	**RXNONCE**	Used for decryption operation when receiving a packet. It consists of 13-bytes: the Source Address (8-byte), the Frame Counter (4-byte) and the Key Sequence Counter (1-byte). **0x211C**: the MSB of theSource Address **0x2115**: theLSB of the Source Address **0x2114**: the MSB of the Frame Counter **0x2111**: the LSB of the Frame Counter **0x2110**: the Key Sequence Counter	R/W	0x00
SAESBUF (STANDALONE AES OPERATION BUFFER REGISTERS, 0x2120~0x212F)				
7:0	**SAESBUF**	Used for storing data only when processing an AES-128 operation by the AES engine. After the AES-128 operation, the result is stored in this register. **0x212F**: MSB of Plaintext and Ciphertext **0x2120**: LSB of Plaintext and Ciphertext	R/W	0x00
KEY1 (ENCRYPTION KEY1 REGISTERS, 0x2130~0x213F)				
7:0	**KEY1**	This register is a 16-byte KEY for the AES operation. **0x213F**: the MSB of the KEY value **0x2130**: the LSB of the KEY value	R/W	0x00
TXNONCE (TX NONCE REGISTERS, 0x2140~0x214C)				
7:0	**TXNONCE**	Used for the encryption operation when transmitting a packet. It consists of 13-bytes: the Source Address (8-byte), the Frame Counter (4-byte) and the Key Sequence Counter (1-byte). **0x214C**: the MSB of the Source Address **0x2145**: the LSB of the Source Address **0x2144**: the MSB of theFrame Counter **0x2141**: the LSB of the Frame Counter **0x2140**: the Key Sequence Counter	R/W	0x00
The following three addresses are used for network compatible with IEEE802.15.4. EXTADDR is the unique address for the chip or module allocated by IEEE 802.15.4. PANID is the network ID which allows each network to be identified when a network is configured. SHORTADDR is the short address of a device in IEEE802.15.4 network. It allows each device to be identified in the same network. SHORTADDR can be changed whenever connecting to the network.				
EXTADDR (EXTENDED ADDRESS REGISTERS, 0x2150~0x2157)				
7:0	**EXTADDR**	Stores the 64-bit IEEE address. **0x2157**: the MSB of the IEEE address **0x2150**: the LSB of the IEEE address	R/W	0x00
PANID (PANID REGISTERS, 0x2158~0x2159)				
7:0	**PANID**	Stores the 16-bit PAN ID. **0x2159**: the PAN ID [15:8] **0x2158**: the PAN ID [7:0]	R/W	0x00
SHORTADDR (SHORTADDRESS REGISTERS, 0x215A~0x215B)				
7:0	**SHORTAD DR**	Stores the Short address (Network address). **0x215B** : Short address [15:8] **0x215A** : Short address [7:0]	R/W	0x00

		MACSTS (MAC STATUS REGISTER, 0x2180)		
7	ENC/DEC	When this field is set to '1', there is data in the AES encryption or decryption operation. Can only be read.	R/O	0
6	TX_BUSY	When this field is set to '1', data in the MAC FIFO is transmitted to a modem. Can only be read.	R/O	0
5	RX_BUSY	When this field is set to '1', data is transmitted from a modem to the MAC FIFO. Can only be read.	R/O	0
4	SAES_DONE	When Standalone AES operation is finished, this field is set to '1'. It is cleared by the MCU.	R/W	0
3	DECODE_OK	Checks the validity of data according to the type of data received or the address mode. If there is no problem, this field is set to '1'. Can only be read.	R/O	0
2	ENC_DONE	When the AES Encryption operation is finished, this field is set to '1'. It is cleared by the MCU.	R/W	0
1	DEC_DONE	When the AES Decryption operation is finished, this field is set to '1'. It is cleared by the MCU.	R/W	0
0	CRC_OK	If there is no problem in checking the CRC of a received packet, this field is set to '1'.	R/W	0
		MACSAES (SAES RUN REGISTER, 0x218E)		
7:1		Reserved	W/O	0
0	SAES	When this field is set to '1', the AES operation is done by data in SAESBUF and KEY selected by the SA_KEYSEL field in the SEC register. This field is cleared automatically.	W/O	0
		MACRST (MAC RESET CONTROL REGISTER, 0x2190)		
7	RST_FIFO	When this field is set to '1', the MAC FIFO is initialized.	R/W	0
6	RST_TSM	When this field is set to '1', the MAC Transmitter State Machine is initialized.	R/W	0
5	RST_RSM	When this field is set to '1', the MAC Receiver State Machine is initialized.	R/W	0
4	RST_AES	When this field is set to '1', the AES Engine is initialized.	R/W	0
3:0		Reserved		0
		MACCRTL (MAC CONTROL REGISTER, 0x2191)		
7:5		Reserved		0
4	PREVENT_ACK	When this field is set to '1', the RX interrupt doesn't occur when the DSN field of received ACK packet is different from the value in MACDSN register during packet reception.	R/W	0
3	PAN_COORDINATOR	When this field is set to '1', function for PAN Coordinator is enabled.	R/W	0
2	ADR_DECODE	When this field is set to '1', an RX interrupt doesn't occur when the address information of the received packet is not matched with address of the device itself.	R/W	1
1	AUTO_CRC	When this field is set to '1', an RX interrupt doesn't occur when the CRC of the received packet is not valid.	R/W	1
0		Should be set to '0'.		0
		MACDSN (MAC DSN REGISTER, 0x2192)		
7:0	MACDSN	Valid if only PREVENT_ACK in MACCTRL is set to '1'. Sets the DSN field value of the received ACK packet, which can cause a PHY (RX) interrupt. In other words, if the DSN field of the received ACK packet is not equal to MACDSN, the PHY (RX) interrupt does not occur.	R/W	0x00

MACSEC (MAC SECURITY REGISTER, 0x2193)				
7	SA_KEYSEL	Selects the KEY value for Standalone SAES operation. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.	R/W	0
6	TX_KEYSEL	Selects the KEY value for AES operation during packet transmission. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.	R/W	0
5	RX_KEYSEL	Selects the KEY value for AES operation during packet reception. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.	R/W	0
4:2	SEC_M	In CBC-MAC operation, it represents the data length used in the authentication field as byte unit. <table><tr><th>SEC_M</th><th>Authentication Field Length</th></tr><tr><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>6</td></tr><tr><td>3</td><td>8</td></tr><tr><td>4</td><td>10</td></tr><tr><td>5</td><td>12</td></tr><tr><td>6</td><td>14</td></tr><tr><td>7</td><td>16</td></tr></table>	R/W	0
1:0	SEC_MODE	Security Mode: 0: No Security 1: CBC-MAC mode 2: CTR mode 3: CCM mode	R/W	0
TXAL (TX AUXILIARY LENGTH REGISTER, 0x2194)				
7		Reserved	R/W	0
6:0	TXAL	Represents the length used in the AES operation for the packet to be transmitted. It has a different meaning for each security mode as follows. **Security mode: CTR** – It represents the number of bytes between length byte and the data to be encoded or decoded in FIFO. **Security mode: CBC-MAC** – It represents the number of bytes between length byte and the data to be authenticated. **Security mode: CCM** – It represents the length of the data which is used not in encoding or decoding but in authentication.	R/W	0x00
RXAL (RX AUXILIARY LENGTH REGISTER, 0x2195)				
7		Reserved	R/W	0
6:0	RXAL	Represents the length used in the AES operation for the received packet. It has a different meaning for each security mode as follows. **Security mode: CTR** – It represents the number of bytes between length byte and the data to be encoded or decoded of data in FIFO. **Security mode: CBC-MAC** – It represents the number of bytes between length byte and the data to be authenticated. **Security mode: CCM** – It represents the length of the data which is used not in encoding or decoding but in authentication.	R/W	0x00

1.9 PHYSICAL LAYER (PHY)

The Physical Layer (PHY), also called the modem block, is used as follows:

- With the MAC block, the data to be transmitted is digitally modulated and then sent to the RF block for transmission.
- With the MAC block, the RF signal received via the RF block is digitally demodulated and sent to the MAC block.

The modulation starts by fetching the data in the TX FIFO. After appending the preamble, SFD and length field to the data, a frame, which is compatible to IEEE802.15.4 standard, is generated. This frame is mapped to symbols via Bit-to-Symbol conversion as shown in Figure 31 below. Bit-to-Symbol conversion maps 4 bit to 1 symbol. Each symbol is spread by Symbol-to-Chip mapping. The Spread symbol is then modulated to a quadrature signal of constant envelope via the Offset Quadrature Phase Shift Keying (O-QPSK) modulation and the Half Sine Wave Filtering.
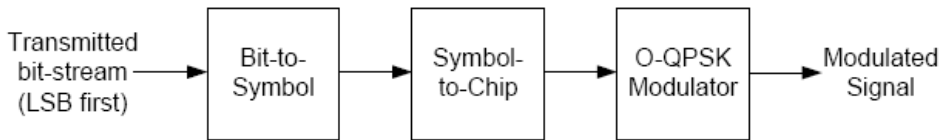
Figure 31 – IEEE 802.15.4 Modulation

Symbol-to-Chip mapping is used for spreading the symbol bandwidth to improve the reception performance. Table 37 shows the mapping rule of chip sequences corresponding to each symbol.

Table 37 – Spreading sequence of 32-chip

Symbol	Chip Sequence (C_0, C_1, C_2, …, C_{31})
0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 1 1 1 0 1 1 1 1 1 0 1 1
9	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 1 1 1 0 1 1 1
10	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
11	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

Figure 32 shows the quadrature signal modulated.
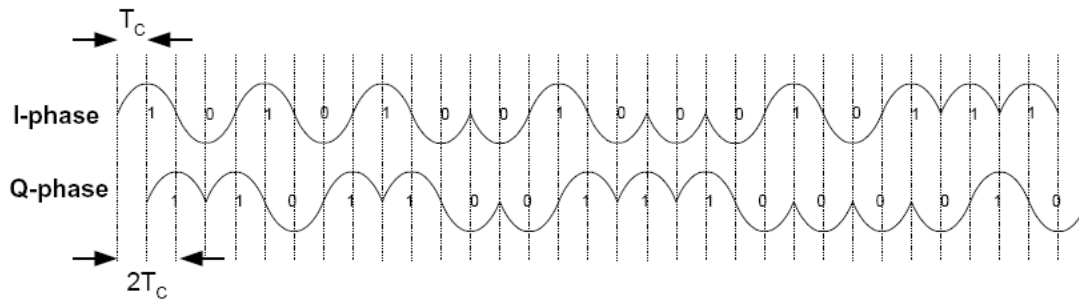
Figure 32 – Quadrature Modulated Signal

The modulated signal is converted to analog by the DAC and then passed to RF block.

The output signal of the DAC is fed to the Quadrature (I/Q) Up-conversion Mixer through the Low Pass Filter (LPF) and then amplified by the Power Amplifier (PA) and transmitted to the antenna.

When an RF signal is received by the antenna, it is amplified by the Low Noise Amplifier (LNA) in the RF block. It is then down-converted to a base-band signal by the Quadrature Down-conversion Mixer. After low pass filtering, the analog signal is amplified through the Variable Gain Amplifier (VGA), and converted to a digital signal by the ADC.

The output signal of the ADC is digitally demodulated by the modem block. Digital demodulation process includes for example, Automatic Gain Control (AGC), De-spreading, Symbol Detection, and Timing Synchronization. When a frame delimiter is detected on the demodulated signal, a modem block generates the interrupt which indicates the start of a packet.

The length and the frame body followed by frame delimiter are stored in RX FIFO of MAC. When the last data is stored, an interrupt is generated to indicate the end of packet reception. After a packet reception interrupt occurs, a user can read the data in TX FIFO by software.

When a packet is received, a modem block provides Received Signal Strength Indication (RSSI) automatically. RSSI is measured by averaging the power level of received signal for a defined period of time.

It can be used as a Link Quality Indicator (LQI) to decide the quality of the communication channel.

RSSI is stored in a special register and the stored RSSI value is kept until a new packet is received. After a packet reception interrupt occurs, a user can read the value stored in RSSI register by software. While a packet is not being received, the modem block continuously provides the RSSI of the RF signal at antenna. Measured RSSI is used to decide the communication channel state. Clear Channel Assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple-users try to use a channel simultaneously. When a channel is determined to be busy, packet transmission is deferred until the channel state changes to idle.

1.9.1   INTERRUPT

The modem block provides four interrupts to notify the MCU of specific events:

- **RX End Interrupt (RXEND_INT)**

This interrupt notifies the MCU of the completion of a packet reception. When this interrupt has been generated, the user can check the received data in the RX FIFO.

Also, the quality of the transmission channel is checked by reading this register, which stores the RSSI information of the received packet.

- **RX Start Interrupt (RXSTART_INT)**

This interrupt notifies the MCU of the start of a packet reception. When the packet reception has been started, all the reception is processed by the hardware.

Note: It is recommended that the RX Start Interrupt is not used.

- **TX End Interrupt (TXEND_INT)**

This interrupt notifies the MCU of the completion of a packet transmission. A new packet cannot be transmitted until a packet transmission is completed. When a communication channel is busy, a TX End Interrupt can be delayed until a communication channel goes to the idle state and the transmission is completed successfully

- **Modem Ready Interrupt (MDREADY_INT)**

This interrupt notifies the MCU that the modem block has changed from the idle state to the ready state due to the modem-on request. The modem block is in the idle state when the supply power is turned on but needs to be changed to the ready state in order to transmit or receive the packet. This interrupt occurs when the RF block has stabilized following the modem-on request.

The user can check whether each interrupt described above occurs through the INTSTS register.   The INTCON register can be set to disable any of the interrupts desired.

The modem block provides the INTIDX register with information from the INTSTS register to check whether an interrupt has occurred. When multiple interrupts occur simultaneously, INTSTS register will show all the interrupts that have occurred. The INTIDX register notifies whether an interrupt is enabled in the order based on the priority of the interrupt. When a user reads the INTSTS or INTIDX register, all interrupts are initialized.

1.9.2   REGISTERS

The registers of the modem block either control or report the state of the modem. The registers, which influence transmission performance of the modem block, should be set with the values provided by CEL, and should not be modified by a user's application program.

Table 38 lists the registers in the PHY Layer of the ZIC2410. The address of each register is assigned to a data memory area in the microcontroller, so a user application program can read and write the register as a general memory.

Table 38 – PHY Register Address Map

Address (Hex)	Name	Description	Initial Value
2200	**PCMD0**	PHY Command0	11111100
2201	**PCMD1**	PHY Command1	11000111
2202	**PLLPD**	PLL Power-Down	11100000
2203	**PLLPU**	PLL Power-Up	11111111
2204	**RXRFPD**	RF RX Path Power-Down	00000000
2205	**RXRFPU**	RF RX Path Power-Up	11111111

Address (Hex)	Name	Description	Initial Value
2206	TXRFPD	RF TX Path Power-Down	11010000
2207	TXRFPU	RF TX Path Power-Up	11111111
220D	TRSWBC	TRSWB Control	00000000
2211	RXFRM1	RX Frame Format1	00000010
2212	SYNCWD	SYNC Word Register	10100111
2213	TDCNF0	Operation Delay Control 0	01001111
2217	TDCNF1	Operation Delay Control 1	01100011
2215	TXFRM1	TX Frame Format1	11110010
2223	AGCCNF3	AGC Configuration3	01111111
2248	CCA0	CCA Control0	11000000
2249	CCA1	CCA Control1	10110010
224A	CCA2	CCA Control2	00000001
224B	CCA3	CCA Control3	11110100
2260	TST	Test Register	10000000
2261	TST1	Test Configuration1	01101100
2262	TST2	Test Configuration2	11111111
2263	TST3	Test Configuration3	00001111
226D	TST13	Test Configuration13	00000000
226E	TST14	Test Configuration14	01000000
2270	PHYSTS0	PHY Status0	10000000
2271	PHYSTS1	PHY Status1	11110000
2272	AGCSTS0	AGC Status0	11111111
2273	AGCSTS1	AGC Status1	11011111
2274	AGCSTS2	AGC Status2	00000000
2275	AGCSTS3	AGC Status3	00000000
2277	INTCON	PHY Interrupt Control	11110000
2278	INTIDX	PHY Interrupt Status and Index	11111100
227E	INTSTS	PHY Interrupt Status	11111111
220D	TRSWC0	TRSW Control 0	00000000
2279	TRSWC1	TRSW Control 1	10010000
2286	PLL0	PLL Frequency Control 0	00111000
2287	PLL1	PLL Frequency Control 1	01000000
2288	PLL2	PLL Frequency Control 2	00000000
228B	PLL3	PLL Frequency Control 3	00110010
2289	PLL4	PLL Frequency Control 4	00101111
228A	PLL5	PLL Frequency Control 5	00010100
22A0	TXPA0	TX PA Control 0	00011000
22A1	TXPA1	TX PA Control 1	11111000
22A2	TXPA2	TX PA Control 2	10010110

Table 39 describes each of the PHY registers.

Table 39 – PHY Registers

Bit	Name	Descriptions	R/W	Reset Value
PCMD0 (PHY COMMAND0 REGISTER, 0x2200)				
This register is used to control the operation of a modem block.				
7	MDOFF	**Modem-off Request**. When this field is set to '0', the modem block status is changed to OFF. In the OFF state, the RF block is in a power-down state and the modem block is in the reset state. In this state, the ZIC2410 cannot receive or transmit packets. For transmission or reception of a packet, the modem block needs to be changed to the ON state. When the modem block goes to the OFF state, this field is set to '1' automatically by the hardware.	R/W	1
6	MDON	**Modem-on Request**. When this field is set to '0', the modem block status is changed to ON. In the ON state, the RF and modem blocks are in the TX or RX ready state. In this state, the modem block controls power-down or power-up for the transmitter or the receiver without an active user application. When the modem block goes to the ON status, this field is set to '1' automatically by the hardware.	R/W	1
5:4		Reserved		11
3	TXSTP	**Packet Transmission Stop Request**. When this field is set to'0' while a packet is being transmitted, the packet transmisson stops. The modem block changes to the RX ready state after a defined delay .	R/W	1
2	TXREQ	**Packet Transmission Request.** When this field is set to '0', the modem block transmits a packet. When a packet transmission is requested, the modem block changes to the TX ready state after a defined delay. Only when a communication channel is in the idle state (CCA='1'), will the packet be transmitted. When the channel is in the busy state (CCA='0'), the transmission is deferred until the channel state goes to idle. This field is set to'1' automatically by hardware after completing transmission. When the packet transmission is completed successfully, a TXEND-INT interrupt is sent. If the packet transmission is abnormal, the interrupt is not sent and the TXREQ field is set to '1'.	R/W	1
1	TXON	**TX Path On**. With the TXOFF field, enables the modulation circuit. When the TXON field is set to '1', the modulation circuit of the modem block is always enabled. The following table shows whether the modulation circuit is enabled based on the values of the TXON and TXOFF fields. When TXON and TXOFF are both set to '0', the modem block automatically enables the modulation circuit during packet transmission and disables the modulation circuit during packet reception. It is recommended that both TXON and TXOFF field be set to '0' **TXON / TXOFF / Modulation Circuit Status** 1 / 1 / Always enabled 1 / 0 / Always enabled 0 / 1 / Always disabled 0 / 0 / Enabled or disabled depending on the control of a modem block.	R/W	0
0	RXON	**RX Path On.** With the RXOFF field, enables the demodulation circuit. When RXON field is set to '1', the demodulation circuit of a modem block is always enabled. The following table shows the status of the demodulation circuit, based on the values of the RXON and RXOFF fields. When RXON and RXOFF are set to '0', the modem block automatically enables the demodulation circuit during packet reception and disables the demodulation circuit during packet transmission. **RXON / RXOFF / Demodulation Circuit Status**	R/W	0

Bit	Name	Descriptions			R/W	Reset Value
		1	1	Always enabled		
		1	0	Always enabled		
		0	1	Always disabled		
		0	0	Enabled or disabled depending on the control of a modem block		
PCMD1 (PHY COMMAND1 REGISTER, 0x2201) This register is used to control the operation of the modem block.						
7:6		Reserved				11
5	**DECS**	**Decryption Start.** When DECS field is set to '1', the decryption is processed by the MAC block. When the encrypted packet is received, the data stored in the RX FIFO should be decrypted. The decrypted data is stored in the RX FIFO again. When the decryption is completed, an interrupt is sent to the MAC block. The setting of the DECS field is not cleared automatically after completing decryption and therefore, should be cleared by the software.			R/W	0
4	**ENCS**	**Encryption Start** When ENCS field is set to '1', the encryption is processed by the MAC block. When the transmission of secured packet is required, the data stored in the TX FIFO should be encrypted. The encrypted data is stored in the TX FIFO again. When the encryption is completed, the interrupt occurs at the MAC block. The setting of the ENCS field is not cleared automatically after completing encryption and therefore, should be cleared by the software.			R/W	0
3:2		Reserved				01
1	**TXOFF**	**TX Path Off**. It is used to disable the modulation circuit with the TXON field. When the TXON field is set to '0' and the TXOFF field is set to '1', the modulation circuit of the modem block is always disabled.			R/W	1
0	**RXOFF**	**RX Path Off**. It is used to disable the modulation circuit with the RXON field. When RXON field is set to '0' and RXOFF field is set to '1', the modulation circuit of a modem block is always disabled.			R/W	1
PLLPD (PLL POWER-DOWN REGISTER, 0x2202) This register is used to control the power-down of the circuits related to the Phase-locked Loop (PLL)						
7:5		Reserved				111
4	**PLLRS TS**	**PLL Reset**: The PLLRSTS field is used to reset the PLL circuit. When the PLLRSTS field is set to '0'and the PLLRSTC field is set to '1', PLL circuit held in reset. The following table shows PLL circuit reset state based on the values of the PLLRSTC and PLLRSTS fields.			R/W	0

PLLRSTS	PLLRSTC	PLL reset state
1	1	Controlled by the modem block
1	0	Always in non-reset
0	1	Always in reset
0	0	Always in non-reset

Bit	Name	Descriptions	R/W	Reset Value
3	**VCOBP D**	**Voltage Controlled Oscillator Buffer Power-down**. The VCOBPD and VCOBPDU fields control the power-down state of the Voltage Controlled Oscillator (VCO) Buffer circuit. In power-down state, the VCO Buffer circuit is disabled and draws no current. When the VCOBPU field is set to '1' and the VCOBPD field is set to '0', the VCO Buffer circuit is in the power-down state. The following table shows the VCO buffer circuit state based on the values of the VCOBPD and VCOBPU fields.	R/W	0

VCOBPD	VCOBPU	VCO Buffer reset state
1	1	Controlled by the modem block
1	0	Always in power-up state
0	1	Always in power-down state
0	0	Always in power-up state

Bit	Name	Descriptions	R/W	Reset Value
2	VCOPD	**Voltage Controlled Oscillator Power-down**. With the VCOPU field, controls the power-down state of the Voltage Controlled Oscillator (VCO) circuit. In power-down state, VCO circuit is disabled and draws no current. When the VCOPU field is set to '1' and the VCOPD field is set to'0', the VCO circuit is in the power-down state. The following table shows the VCO circuit state based on the values of the VCOPD and VCOPU fields. | VCOPD	VCOPU	VCO state
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state
0	0	Always power-up state		R/W	0
1	DIVPD	**Divider Power-down**. With the DIVPU field, controls the power-down state of the Divider circuit. In power-down state, the Divider circuit is disabled and draws no current. When the DIVPU field is set to '1' and the DIVPD field is set to'0', the Divider circuit is in the power-down state. The following table shows the Divider circuit state based on the values of the DIVPD and DIVPU fields. | DIVPD	DIVPU	Divider state
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state
0	0	Always power-up state		R/W	0
0	CPPD	**Charge Pump Power-down**. With the CPPU field, controls the power-down state of the Charge Pump (CP) circuit. In the power-down state, the CP circuit is disabled and draws no current. When the CPPU field is set to '1' and the CPPD field is set to'0', the CP circuit is in power-down state. The following table shows the CP circuit state based on the values of the CPPD and CPPU fields. | CPPD	CPPU	CP state
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state
0	0	Always power-up state.		R/W	0
PLLPU (PLL POWER-UP REGISTER, 0x2203) This register is used to control the power-up of circuits related to Phase-locked Loop (PLL)				
7:5		Reserved		111
4	PLLRSTC	**PLL Reset Clear**. PLLRSTC field is used to release the reset PLL circuit. When PLLRSTC field is set to '0', the reset of PLL circuit is released.	R/W	1
3	VCOBPU	**Voltage Controlled Oscillator Buffer Power-up**. Controls the power-up state of the VCO Buffer circuit. In the power-up state, the VCO Buffer circuit is enabled. When the VCOBPU field is set to '0', the VCO Buffer circuit is in power-up state. See VCOBPD above for truth table.	R/W	1
2	VCOPU	**Voltage Controlled Oscillator Power-up**. Controls the power-up state of the VCO circuit. In the power-up state, the VCO circuit is enabled. When the VCOPU field is set to '0', the VCO circuit is in a power-up state. See VCOPD above for truth table.	R/W	1
1	DIVPU	**Divider Power-up**. Controls the power-up state of the Divider circuit. In the power-up state, the Divider circuit is enabled. When the DIVPU field is set to '0', the Divider circuit is in the power-up state. See DIVPD above for the truth table.	R/W	1

Bit	Name	Descriptions	R/W	Reset Value
0	**CPPU**	**Charge Pump Power-up**. Controls the power-up state of the CP circuit. In the power-up state, the CP circuit is enabled. When the CPPU field is set to '0', the CP circuit is in a power-up state. See CPPD above for truth table.	R/W	1
RXRFPD (RF RX PATH POWER-DOWN REGISTER, 0x2204) This register is used to power down circuits related to reception in RF block.				
7	**LNAPD**	**Low Noise Amplifier Power-down.** With the LNAPU field, controls the power-down state of the LNA circuit. In the power-down state, the LNA circuit is disabled and draws no current. When the LNAPU field is set to '1' and the LNAPD field is set to'0', the LNA circuit is in the power-down state. The following table shows the LNA circuit state based on the values of the LNAPD and LNAPU fields. 	**LNAPD**	**LNAPU**	**LNA state**	 	1	1	Controlled by the modem block	 	1	0	Always power-up state.	 	0	1	Always power-down state	 	0	0	Always power-up state.		R/W	0
6	**RMIXPD**	**RX Mixer Power-down**. With the RMIXPU field, controls power-down state of the RX Mixer circuit. In the power-down state, the RX Mixer circuit is disabled and draws no current. When the RMIXPU field is set to '1' and the RMIXPD field is set to'0', the RX Mixer circuit is in the power-down state. The following table shows the RX Mixer circuit state based on the values of the RMIXPD and RMIXPU fields. 	**RMIXPD**	**RMIXPU**	**RX Mixer state**	 	1	1	Controlled by the modem block	 	1	0	Always power-up state.	 	0	1	Always power-down state	 	0	0	Always power-up state		R/W	0
5	**BBAMPPD**	**Base-band Analog Amplifier Power-down**. With the BBAMPPU field, controls the power-down state of the Base-band Analog Amplifier (BBAMP) circuit. In the power-down state, the BBAMP circuit is disabled and draws no current. When the BBAMPPU field is set to '1' and the BBAMPPD field is set to'0', the BBAMP circuit is in the power-down state. The following table shows the BBAMP circuit state based on the values of the BBAMPPD and BBAMPPU fields. 	**BBAMPPD**	**BBAMPPU**	**BBAMP state**	 	1	1	Controlled by the modem block	 	1	0	Always power-up state.	 	0	1	Always power-down state	 	0	0	Always power-up state		R/W	0
4	**RMIXBUFPD**	**RF RX Mixer Buffer Power-down**. With the RMIXBUFPU field, controls the power-down state of the RX Mixer Buffer circuit. In the power-down state, the RX Mixer Buffer circuit is disabled and draws no current. When the RMIXBUFPU field is set to '1' and the RMIXBUFPD field is set to'0', the RX Mixer Buffer circuit is in a power-down state. The following table shows the RX Mixer Buffer circuit state based on the values of the RMIXBUFPD and RMIXBUFPU fields. 	**RMIXBUFPD**	**RMIXBUFPU**	**RX Mixer Buffer state**	 	1	1	Controlled by the modem block	 	1	0	Always power-up state.	 	0	1	Always power-down state	 	0	0	Always power-up state.		R/W	0
3		Reserved and should be fixed to '0'.	R/W	0

Bit	Name	Descriptions	R/W	Reset Value
2	RLPFPD	**RX Low-pass Filter Power-down**. With the RLPFPU field, controls the power-down state of the RX Low-pass Filter (LPF) circuit. In the power-down state, the RX LPF circuit is disabled and draws no current. When the RLPFPU field is set to '1' and the RLPFPD field is set to'0', the RX LPF circuit is in the power-down state. The following table shows the RX LPF circuit state based on the values of the RLPFPD and RLPFPU fields. | RLPFPD	RLPFPU	RX LPF state
---	---	---
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state.
0	0	Always power-up state.		R/W	0
1	VGAPD	**Variable Gain Amplifier Power-down**. With the VGAPU field, controls the power-down state of the Variable Gain Amplifier (VGA) circuit. In the power-down state, the VGA circuit is disabled and draws no current. When the VGAPU field is set to '1' and the VGAPD field is set to'0', the VGA circuit is in the power-down state. The following table shows the VGA circuit state based on the values of the VGAPD and VGAPU fields. | VGAPD	VGAPU	VGA state
---	---	---
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state.
0	0	Always power-up state.		R/W	0
0	ADCPD	**Analog-to-Digital Converter Power-down**. With the ADCPUfield, controls the power-down state of the ADC circuit. In the power-down state, the ADC circuit is disabled and draws no current. When the ADCPU field is set to '1' and the ADCPD field is set to'0', the ADC circuit is in the power-down state. The following table shows the ADC circuit state based on the values of the ADCPD and ADCPU fields. | ADCPD	ADCPU	ADC state
---	---	---
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state.
0	0	Always power-up state.		R/W	0
		**RXRFPU (RF RX PATH POWER-UP REGISTER, 0x2205)** This register is used to power up the circuits related to reception in RF block		
7	LNAPU	**Low Noise Amplifier Power-up**. Controls the power-up state of the LNA circuit. In the power-up state, the LNA circuit is enabled. When the LNAPU field is set to '0', the LNA circuit is in the power-up state. See LNAPD above for truth table.	R/W	1
6	RMIXPU	**RX Mixer Power-up**. Controls the power-up state of the RX Mixer circuit. In the power-up state, the RX Mixer circuit is enabled. When the RMIXPU field is set to '0', the RX Mixer circuit is in the power-up state. See RMIXPD above for truth table.	R/W	1
5	BBAMPPU	**Base-band Analog Amplifier Power-up**. Controls the power-up state of the BBAMP circuit. In the power-up state, the BBAMP circuit is enabled. When the BBAMPPU field is set to '0', the BBAMP circuit is in the power-up state. See BBAMPPD above for truth table.	R/W	1
4	RMIXBUFPU	**RFRX-path Mixer Buffer Power-up**. Controls the power-up state of the RX Mixer Buffer circuit. In the power-up state, the RX Mixer Buffer circuit is enabled. When the RXMIXBUFPU field is set to '0', the RX Mixer Buffer circuit is in the power-up state. See RXMIXBUFPD above for truth table.	R/W	1

Bit	Name	Descriptions	R/W	Reset Value
3		Reserved and should be fixed to '1'.	R/W	1
2	RLPFPU	**RX Low-pass Filter Power-up**. Controls the power-up state of the RX LPF circuit. In the power-up state, the RX LPF circuit is enabled. When the RLPFPU field is set to '0', the RX LPF circuit is in the power-up state. See RLPFPD above for truth table.	R/W	1
1	VGAPU	**Variable Gain Amplifier Power-up**. Controls the power-up state of the VGA circuit. In the power-up state, the VGA circuit is enabled. When the VGAPU field is set to '0', the VGA circuit is in the power-up state. See VGAPD above for truth table.	R/W	1
0	ADCPU	**Analog-to-Digital Converter Power-up**. Controls the power-up state of the ADC circuit. In the power-up state, the ADC circuit is enabled. When the ADCPU field is set to '0', the ADC circuit is in the power-up state. See ADCPD above for truth table.	R/W	1

TXRFPD (RF TX PATH POWER-DOWN REGISTER, 0x2206)
This register is used to power down circuits related to transmission in RF block.

Bit	Name	Descriptions	R/W	Reset Value
7:6		Reserved		11
5	TXUMBUFPD	**TX Up-mixer Buffer Power-down**. With the TXUMBUFPU field, controls the power-down state of the TX Up-mixer Buffer circuit. In the power-down state, the TX Up-mixer Buffer circuit is disabled and draws no current. When the TXUMBUFPU field is set to '1' and the TXUMBUFPD field is set to'0', the TX Up-mixer Buffer circuit is in the power-down state. The following table shows the TX Up-mixer Buffer circuit state based on the values of the TXUMBUFPD and TXUMBUFPU fields. <table><tr><td>**TXUMBUFPD**</td><td>**TXUMBUFPU**</td><td>**TX Up-mixer Buffer state**</td></tr><tr><td>1</td><td>1</td><td>Controlled by the modem block</td></tr><tr><td>1</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>1</td><td>Always power-down state.</td></tr><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table>	R/W	0
4		Reserved		1
3	PAPD	**Power Amplifier Power-down**. With PAPU field, controls the power-down state of the Power Amplifier (PA) circuit. In power-down state, the PA circuit is disabled and draws no current. When the PAPU field is set to '1' and the PAPD field is set to'0', the PA circuit is in the power-down state. The following table shows the PA circuit state based on the values of the PAPD and PAPU fields. <table><tr><td>**PAPD**</td><td>**PAPU**</td><td>**PA state**</td></tr><tr><td>1</td><td>1</td><td>Controlled by the modem block</td></tr><tr><td>1</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>1</td><td>Always power-down state.</td></tr><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table>	R/W	0
2:1	TXUMPD	**TX Up-mixer Power-down**. With the TXUMPU field, controls the power-down state of the TX Up-mixer circuit. In the power-down state, the TX Up-mixer circuit is disabled and draws no current. When the TXUMPU field is set to '3' and then TXUMPD field is set to'0', the TX Up-mixer circuit is in the power-down state. The following table shows the TX Up-mixer circuit state based on the values of the TXUMPD and TXUMPU fields. The values of '1' and '2' are not used in these fields. <table><tr><td>**TXUMPD**</td><td>**TXUMPU**</td><td>**TX Up-mixer state**</td></tr><tr><td>3</td><td>3</td><td>Controlled by the modem block</td></tr><tr><td>3</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>3</td><td>Always power-down state.</td></tr><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table>	R/W	00

Bit	Name	Descriptions	R/W	Reset Value
		others	Others	Reserved		
0	DACPD	**Digital-to-Analog Converter Power-down**. With the DACPU field, controls the power-down state of the Digital-to-Analog Converter (DAC) circuit. In the power-down state, the DAC circuit is disabled and draws no current. When the DACPU field is set to '1' and the DACPD field is set to'0', the DAC circuit is in the power-down state. The following table shows the DAC circuit state based on the values of the DACPD and DACPU fields. | DACPD	DACPU	DAC state
---	---	---
1	1	Controlled by the modem block
1	0	Always power-up state.
0	1	Always power-down state.
0	0	Always power-up state.		R/W	0
TXRFPU (RF TX PATH POWER-UP REGISTER, 0x2207) This register is used to power up the circuits related to transmission in RF block.				
7:6		Reserved		11
5	TXUMB UFPU	**TX Up-mixer Buffer Power-up.** Controls the power-up state of the TX Up-mixer Buffer circuit. In the power-up state, the TX Up-mixer Buffer circuit is enabled. When the TXUMBUFPU field is set to '0', the TX Up-mixer Buffer circuit is in the power-up state. See TXUMBUFPD above for truth table.	R/W	1
4		Reserved		1
3	PAPU	**Power Amplifier Power-up**. Controls the power-up state of the PA circuit. In the power-up state, the PA circuit is enabled. When the PAPU field is set to '0', the PA circuit is in a power-up state. See PAPD above for truth table.	R/W	1
2:1	TXUMP U	**TX Up-mixer Power-up**. Controls the power-up state of the TX Up-mixer circuit. In the power-up state, the TX Up-mixer circuit is enabled. When the TXUMPU field is set to '0', the TX Up-mixer circuit is in the power-up state. See TXUMPD above for truth table.	R/W	1
0	DACPU	**Digital-to-Analog Converter Power-up**. Controls the power-up state of the Digital-to-Analog Converter (DAC) circuit. In the power-up state, the DAC circuit is enabled. When the DACPU field is set to '0', the DAC circuit is in the power-up state. See DACPD above for truth table.	R/W	1
RXFRM1 (RX FRAME FORMAT1 REGISTER, 0x2211) This register is used to set the frame format of RX Packet.				

7:6	RXRAT E	**Receptable RX Packet Rate**. Sets the receptable RX data rate. ZIC2410 supports 250kbps compatible with IEEE802.15.4 standard and 500kbps or 1Mbps extended data rate provided by CEL Inc.
		  0: Supports 250kbps data rate (compatible with IEEE802.15.4 std)
		  1: Supports 250kbps and 500kbps data rates
		  2 or 3: Supports 250kbps and 1Mbps data rates
			R/W	00

5:4	TXRAT E	**Transmission Rate**. Sets the transmisson data rate. ZIC2410 supports 250kbps compatible with IEEE802.15.4 standard and 500kbps or 1Mbps extended data rate provided by CEL Inc.
		  0: Supports 250kbps data rate (compatible with IEEE802.15.4 std)
		  1: Supports 250kbps and 500kbps data rates
		  2 or 3: Supports 250kbps and 1Mbps data rates
			R/W	00

Bit	Name	Descriptions	R/W	Reset Value
3:0	RXPRM LNG	**RX Preamble Length**. Sets the preamble length of the received packet. The ZIC2410 supports a preamble of 8 symbol length defined in the IEEE 802.15.4 std. At the same time, the ZIC2410 provides a configurable preamble length. When 'n' value is set in RXPRMLNG field, the length of the preamble is set to (n+6)symbol. The length of preamble can be varied from 6 to 21 symbols. *Note: The value of this field should be set the same as the TXPRMLNG field. It is recommended to use a default value of '2'*.	R/W	0010

SYNCWD (SYNCWORD REGISTER, 0x2212)
Sets two bytes of data to be used as the Start-of-Frame Delimiter (SFD). IEEE802.15.4 standard uses 2 symbols as an SFD. The 2 symbols are '0xA7'. The '7' is the first of the 2 symbols transmitted.

TDCNF0 (OPERATION DELAY CONTROL 0 REGISTER, 0x2213)
This register sets the delay to power down RF after TX.

Bit	Name	Descriptions	R/W	Reset Value
7:4	TXPDT M	Sets the delay time between a packet transmission and RF TX-path power-down. The delay time is set in 16µs increments. The minimum and maximum values are 0µs and 240µs respectively.	R/W	0100
3:0		Reserved	R/W	1111

TDCNF1 (OPERATION DELAY CONTROL 1 REGISTER, 0x2217)
This register sets the delay for switching between TX and RX.

Bit	Name	Descriptions	R/W	Reset Value
7:4	TXRXT M	Sets the delay time of the transition from TX to RX state. The delay time is set in16µs increments. The minimum and maximum values are 0µs and 240µs respectively.	R/W	0110
3:0	RXTXT M	Sets the delay time of the transition from RX to TX state. The delay time is set in16µs increments. The minimum and maximum values are 0µs and 240µs respectively.	R/W	0011

TXFRM1 (TX FRAME FORMAT1 REGISTER, 0x2215)
This register is used to set the frame format of the TX packet.

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved		1111
3:0	TXPRM LNG	**TX Packet Preamble Length**. Sets the preamble length of the transmission packet. The ZIC2410 supports a preamble of 8 symbol length defined in the IEEE 802.15.4 std. At the same time, the ZIC2410 provides a configurable preamble length. When 'n' value is set in TXPRMLNG field, the length of the preamble is set to (n+6)symbol. The length of preamble can be varied from 6 to 21 symbols. *Note: The value of this field should be set the same as the RXPRMLNG field. It is recommended to use a default value of '2'*.	R/W	0010

AGCCNF3 (AGC CONFIGURATION3 REGISTER, 0x2223)
This register sets AGC operation environment

Bit	Name	Descriptions		R/W	Reset Value
7:5		Reserved			111
4:3	RXEAW S	**RX Energy Accumulator Window size**. AGC calculates the average of the received signal energy for a defined time when measuring RSSI. RXEAWS field is used to set the defined time.		R/W	
		RXEAWS	**Average Calculation Duration**		
		0	16µs		
		1	32µs		
		2	64µs		
		3	128µs		
2:0		Reserved			111

CCA0 (CCA CONTROL CONFIGURATION0 REGISTER, 0x2248)
This register is used to set CCA operation environment.

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved		1

Bit	Name	Descriptions	R/W	Reset Value
6:4	CCAA WS	When CCA uses the energy detection method, it sets the average duration for the received signal energy. 	CCAAWS	Average Calculation Duration	 0 — 1µs 1 — 2µs 2 — 4µs 3 — 8µs others — 16µs	R/W	100
3	CCAFIX	**CCA Indication Lock-up**. Fixes the communication channel state to idle. A com channel state is determined by the CCA circuit in the ZIC2410. When a channel state is busy, a packet is not transmitted. This field allows packet transmission regardless of the channel state. When this field is set to '1', the channel is always in idle state.	R/W	0
2		Reserved		1
1:0	CCAMD	**CCA Indication Mode:** Sets the method to determine the com channel state. The following describes the three methods to detect the channel state. **ED** (Energy Detection): This method determines the channel state as 'busy' when the energy of a received signal is higher than the defined level. **CD** (Carrier Detection): This method determines the channel state as 'busy' when an IEEE802.15.4 carrier is detected. **FD** (Frame Detection): This method determines the channel state as 'busy' when the normal IEEE802.15.4 packet is detected. CCAMD — Method 0 — ED 1 — CD 2 — FD 3 — Reserved	R/W	00

CCA1 (CCA CONTROL CONFIGURATION1 REGISTER, 0x2249) R/W. CCA Decision Threshold.

This register defines threshold of energy level to determine whether a channel state is busy. This register is used only when CCA methods based on energy detection are used. The CCATHRS threshold is stored as a 2's complement integer in dBm. The default value of CCATHRS register is 0xB2 and corresponds to '-78dBm'.

CCA2 (CCA CONTROL CONFIGURATION2 REGISTER) R/W. Energy Calculation Offset(ENRGOFST)

The ZIC2410 and calculates the energy level of the received signal based on the gain of RF block per the following equation.

Equation 4 – Calculation of RX Signal Energy Level
$$\text{Energy Level (dBm)} = \text{CCA2} - \text{RF\_GAIN}$$

As Equation 4 above describes, the CCA2 register compensates for an offset of calculated energy level for the received signal. A user can set the difference between the energy level calculated on a developed system and the real energy level of the received signal in the CCA2 register.

CCA3 (CCA CONTROL CONFIGURATION3 REGISTER, 0x224B)

The small change in energy level may cause some uncertainty in determining the channel state when that state is defined using only the threshold of the CCA1 register.

To prevent that uncertainty, the ZIC2410 can define a hysteresis value to define a minimum drop in energy level to initiate a change in the channel state from busy to the idle state. The CCA3 register is used to set that hysteresis.

Table 40 – CCA3 Registers

Bit	Name	Descriptions	R/W	Reset Value
CCA3 (CCA CONTROL CONFIGURATION3 REGISTER, 0x224B)				
7:4				1111
3:0	CCAHY ST	**CCA Hysteresis Level**: Once the channel is determined to be in a busy state, it can be changed to an idle state only when the calculated energy level is decreased by more than the level defined in the CCAHYST field. The CCAHYST field is stored as a 2's complement integer and the unit is dB.	R/W	0100
TST0 (TEST CONFIGURATION0 REGISTER, 0x2260)				
This register is used to control the test of a modem and RF block.				
7	TSTEN	**Test Enable**: Used to change the ZIC2410 to a test mode. When TSTEN field is set to '0', the modem block controls the RF block according to the test mode which is set by the STAMD and TSTMD fields. The TSTEN field should be set after setting the registers that are required to set up a test mode. In order to set a new test mode, TSTEN field should be set to '1' before setting a new test mode. After that, TESTEN field should be set to '0'.	R/W	1

6:5	STAMD	**Station Mode**. Sets ZIC2410 to a transmitter during a test mode.
		  1: Set as a transmitter
		  2: Set as a receiver
		  3: Set as a transceiver
			R/W	00

4:0	TSTMD	**Test Mode**. Sets a test mode. Refer to the Table 41 for the various modes base on the setting of the STAMD and TSTMD fields.	R/W	00000

Table 41 – Test Mode Setting

Mode	STAMD [1.0]	TSTMD [4]	TSTMD [3:2]	TSTMD [1]	TSTMD [0]	Operation
Single Tone Generation for RF Test	01	0	00	0	0	I=cos, Q=sin single tone generation
	01	0	01	0	0	I=8h80, Q=sin single tone generation
	01	0	10	0	0	I=cos, Q=8h80 single tone generation
	01	0	11	0	0	I=8h80, Q=8h80
	01	1	00	0	0	I=cos, Q=sin single tone generation
	01	1	01	0	0	I=8h80, Q=sin single tone generation
	01	1	10	0	0	I=cos, Q=8h80 single tone generation
	01	1	11	0	0	I=8h80, Q=8h80
				0	0	No operation
Modulated Carrier Generation for RF Test	01	X	XX	1	0	Continuous 802.15.4 Modulated Signal
	others			1	0	No operation

Table 42 – Test Configuration Registers

Bit	Name	Descriptions	R/W	Reset Value
TST1 (TEST CONFIGURATION1 REGISTER, 0x2261) This register defines the fixed symbol to be modulated for generating a test packet. TST1 register sets two fixed symbols.				
7:4	TSTSY ML	**Test Symbol, Low Nibble**. Sets the symbol to be transmitted first in fixed symbols.	R/W	0110
3:0	TSTSY MH	**Test Symbol, High Nibble**. Sets the symbol to be transmitted later in fixed symbols.	R/W	1100
TST2 (TEST CONFIGURATION2 REGISTER, 0x2262) This register sets the inter-packet time interval when the test mode transmits the modulated packet of a random data. The inter-packet time interval is needed for setting-up EVM measurement.				
7:3	IFS	**Inter-frame Space**. Sets the number of the symbols corresponding to the inter-packet time interval in the IFS field. The duration of 1 symbol is 16µs. Therefore, if IFS is set to 'N', inter-packet time interval is set to (16*N) µs. *Note: The defined value of the IFS field is valid only when the TSTMD field is set to '23'.*	R/W	11111
2:0		Reserved		111

TST3 (TEST CONFIGURATION3 REGISTER, 0x2263) R/W.
This register is used to support the generation of a random symbol for the modulation in a test mode. The Random Number Generator (RNG) generates the random number by CRC-16. TST3 register stores the seed for RNG circuit. Any number except '0' can be used as the seed for RNG circuit.

TST13 (TEST CONFIGURATION13 REGISTER, 0x226D) R/W.
This register sets the length of transmitting packet in a test mode. The length of packet can be set from 1 byte to 127 byte and the duration of each packet is from 256µs to 4,256µs.

TST14 (TEST CONFIGURATION14 REGISTER, 0x226E) R/W.
This register sets the frequency of a single-tone in a test mode for transmitting single-tone.

TST14 register can set from a 1/4 frequency of DAC operating clock to a 1/256 frequency of DAC operating clock. This single-tone signal can be used to test RF block characteristics. Cosine and sine signal can be selectively assigned to I-phase or Q-phase of RF block.

The frequency of single-tone is defined by Equation 5.

$$\text{Frequency} = \frac{f_{DAC} \cdot CFRQ}{1024} Hz$$

Equation 5 – Definition of Single-Tone Frequency

Table 43 – PHY Status Registers

Bit	Name	Descriptions	R/W	Reset Value
PHYSTS0 (PHY STATUS0 REGISTER, 0x2270) These registers are used to monitor or control the state of the modulation or demodulation blocks in the modem block.				
7	RXSTS F	**RX Status Lock-up**: Fixes the state of the demodulation block to a defined state. With a desired state in the RXSTS field, setting '0' in the RXSTSF field, caused the state of the demodulation block to be fixed and retained until RXSTSF is set to '1'.	R/W	1
6:4	RXSTS	**RX Block Status**: Shows the state of the demodulation block in a modem block. RXSTS field can read the current state of the demodulation block. This field stores the state to be changed. However, the state of the demodulation block is not changed as a new state is only recorded to this field. In order to be changed to the recorded state, RXSTSF field should be set to '0'. The state in RXSTS field can be different from the recorded state because RXSTS shows the current state of demodulation block which is updated from the recorded state. The following table shows the state in RXSTS. RXSTS='000' — **RX_IDLE:** The demodulation block cannot receive a packet. RXSTS='001' — **RX_PKTD:** The demodulation block is waiting for reception of a packet (RX ready state). RXSTS='010' — **RX_WAIT:** The demodulation block is waiting for the completion of the timing synchronization following packet detection. RXSTS='011' — **RX_CFE1:** Coarse carrier frequency offset The demodulation block is in the first stage of coarse carrier frequency offset estimation (CFE) waiting for a receive signal adequate for CFE. RXSTS='100' — **RX_CFE2:** The demodulation block is in the second stage of CFE estimating the coarse offset of the carrier frequency. RXSTS='101' — **RX_SYMD1:** The demodulation block is in the first stage of symbol detection (SYMD) waiting for a receive signal adequate for SYMD. RXSTS='110' — **RX_SYMD2**: The demodulation block is in the second stage of the SYMD detecting the symbol from the received signal. RXSTS='111' — **RX_PKTEND**: The demodulation block ends a successful packet reception.	R/W	000
3:0	TXSTS	**TX Block Status**. This field shows the state of the modulation block in the modem block. TXSTS field can read the current state of the modulation block. This field stores the state to be changed. However, the state of the modulation block is not changed as a new state is only recorded to this field. In order to be changed to the recorded state, TXSTSF field should be set to '0'. The state in TXSTS field can be different from the recorded state because TXSTS shows the current state of modulation block. The following table shows the state in TXSTS.	R/W	0000

Bit	Name	Descriptions		R/W	Reset Value
		TXSTS='0000'	**TX_IDLE:** The modulation block cannot transmit a packet.		
		TXSTS='0001'	**TX_WAIT1:** The modulation block is waiting for the TX FIFO to be ready before packet transmission.		
		TXSTS='0010'	**TX_WAIT2:** The modulation block is waiting for the TX FIFO to be ready before packet transmission.		
		TXSTS='0011'	**TX_CHK:** In TX_WAIT1 state, the modulation block checks the validity of the transmission packet length.		
		TXSTS='0100'	**TX_PRM:** In TX_PRM state, the modulation block transmits the SFD.		
		TXSTS='0101'	In TX_SFD state, the modulation block transmits the SFD.		
		TXSTS='0110' TXSTS='0111'	**TX_TAIL:** In TX_LNG state, the modulation block transmits the length.		
		TXSTS='1000'	**TX_BDY:** In TX_BDY state, the modulation block transmits the frame body of transmission packet.		
		TXSTS='1001'	**TX_TAIL:** In TX_TAIL state, the modulation block transmits the tail data of frame body.		
		TXSTS='1010'	**TX_CONT:** In TX_CONT, the modulation block transmits the modulated signal for a test mode.		
		TXSTS='111'	Reserved		
PHYSTS1 (PHY STATUS1 REGISTER, 0x2271) This register is used to monitor or control the state of a modem block.					
7	**TXSTSF**	**TX Status Lock-up**. Fixes the state of the modem block to a defined state. With a desired state in the TXSTS field, setting '0' in the RXSTSF field, caused the state of the demodulation block to be fixed and retained until TXSTSF is set to '1'.		R/W	1
6:5		Reserved		R/W	11
4	**MDSTSF**	**Modem Status Lock-up**. Fixes the state of the modem block to a defined state. With a desired state in the MDSTS field, setting '0' in the MDSTSF field, caused the state of the demodulation block to be fixed and retained until MDSTSF is set to '1'.		R/W	1
3:0	**MDSTS**	**Modem State**. Shows the state of the modem block. MDSTS field can read the current state of the modem block. When a new state is recorded in this field, it is stored. The state of the modem block is not changed when only recording a state in MDSTS field. In order to be changed to the recorded state, MDSTSU or MDSTSF field should be set to '0'. The state in MDSTS field can be different from the recorded state because MDSTS shows the current state of the modem block. Table 44 shows the state in MDSTS.		R/W	0000

Table 44 – MDSTS Field

MDSTS='0000'	**MD_IDLE:** In MD_IDLE state, the modem block is in idle state. The modem block cannot transmit or receive a packet. The modem block consumes the minimum current. The transmission or reception of a packet is available only when the modem block is in a modem ready state.
MDSTS='0001'	**MD_DCCAL:** In MD_DCCAL state, it does the calibration of DC cancellation block. After calibration, PLL is powered-up PLL automatically.
MDSTS='0010'	**MD_WAITON:** In MD_WAITON state, the modem block is in midterm to a modem ready state and waits the stabilization of the supply power to PCC circuit.
MDSTS='0011'	**MD_WAITLCK:** In MD_WAITLCK state, the PLL is waiting to be locked.
MDSTS='0100'	**MD_RDY:** In MD_RDY state, the modem block is in already state. The supply power to PLL circuit is stabilized and the PLL is locked.
MDSTS='0101'	**MD_TXCAL:** In MD_TXCAL state, the modem block is waiting for the transmitter of the RF block to be stabilized before the packet transmission. After the stabilization, the state of the modem block is changed to MD_TXPKT state.
MDSTS='0110'	**MD_TXPKT:** In MD_TXPKT state, the modem block transmits a packet.
MDSTS='0111'	**MD_RXCAL.** In MD_RXCAL state, the modem block is waiting for the receiver of the RF block to be stabilized before the packet reception. After the stabilization, the state of the modem block is changed to MD_RXON state.
MDSTS='1000'	**MD_RXON:** In MD_RXON state, the modem block is waiting for the reception of a packet. During this state, the modem block continuously monitors the reception of a packet.
MDSTS='1001'	**MD_RXPKT:** In MD_RXPKT state, the modem block performs the demodulation of the received packet. After the completion of the packet reception, the state of the modem block is changed to MD_RXON state.
MDSTS='1010'	Reserved
MDSTS='1011'	**MD_RFTST.** In MD_RFTST state, the modem block works in a selected test mode.
MDSTS='1100'	**MD_IFS.** In MD_IFS state, the modem block is ready for transmitting the next packet after the completion of a packet transmission in a test mode.
MDSTS='1101'	**MD_CLR.** In MD_CLR state, the modem block ends the packet transmission and sets TXREQ field to '1' automatically. The state of the modem block is changed to MD_RXON state when TXREQ field is set to '1'.
MDSTS='1110' MDSTS='1111'	Reserved

Table 45 – AGC Status Registers

<u>Bit</u>	<u>Name</u>	Descriptions	<u>R/W</u>	<u>Reset Value</u>
AGCSTS0 (AGC STATUS0 REGISTER, 0x2272) This register is used to monitor and control the gain of LNA or RX Mixer in RF block.				
7	**MGF**	**Mixer Gain Lock-up**. Sets the gain of RX Mixer to a fixed value recorded in the MG field. When the MGF field is set to '0', the RX Mixer gain is set to the value recorded in the MG field. Only when the MGF field is set to '1', can the RX Mixer gain be adjusted by the AGC block.	R/W	1
6	**LGF**	**LNA Gain Lock-up**. Sets the gain of LNA to a fixed value recorded in the LG field. When the LGF field is set to '0', LNA gain is set to the value recorded in the LG field. Only when LGF field is set as '1', can the LNA gain be adjusted by the AGC block.	R/W	1
5	**MG**	**RX Mixer Gain**. Used to monitor the RX Mixer gain set by AGC block. The RX Mixer gain with MG='1' is 25 dB higher than with MG='0'. When the value of the MGF field is '0', the MG field sets the gain of RX Mixer.	R/W	1

4	LG	**LNA Gain**. Used to monitor the LNA gain set by AGC block. The LNA gain with LG='1' is 25 dB higher than with LG='0'. When the value of the LGF field is '0', the LG field sets the gain of the LNA.	R/W	1
3:0		Reserved		1111

AGCSTS1 (AGC STATUS1 REGISTER, 0x2273)
This registers is used to monitor and control the gain of the VGA in the RF block.

7	VGF	**VGA Gain Lock-up**. Sets the gain of the VGA as a fixed value recorded in the VG field. When the VGF field is set to '0', the VGA gain is set to the value recorded in the VG field. Only when the VGF field is set to '1', can the VGA gain be adjusted by the AGC block.		R/W	1
6:1	VG	**VGA Gain.** Used to monitor the VGA gain set by the AGC block. The VGA consists of three stages and the gain of the VGA can be set from 0 to 63dB in 1 dB steps. When the value of the VGF field is '0', the VG field sets the gain of the VGA.		R/W	101111
		VG[1:0]	Stage 1 gain (0 ~ 3dB) '00' : 0dB '01' : 1dB '10' : 2dB '11' : 3dB		
		VG[3:2]	Stage 2 amplifier gain (0 ~ 12dB) '00' : 0dB '01' : 4dB '10' : 8dB '11' : 12dB		
		VG[5:4]	Stage 3 amplifier gain (0 ~ 32dB) '00' : 0dB '01' : 16dB '10' : 32dB '11' : reserved		
0		Reserved			1

AGCSTS2 (AGC STATUS2 REGISTER, 0x2274) R/W.
This register stores the average energy level of the received RF signal at antenna. The stored energy level is the average of the received signal energy which is measured for the time interval defined in RXEAWS field. The indicated value at AGCSTS2 register is stored as a 2's complement integer in dBm.

AGCSTS3 (AGC STATUS3 REGISTER, 0x2275) R/W.
This register stores the average energy level of the received packet. AGCSTS2 register indicates the average of received signal's energy level for a defined time interval. AGCSTS3 register shows the energy level of the last received packet. The value in AGCSTS3 register is retained until another packet is received.

Table 46 – Interrupt Control, Status, and Index Registers

Bit	Name	Descriptions	R/W	Reset Value
INTCON				

Bit	Name	Descriptions	R/W	Reset Value
INTCON (PHY INTERRUPT CONTROL REGISTER, 0x2277) This register is used to mask off the interrupt of a modem block				
7:4		Reserved		111
3	**RXEND MSK**	**RXEND_INT Interrupt Mask**. This field masks RXEND_INT off. When RXENDMSK field is set to '0', RXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet reception.	R/W	0
2	**RXSTM SK**	**RXSTART_INT Interrupt Mask**. This field masks RXEND_START off. When RXSTMSK field is set to '0', RXSTART_INT interrupt is not generated. RXSTART_INT is not a mandatory interrupt. It is recommended to mask off RXSTART_INT interrupt when the rapid packet reception is needed.	R/W	0
1	**TXEND MSK**	**TXEND_INT Interrupt Mask**. This field masks TXEND_INT off. When TXENDMSK field is set to '0', TXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet transmission.	R/W	0
0	**MRDYM SK**	**MDREADY_INT Interrupt Mask**. This field masks MDRDY_INT off. When MRDYMSK field is set to '0', MDRDY_INT interrupt is not generated. This interrupt should be used to check whether a modem block is ready for transmission /reception or not.	R/W	0
INTIDX (PHY INTERRUPT STATUS AND INDEX REGISTER, 0x2278) This register is used to indicate the kinds of the interrupt when it occurs				
7:5		Reserved		111
4	**FRMDX**	**Reception of Extended Transfer Rate Packet**. Indicates the data rate of the received packet when an RXEND_INT interrupt occurs. When FRMDX field is set to '0' and RXRATE field in RXFRM1 register is '1', it indicates a packet reception data rate of 500kbps. When RXRATE field is '2', it indicates the packet reception data rate of 1Mbps.	R/W	1
3	**ALLINT CLR**	**All Interrupt Clear**. Disables all interrupts when they occur. This field clears all interrupts occurred. When multiple interrupts occur at the same time, the modem block stores them in a buffer and processes them in order. When INTIDX field is read, the executed interrupts are cleared in order. When ALLINTCLR field is set to '0', all the interrupts in buffer are cleared at the same time.	R/W	1
2		Reserved		1
1:0	**INTIDX**	**Interrupt Table Index**. Shows the kind of the interrupt when an interrupt occurs, in order if multiple interrupts occur simultaneously. The INTSTS field in the INTSTS register should be used for looking through a list of all interrupts that have been triggered. After reading INTIDX field, executed interrupts are cleared automatically. **INTIDX** / **Interrupt** 0 / MDREADY_INT interrupt 1 / TXEND_INT interrupt 2 / RXSTART_INT interrupt 3 / RXEND_INT interrupt	R/W	00
INTSTS (PHY INTERRUPT STATUS REGISTER, 0x227E) This register is used to indicate the kinds of the interrupt when the multiple interrupts occur.				
7:5		Reserved		111
4	**FRMDX**	**Reception of Extended Transfer Rate Packet**. This field is equal to the FRMDX field in the INTIDX register.	R/W	1

Bit	Name	Descriptions	R/W	Reset Value
3:0	INTSTS	**Multiple Interrupt Status**. Shows the interrupt status when multiple interrupts occur concurrently. Each bit in INTSTS field represents the status of a specific interrupt. A Table of Bit vs. Interrupt is shown below.. INTSTS[0] : MDREADY_INT interrupt INTSTS[1] : TXEND_INT interrupt INTSTS[2] : RXSTART_INT interrupt INTSTS[3] : RXEND_INT interrupt When an interrupt is triggered, the INTSTS field corresponding to each interrupt is set to '0'. To clear the executed interrupt, the bit for each of the executed interrupts should be reset to '1' by software.	R/W	1111

TRSWC0 (TX/RX SWITCH CONTROL0 REGISTER, 0x220D) R/W.
This register is used to set two GPIO pins (P1.6, P1.7) as TX/RX switching control pins.

P1.6 and P1.7 can be used to control TX/RX switching when the TRSWC0 register is set to '0x50'. When TRSWC0 is set to '0x00', the two pins are used as GPIO pins. TRSWC1 register should be set the same as TRSWC0 to avoid collision.

TRSWC1 (TX/RX SWITCH CONTROL1 REGISTER, 0x2279) R/W.
This register is used to output TRSW and TRSWB signal at P1.6 and P1.7. TRSW signal remains as a logic '1' during packet transmission and as a logic '0' during packet reception. TRSWB, the complementary signal of TRSW, remains as a logic '0' during packet transmission and as a logic '1' during packet reception. TRSWC1 register should be set to '0x00' to output TRSW and TRSWB signal.

PLL0/1/2/3 (PLL CONTROL 0/1/2/3 REGISTER, 0x2286, 0x2287, 0x2288, 0x228B) R/W.
To modify the PLL offset frequency, refer to Table 47 below.

As shown in Table 47, the delta K correction factor is determined based on the values in the FRAC_K [19:0] registers as follows.

Table 47 – FRAC_K[19:0] Registers

Register Name Offset Frequency	PLL0 Address: 0x2286 FRAC_K [19:12]	PLL1 Address: 0x2287 FRAC_K [11:4]	PLL2 [3:0] Address: 0x2288 FRAC_K [3:0]
1MHz	01	40	0
100kHz	00	20	0
10kHz	00	03	3
1kHz	00	00	5
*195.31Hz	00	00	1

*1LSB = 195.31Hz

* The values of PLL0, PLL1, PLL2 [3:0] in Table 47 are HEX.

When using a 16MHz crystal, the values of PLL0, PLL1 and PLL2 need to be adjusted in order to define the adjustment to the channel frequency as shown in Table 47.

New Frequency = Original Frequency + Frequency Offset. Here, delta K, which is the Frequency Offset, can be derived from the following formula.

$$\text{delta K} = \text{Frequency Offset} / 195.31\text{Hz}$$

The New Frequency can be obtained by converting the delta K calculated above to Hex format and adding it to the value of the registers for the current frequency.

In order to adjust the frequency of channel 26, set PLL3 (0x228B) to 0x32 and then adjust it.

Table 48 – Phase Lock Loop Control Registers

Bit	Name	Descriptions	R/W	Reset Value
PLL4 (PLL CONTROL 4 REGISTER, 0x2289) This register is used to process an automatic frequency calibration (AFC) when changing the locking frequency of the PLL.				
7	AFCST ART	**Automatic Frequency Calibration Start**. Used to request the start of AFC. AFC is processed when the AFCSTART is set to '1'. After the AFC process, the AFCSTART field is automatically cleared to '0'.	R/W	0
6	AFCEN	**Automatic Frequency Calibration Enable**. Used to enable the AFC process and should be set to '1' to run AFC.	R/W	0
5:0		Reserved		111111
PLL5 (PLL CONTROL 5 REGISTER, 0x228A) This register is used to check whether PLL is locked or not.				
7		Reserved	R/W	0
6	PLLOC K	Shows the locking status of PLL circuit. When this field is set to '1', the PLL circuit is locked. When '0', the PLL circuit is not locked.	R/W	0
5:0		Reserved		111111

To change the channel setting, the PLL0, PLL1, PLL2, PLL3, PLL4 registers need to be changed by the following procedure:

1) Change the RF RX-path to the power-down state by setting the RXRFPD register to 00000000.

2) Change the RF TX-path to the power-down state by setting the TXRFPD register to 11010000.
3) Set the values of the PLL0, PLL1, PLL2, PLL3 registers.
4) Start the AFC by setting 11101111 into the PLL4 register.
5) Retain Stand-by state until setting PLLLOCK in PLL5 register to '1'.
6) Change the RF TX-path from the power-down state to the normal state by setting the TXRFPD register to 11111111 after setting the PLLLOCK to '1'.
7) Change the RF RX-path from the power-down state to the normal state by setting the RXRFPD register to 11111111.

TXPA0/1/2 (POWER AMPLIFIER OUTPUT CONTROL REGISTER, 0x22A0/1/2) R/W.
This register determines the power out of the device. For the linear output level, TXPA0, TXPA1 and TXPA2 should be adjusted per the following table.

Table 49 – TX Output Power Settings

TX Output Power Level (dBm)	TXPA0(0xA0)	TXPA1(0xA1)	TXPA2(0xA2)
8	10011111	11111111	01101111
7	10011111	11110101	01101111
6	10011101	11110000	01101111
5	10011111	11101101	01101111
4	10010101	11101101	01101111
3	00011111	11110011	01101111
2	00011111	11101100	01101111
1	00011110	11101010	01101111
0	00011100	11101001	01101111
-5	00011110	11100011	01101111
-7	00011000	11100011	01101111
-10	00011000	11100010	01101111
-15	00010011	11100010	01101111
-20	00010010	11100010	01101110

1.10 IN-SYSTEM PROGRAMMING (ISP)

In-system programming (ISP) function enables a user to download an application program to the internal flash memory. When Power-on, the ZIC2410 checks the value of the MS [2:0] pin. When the value of the MS [2] pin is '1' and the value of the MS [1:0] is '0', ISP mode is selected. The following procedure is to use the ISP function.

1. In MS [2:0] pin, MS [2] should be set to'1'. MS [1] and MS [0] should be set to '0'.
2. Make RS-232 connection with the PC by using the Serialport1.
   The configuration is 8-bit, no parity, 1 stop bit and 115200 baud rate.
3. Power up the device.
4. Execute the ISP program. (It is included in the Development Kit)
5. Load an application program in Intel HEX format.
6. Download.

When the procedure is finished, an application program is stored in the internal flash memory. To execute the application program, a device should be reset after setting MS [2:0] pin to '0'

After reset, the application program in the internal flash memory is executed by the internal MCU.
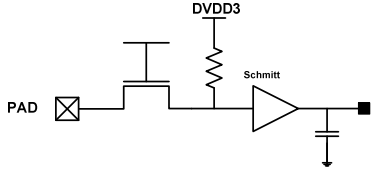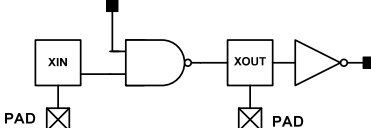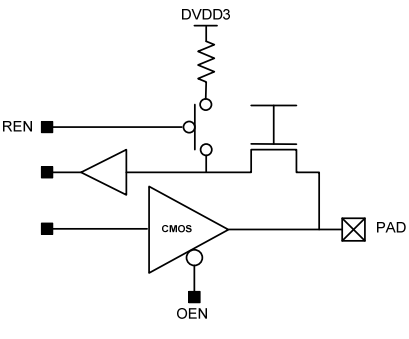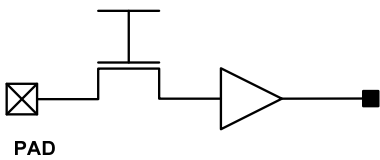
1.11 ZIC2410 INSTRUCTION SET SUMMARY
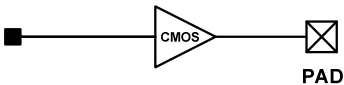
Table 50 – Instruction Set Summary

MNEMONIC	DESCRIPTION	BYTE	CYCLE
ARITHMETIC OPERATIONS			
ADD A, Rn	Add register to Accumulator	1	1
ADD A, direct	Add direct byte to Accumulator	2	1
ADD A, @Ri	Add indirect RAM to Accumulator	1	1
ADD A, #data	Add immediate data to Accumulator	2	1
ADDC A,Rn	Add register to Accumulator with Carry	1	1
ADDC A,direct	Add direct byte to Accumulator with Carry	2	1
ADDC A,@Ri	Add indirect RAM to Accumulator with Carry	1	1
ADDC A,#data	Add immediate data to Accumulator with Carry	2	1
SUBB A,Rn	Subtract register to Accumulator with borrow	1	1
SUBB A,direct	Subtract direct byte to Accumulator with borrow	2	1
SUBB A,@Ri	Subtract indirect RAM to Accumulator with borrow	1	1
SUBB A,#data	Subtract immediate data to Accumulator with borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment direct RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement direct RAM	1	1
INC DPTR	Increment Data Pointer	1	3
MUL AB	Multiply A & B	1	3
DIV AB	Divide A by B	1	10
DA A	Decimal Adjust Accumulator	1	1
LOGICAL OPERATIONS			
ANL A,Rn	AND register to Accumulator	1	1
ANL A,direct	AND direct byte to Accumulator	2	2
ANL A,@Ri	AND indirect RAM to Accumulator	1	1
ANL A,#data	AND immediate data to Accumulator	2	1
ANL direct,A	AND Accumulator to direct byte	2	2
ANL direct,#data	AND immediate data to direct byte	3	2
ORL A,Rn	OR register to Accumulator	1	1
ORL A,direct	OR direct byte to Accumulator	2	2
ORL A,@Ri	OR indirect RAM to Accumulator	1	1
ORL A,#data	OR immediate data to Accumulator	2	1
ORL direct,A	OR Accumulator to direct byte	2	2
ORL direct,#data	OR immediate data to direct byte	3	2
XRL A,Rn	Exclusive-OR register to Accumulator	1	1
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	2
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	2
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	2
CLR A	Clear Accumulator	1	1
CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator Left	1	1
RLC A	Rotate Accumulator Left through the Carry	1	1
RR A	Rotate Accumulator Right	1	1
RRC A	Rotate Accumulator Right through the Carry	1	1

MNEMONIC	DESCRIPTION	BYTE	CYCLE
SWAP A	Swap nibbles within the Accumulator	1	1
DATA TRANSFER			
MOV A,Rn	Move register to Accumulator	1	1
MOV A,direct	Move direct byte to Accumulator	2	1
MOV A,@Ri	Move indirect RAM to Accumulator	1	1
MOV A,#data	Move immediate data to Accumulator	2	3
MOV Rn,A	Move Accumulator to register	1	3
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate data to register	2	2
MOV direct,A	Move Accumulator to direct byte	2	2
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate data to direct byte	3	2
MOV @Ri,A	Move Accumulator to indirect RAM	1	2
MOV @RI,direct	Move direct byte to indirect RAM	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	2	2
MOV DPTR,#data16	Load Data Pointer with a 16-bit constant	3	3
MOVC A,@A+DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A,@A+PC	Move Code byte relative to PC to Accumulator	1	1
MOVX A,@Ri	Move External RAM (8-bit addr) to Accumulator	1	1
MOVX A,@DPTR	Move External RAM (16-bit addr) to Accumulator	1	1
MOVX @Ri,A	Move Accumulator to External RAM (8-bit addr)	1	2
MOVX @DPTR,A	Move Accumulator to External RAM (16-bit addr)	1	1
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with Accumulator	1	2
XCH A,direct	Exchange direct byte with Accumulator	2	2
XCH A,@Ri	Exchange indirect RAM with Accumulator	1	2
XCHD A,@Ri	Exchange low-order Digit indirect RAM with Accumulator	1	2
BOOLEAN VARIABLE MANUPULATION			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	1
ANL C,bit	AND direct bit to Carry	2	2
ANL C,/bit	AND complement of direct bit	2	2
ORL C,bit	OR direct bit to Carry	2	1
ORL C,/bit	OR complement of direct bit to Carry	2	1
MOV C,bit	Move direct bit to Carry	2	1
MOV bit,C	Move Carry to direct bit	2	1
JC rel	Jump if Carry is set	2	2
JNC rel	Jump if Carry is not set	2	2
JB bit.rel	Jump if direct Bit is set	3	2
JNB bit,rel	Jump if direct Bit is Not set	3	3
JBC bit,rel	Jump if direct Bit is set & clear bit	3	3
PROGRAM BRANCHING			
ACALL addr11	Absolute Subroutine Call	2	3
LCALL addr16	Long Subroutine Call	3	3
RET	Return from Subroutine	1	3

MNEMONIC	DESCRIPTION	BYTE	CYCLE
RETI	Return from interrupt	1	3
AJMP addr11	Absolute Jump	2	3
LJMP addr16	Long Jump	3	3
SJMP rel	Short Jump (reletive addr)	2	2
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is Zero	2	2
JNZ rel	Jump if Accumulator is Not Zero	2	2
CJNE A,direct,rel	Compare direct byte to Accumulator and Jump if Not Equal	3	3
CJNE A,#data,rel	Compare immediate to Accumulator and Jump if Not Equal	3	3
CJNE Rn,#data,rel	Compare immediate to register and Jump if Not Equal	3	3
CJNE @Ri,#data,rel	Compare immediate to indirect and Jump if Not Equal	3	3
DJNZ Rn,rel	Decrement register and Jump if Not Zero	2	2
DJNZ direct,rel	Decrement direct byte and Jump if Not Zero	3	2
NOP	No Operation	1	1

1.12 DIGITAL I/O

EQUIVALENT SCHEMATIC	POWER (uW/MHz)	MAX DRIVE (mA)
RESET#		
	4.67	N.A
XOSCI/XOSCO, RTCI/RTCO		
	53.86	N.A
GPIO (P0, P1, P3)		
	82.08	4
MS2,MS1, MS0,MSV		
	3.53	N.A.
TSRW, CSROM#		
	55.67	4

2   AC & DC CHARACTERISTICS

2.1   ABSOLUTE MAXIMUM RATINGS

Table 51 – Absolute Maximum Ratings: ZIC2410 (all packages)

Symbol	Parameter	Rating	Unit
VDD	Chip Core Supply Voltage	-0.3 to 2.0	V
VDDIO	I/O Supply Voltage	-0.3 to 3.6	V
RFIN	Input RF Level	10	dBm
TSTG	Storage Temperature	-40 to 85	°C

Exceeding one or more of these ratings may cause permanent damage to the device.

NOTE: All voltage values are based on V_{SS} and V_{SSIO}.

CAUTION: *ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.*

2.2   DC CHARACTERISTICS

Table 52 – DC Characteristics: ZIC2410 (all packages)

VDD = 1.5 V, VDDIO = 3.0 V, TA (ambient temperature) = 25°C unless otherwise stated.

Symbol	Parameter	min	typ	max	Unit
V_{DD}	Core Supply voltage **NOTE 1** (DVDD, AVDD_VCO, AVDD_RF1, AVDD_DAC, DVDD_XOSC, AVDD, AVDD_CP)	1.35	1.5	2.0	V
V_{DDIO}	I/O Supply voltage (DVDD3V) **NOTE 2**	1.35	3.0	3.3	V
AGND	Chip Ground		0		V
V_{IH}	High level input voltage **NOTE 1**	$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage **NOTE 1**	0		$0.3 \times V_{DD}$	V
V_{OH}	High level output voltage **NOTE 1**	2		V_{DD}	V
V_{OL}	Low level output voltage **NOTE 1**	0		0.4	V
T_A	Air temperature	-40		85	°C

NOTE 1: All voltage values are based on AGND. All input and output voltage levels are TTL-compatible.

NOTE 2: For the I/O Supply Voltage (DVDD3), we recommend using a value that is less than twice that of the Core Supply Voltage.

2.3 ELECTRICAL SPECIFICATIONS

2.3.1 ELECTRICAL SPECIFICATIONS with an 8MHz CLOCK

Table 53 – Electrical Specifications: 8MHz Clock

Temp = 25˚C, VDD=3.0V, Core Voltage[1]=1.5V, MCU Clock=8MHz[2]

Parameter	ZIC2410QN48			ZIC2410FG72			Unit
	min	typ	max	min	typ	max	
Current Consumption							
Active MCU without RX/TX Operation (AES, Peripheral, SADC Disabled)		3.35			3.35		mA
Active MCU with TX Mode (AES, Peripheral, SADC Disabled) @+8dBm Output Power @+7dBm Output Power @+6dBm Output Power @+5dBm Output Power @+4dBm Output Power @+3dBm Output Power @+2dBm Output Power @+1dBm Output Power @+0dBm Output Power		43 41.4 39.8 37.9 35.8 34.2 32.9 31.9 30.6			42.1 40.2 38.5 38.4 34.8 33.2 31.8 30.9 29.7		mA
Active MCU with RX Mode (AES, Peripheral, SADC Disabled)		33.2			33.2		mA
PM1		25			25		µA
PM2		1.7			1.7		µA
PM3		0.3[3]			0.3[3]		µA
AES		2.1			2.1		mA
Peripheral		2.2			2.2		mA
Sensor ADC		1			1		mA
RF Characteristics							
RF Frequency Range	2.400		2.4835	2.400		2.4835	GHz
Transmit Data Rate (Normal Mode[4] – 250kbps)		250			250		kbps
Transmit Data Rate (Turbo Mode – 500kbps)		500			500		kbps
Transmit Data Rate (Premium Mode – 1Mbps)		1000			1000		kbps
Transmit Chip Rate		2000			2000		kChips/s
Output Power		8			8		dBm
Programmable Output Power Range		30			30		dB
Receiver Sensitivity Normal Mode (250kbps) Turbo Mode (500kbps) Premium Mode (1Mbps)		–98 –95 –91			–98 –95 –91		dBm

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[1] AVDD_VCO, AVDD_RF1, AVDD_CP, AVDD_DAC, AVDD, DVDD_XOSC, DVDD

[2] Refer to **Section 1.4** in this document for register setting of MCU clock.

[3] Based on the Teradyne J750 MP(Mass Production) test equipment

[4] ZigBee Standard

Temp = 25°C, VDD=3.0V, Core Voltage[1]=1.5V, MCU Clock=8MHz[2]

Parameter	ZIC2410QN48			ZIC2410FG72			Unit
	min	typ	max	min	typ	max	
Adjacent Channel Rejection							
+5MHz		47			49		dB
−5MHz		47			48.8		
Alternate Channel Rejection							
+10MHz		53			56.1		dB
−10MHz		51			56.8		
Others Channel Rejection							
≥+15MHz		43			52.7		dB
≥−15MHz		42			58.3		
Co-channel Rejection		−9.6			−10.7		dB
Blocking/Desensitization							
± 5 MHz		−42			−45		
± 10 MHz		−36			−42		
± 15 MHz		−46			−48		dBm
± 20 MHz		−35			−40		
± 30 MHz		−42			−43		
± 50 MHz		−45			−46		
Spurious Emission (30Hz~1GHz)		−50			−50		dBm
Spurious Emission (1GHz~2.5GHz)		−40			−40		dBm
Spurious Emission (2.5~12.7GHz)		−50			−50		dBm
2nd Harmonics		−50			−50		dBm
3rd Harmonics		−70			−70		dBm
Frequency Error Tolerance			±200			±200	kHz
Error Vector Magnitude (EVM)		10			9.8		%
Saturation(Maximum Input Level)		5			5		dBm
RSSI Dynamic Range		90			90		dB
RSSI Accuracy		±1.2	+6/−3		±1.2	+6/−3	dB
RSSI Linearity		±0.2	±6		±0.2	±6	dB
RSSI Average Time		128			128		μsec
Frequency Synthesizer							
Phase Noise							
@ ±100KHz offset		−81.9			−80.3		
@ ±1MHz offset		−108.6			−108.8		dBc/
@ ±2MHz offset		−113.3			−113.3		Hz
@ ±3MHz offset		−120.3			−120.4		
@ ±5MHz offset		−124.3			−124.2		
PLL Lock Time		110			110		μsec
PLL Jitter		16			16		psec
Crystal Oscillator Frequency		16			16		MHz
Crystal Frequency Accuracy Requirement	−10		+10	−10		+10	ppm
On-chip RC Oscillator							
Frequency		32.78			32.78		KHz
Sensor ADC							
Number of Bits		8			8		bits

Temp = 25°C, VDD=3.0V, Core Voltage[1]=1.5V, MCU Clock=8MHz[2]

Parameter	ZIC2410QN48			ZIC2410FG72			Unit
	min	typ	max	min	typ	max	
Conversion Time		256			256		μsec
Differential Nonlinearity (DNL)		±1.7			±1.7		LSB
Integral Nonlinearity (INL)		±2.4			±2.4		LSB
Signal to Noise and Distortion Ratio (SINAD)(Sine Input)		51.0			51.0		dB
On-chip Voltage Regulator							
Supply range for Regulator	1.9	3.0	3.6	1.9	3.0	3.6	V
Regulated Output		1.5			1.5		V
Maximum Current			140[5]			140[6]	mA
No Load Current		15			15		μA
Start-up Time		260[7]			260[8]		μsec

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[5] Voltage Regulator Input Voltage=3V, 80mV voltage drop
[6] Voltage Regulator Input Voltage=3V, 80mV voltage drop
[7] 10μF and 100pF load capacitor
[8] 10μF and 100pF load capacitor

2.3.2 ELECTRICAL SPECIFICATIONS with a 16MHz CLOCK

Table 54 – Electrical Specifications: 16MHz Clock

Temp = 25˚C, VDD=3.0V, Core Voltage[9]=1.5V, MCU Clock=16MHz[10]

Parameter	ZIC2410QN48			ZIC2410FG72			Unit
	min	typ	max	min	typ	max	
Current Consumption							
Active MCU without RX/TX Operation (AES, Peripheral, SADC Disabled)		4.6			4.6		mA
Active MCU with TX Mode (AES, Peripheral, SADC Disabled) @+8dBm Output Power @+7dBm Output Power @+6dBm Output Power @+5dBm Output Power @+4dBm Output Power @+3dBm Output Power @+2dBm Output Power @+1dBm Output Power @+0dBm Output Power		46.3 44.6 43.0 43.1 38.9 37.3 36.0 35.1 33.8			45.1 43.2 41.5 41.4 37.8 36.2 34.8 33.9 32.7		mA
Active MCU with RX Mode (AES, Peripheral, SADC Disabled)		36.4			35.2		mA
PM1		25			25		μA
PM2		1.7			1.7		μA
PM3		0.3[11]			0.3[12]		μA
AES		3.1			3.1		mA
Peripheral		2.6			2.6		mA
Sensor ADC		1			1		mA
RF Characteristics							
RF Frequency Range	2.400		2.4835	2.400		2.4835	GHz
Transmit Data Rate (Normal Mode[13] – 250kbps)		250			250		kbps
Transmit Data Rate (Turbo Mode – 500kbps)		500			500		kbps
Transmit Data Rate (Premium Mode – 1Mbps)		1000			1000		kbps
Transmit Chip Rate		2000			2000		kChips/s
Output Power		8			8		dBm
Programmable Output Power Range		30			30		dB
Receiver Sensitivity Normal Mode (250kbps) Turbo Mode (500kbps) Premium Mode (1Mbps)		–98 –95 –91			–98 –95 –91		dBm

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[9] AVDD_VCO, AVDD_RF1, AVDD_CP, AVDD_DAC, AVDD, DVDD_XOSC, DVDD

[10] Refer to **Section 1.4** in this document for register setting of MCU clock.

[11] Based on the Teradyne J750 MP(Mass Production) test equipment

[12] Based on the Teradyne J750 MP(Mass Production) test equipment

[13] ZigBee Standard

Temp = 25˚C, VDD=3.0V, Core Voltage[9]=1.5V, MCU Clock=16MHz[10]

Parameter	ZIC2410QN48			ZIC2410FG72			Unit
	min	typ	max	min	typ	max	
Adjacent Channel Rejection							
+5MHz		47			49		dB
–5MHz		47			48.8		
Alternate Channel Rejection							
+10MHz		53			56.1		dB
–10MHz		51			56.8		
Others Channel Rejection							
≥+15MHz		43			52.7		dB
≥–15MHz		42			58.3		
Co-channel Rejection		–9.6			–10.7		dB
Blocking/Desensitization							
± 5 MHz		–42			–45		
± 10 MHz		–36			–42		
± 15 MHz		–46			–48		dBm
± 20 MHz		–35			–40		
± 30 MHz		–42			–43		
± 50 MHz		–45			–46		
Spurious Emission (30Hz~1GHz)		–50			–50		dBm
Spurious Emission (1GHz~2.5GHz)		–40			–40		dBm
Spurious Emission (2.5~12.7GHz)		–50			–50		dBm
2nd Harmonics		–50			–50		dBm
3rd Harmonics		–70			–70		dBm
Frequency Error Tolerance			±200			±200	kHz
Error Vector Magnitude (EVM)		10			9.8		%
Saturation(Maximum Input Level)		5			5		dBm
RSSI Dynamic Range		90			90		dB
RSSI Accuracy		±1.2	+6/–3		±1.2	+6/–3	dB
RSSI Linearity		±0.2	±6		±0.2	±6	dB
RSSI Average Time		128			128		μsec
Frequency Synthesizer							
Phase Noise							
@ ±100KHz offset		–81.9			–80.3		
@ ±1MHz offset		–108.6			–108.8		dBc/
@ ±2MHz offset		–113.3			–113.3		Hz
@ ±3MHz offset		–120.3			–120.4		
@ ±5MHz offset		–124.3			–124.2		
PLL Lock Time		110			110		μsec
PLL Jitter		16			16		psec
Crystal Oscillator Frequency		16			16		MHz
Crystal Frequency Accuracy Requirement	–10		+10	–10		+10	ppm
On-chip RC Oscillator							
Frequency		32.78			32.78		KHz
Sensor ADC							
Number of Bits		8			8		bits
Conversion Time		256			256		μsec

Temp = 25˚C, VDD=3.0V, Core Voltage[9]=1.5V, MCU Clock=16MHz[10]

Parameter	ZIC2410QN48			ZIC2410FG72			Unit
	min	typ	max	min	typ	max	
Differential Nonlinearity(DNL)		±1.7			±1.7		LSB
Integral Nonlinearity(INL)		±2.4			±2.4		LSB
Signal to Noise and Distortion Ratio (SINAD) (Sine Input)		51.0			51.0		dB
On-chip Voltage Regulator							
Supply range for Regulator	1.9	3.0	3.6	1.9	3.0	3.6	V
Regulated Output		1.5			1.5		V
Maximum Current			140[14]			140[15]	mA
No Load Current		15			15		µA
Start-up Time		260[16]			260[17]		µsec

2.3.3 AC CHARACTERISTICS

Table 55 – Timing Specifications

Parameter	MIN	TYP	MAX	UNIT
Internal MCU Clock Timing (See Error! Reference source not found.)				
t_{XTAL} (Crystal Oscillator Duration)		62.5		ns
t_{SYS} (Internal MCU Clock Duration)		125		ns
t_{CDELAY} (Internal MCU Clock Delay)			0.5	ns
POR Timing (See Figure 34 below.)				
16 t_{XTAL}		16 x 62.5		ns
RESET# Timing (See Figure 35 below.)				
t_{EXTRST} (RESET# Interval)	1			ms
16 t_{XTAL}		16 x 62.5		ns
GPIO Timing (See Figure 36 below.)				
t_{SETUP}	1			ns
t_{HOLD}	1			ns
t_{VALID}			10	ns
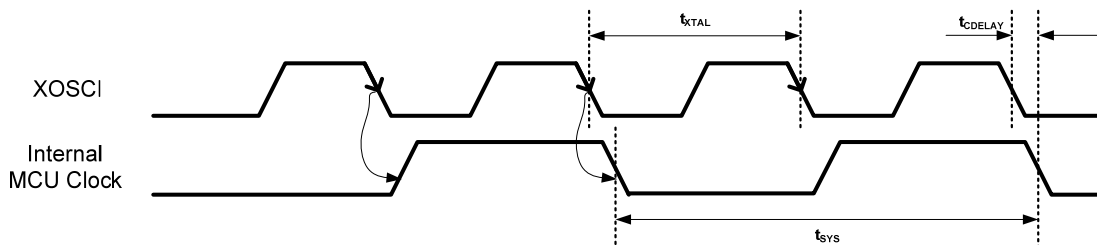
Figure 33 – Internal MCU Clock Timing

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[14] Voltage Regulator Input Voltage=3V, 80mV voltage drop
[15] Voltage Regulator Input Voltage=3V, 80mV voltage drop
[16] 10µF and 100pF load capacitor
[17] 10µF and 100pF load capacitor
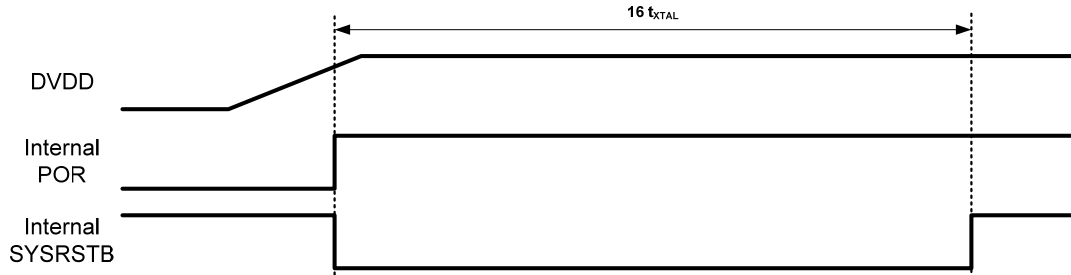
Figure 34 – POR Timing
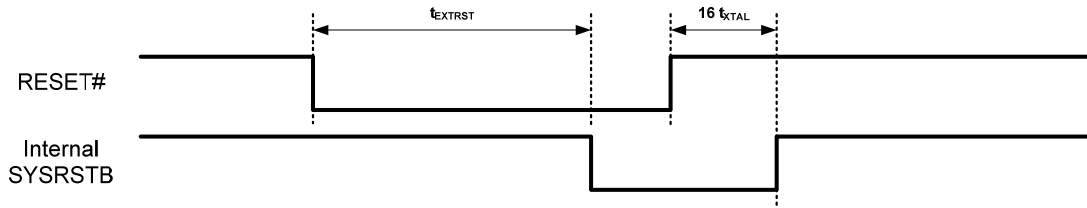
Figure 35 – RESET# Timing
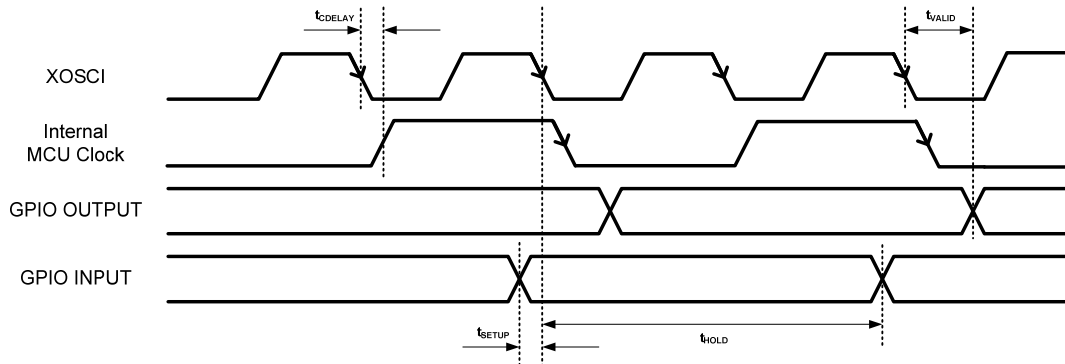
Figure 36 – GPIO Timing

3 PACKAGE & PIN DESCRIPTIONS

3.1 PIN ASSIGNMENTS

3.1.1 QN48 Package
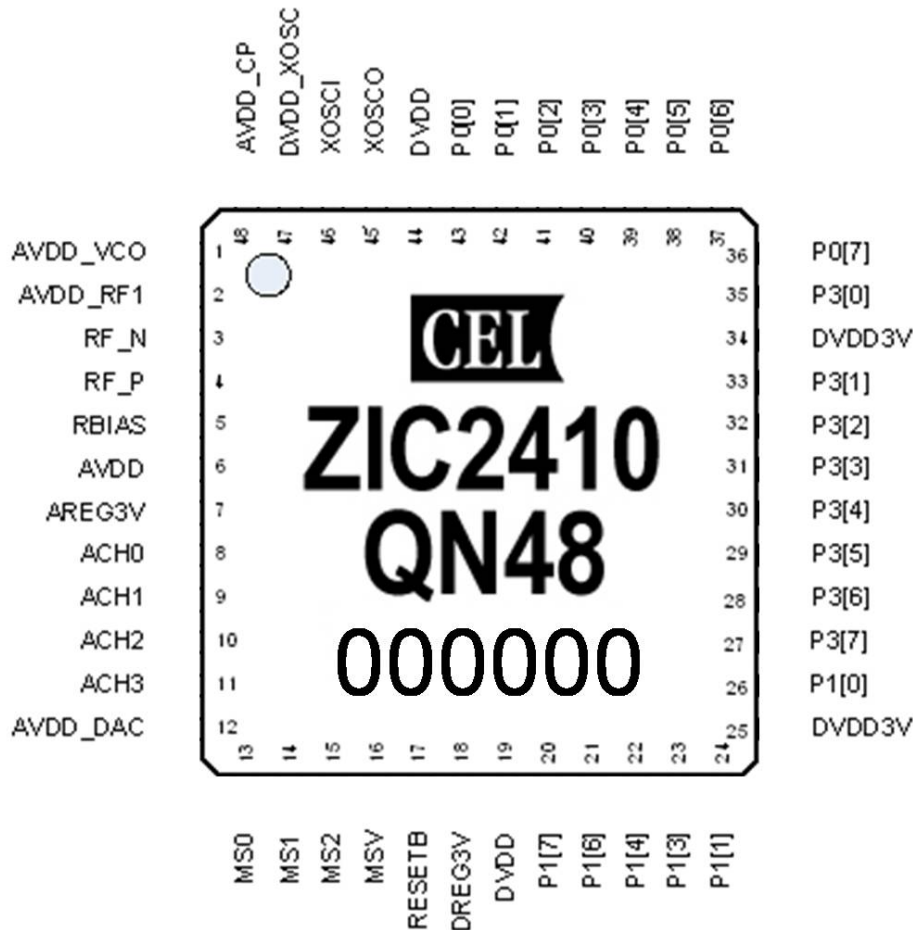
Figure 37 – Pin-out top view of QN48 Package
Chip Ground (GND) is located in the center on the bottom of a chip.

The ZIC2410QN48 Pin-out overview is shown in Table 56.

Table 56 – Pin-out overview; QN48 package

Pin NO.	Pin Name	Pin Type	Pin Description
Exposed bottom	GND	Ground	Ground for RF, Analog, digital core, and IO
1	AVDD_VCO	Power	1.5V Power supply for VCO and Divider
2	AVDD_RF1	Power	1.5V Power supply for LNA and PA
3	RF_N	RF	Negative RF input/output signal to LNA / from PA in receive / transmit mode
4	RF_P	RF	Positive RF input/output signal to LNA / from PA in receive / transmit mode
5	RBIAS	Analog	External bias resistor
6	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA, and LPF (input mode @ No REG)
7	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator
8	ACH0	Analog	Sensor ADC input
9	ACH1	Analog	Sensor ADC input
10	ACH2	Analog	Sensor ADC input
11	ACH3	Analog	Sensor ADC input
12	AVDD_DAC	Power	1.5V Power supply for ADC and DAC

13	MS[0]	I (digital)	MS[2:0] (Mode Select)
			▪ When using Internal Regulator of ZIC2410
			    000: Normal mode
			    001: ISP mode

14	MS[1]	I (digital)	

15	MS[2]	I (digital)	▪ When NOT using Internal Regulator of ZIC2410
			    010: Normal mode
			    110: ISP mode

16	MSV	I (digital)	Mode Select of Voltage 0 – 1.5V
17	RESETB	I (digital)	Reset (Active Low)
18	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator
19	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG)
20	P1[7]	O (digital)	Port P1.7 GPO / P0AND / TRSW
21	P1[6]	I/O (digital)	Port P1.6 / TRSWB
22	P1[4]	I/O (digital)	Port P1.4 / QUADZB / Sleep Timer OSC Buffer Input
23	P1[3]	I/O (digital)	Port P1.3 / QUADZA / Sleep Timer OSC Buffer Output / RTCLKOUT
24	P1[1]	I/O (digital)	Port P1.1 / TXD1
25	DVDD3V	Power	3.0V Power supply for Digital IO
26	P1[0]	I/O (digital)	Port P1.0 / RXD1
27	P3[7]	I/O (digital)	Port P3.7 / 12mA Drive capability / PWM3 / CTS1 / SPICSN
28	P3[6]	I/O (digital)	Port P3.6 / 12mA Drive capability /PWM2 / RTS1 / SPICLK
29	P3[5]	I/O (digital)	Port P3.5 / T1 / CTS0 / QUADYB / SPIDO
30	P3[4]	I/O (digital)	Port P3.4 / T0 / RTS0 / QUADYA / SPIDI
31	P3[3]	I/O (digital)	Port P3.3 / INT1 (active low)

Pin NO.	Pin Name	Pin Type	Pin Description
32	P3[2]	I/O (digital)	Port P3.2 / INT0 (active low)
33	P3[1]	I/O (digital)	Port P3.1 / TXD0 / QUADXB
34	DVDD3V	Power	3.0V Power supply for Digital IO
35	P3[0]	I/O (digital)	Port P3.0 / RXD0 / QUADXA
36	P0[7]	I/O (digital)	Port P0.7 / I2STX_MCLK
37	P0[6]	I/O (digital)	Port P0.6 / I2STX_BCLK
38	P0[5]	I/O (digital)	Port P0.5 / I2STX_LRCLK
39	P0[4]	I/O (digital)	Port P0.4 / I2STX_DO
40	P0[3]	I/O (digital)	Port P0.3 / I2SRX_MCLK
41	P0[2]	I/O (digital)	Port P0.2 / I2SRX_BCLK
42	P0[1]	I/O (digital)	Port P0.1 / I2SRX_LRCK
43	P0[0]	I/O (digital)	Port P0.0 / I2SRX_DI
44	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core (input mode @ No REG)
45	XOSCO	Analog	Crystal Oscillator Output
46	XOSCI	Analog	Crystal Oscillator Input
47	DVDD_XOSC	Power	1.5V Power supply for Crystal oscillator.
48	AVDD_CP	Power	1.5V Power supply for Charge Pump and PFD

3.1.2 FG72 Package
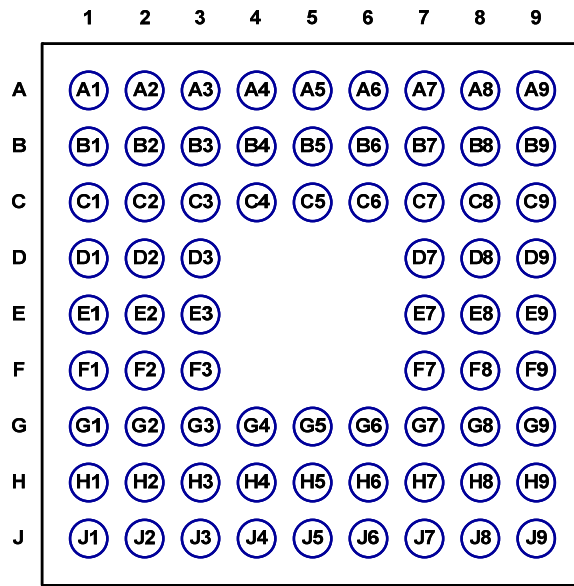
Figure 38 – Pin-out top view (1) of ZIC2410FG72 (72-pin VFBGA Package)
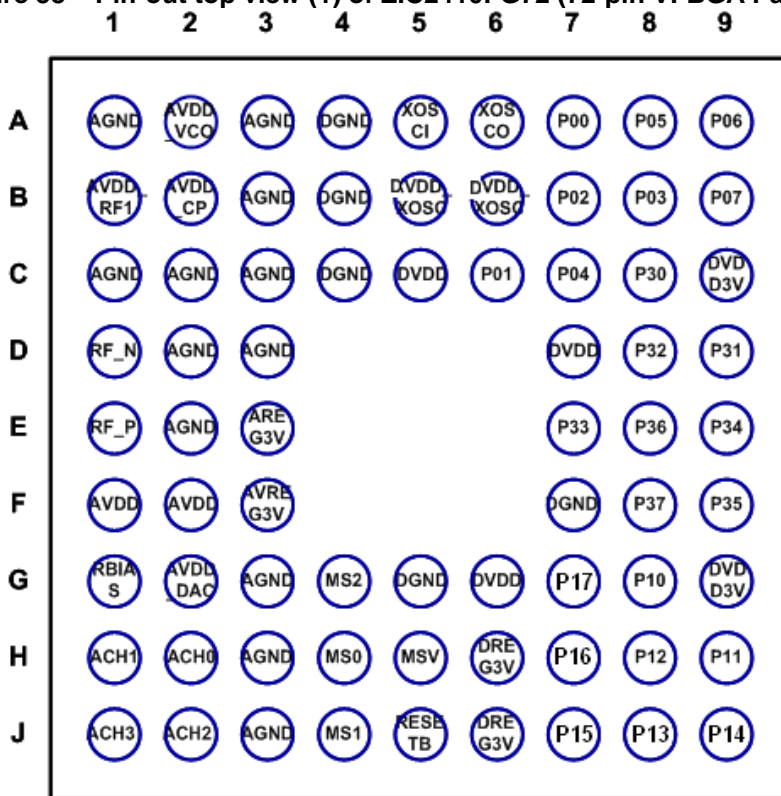
Figure 39 – Pin-out top view (2) of ZIC2410FG72 (72-pin VFBGA Package)

The ZIC2410FG72 Pin-out overview is shown in Table 57.

Table 57 – Pin-out overview; FG72 package

Ball	Ball Name	Ball Type	Ball Description
A1	AGND	Ground	Ground for RF and Analog blocks.
A2	AVDD_VCO	Power	1.5V Power supply for VCO and Divider
A3	AGND	Ground	Ground for RF and Analog blocks.
A4	DGND	Ground	Ground for digital core and IO.
A5	XOSCI	Analog	Crystal Oscillator Input.
A6	XOSCO	Analog	Crystal Oscillator Output.
A7	P0[0]	I/O(digital)	Port P0.0 / I2SRX_DI.
A8	P0[5]	I/O(digital)	Port P0.5 / I2STX_LRCLK.
A9	P0[6]	I/O(digital)	Port P0.6 / I2STX_BCLK.
B1	AVDD_RF1	Power	1.5V Power supply for LNA and PA.
B2	AVDD_CP	Power	1.5V Power supply for Charge Pump and PFD.
B3	AGND	Ground	Ground for RF and Analog blocks.
B4	DGND	Ground	Ground for digital core and IO.
B5	DVDD_XOSC	Power	1.5V Power supply for Crystal oscillator.
B6			
B7	P0[2]	I/O(digital)	Port P0.2 / I2SRX_BCLK.
B8	P0[3]	I/O(digital)	Port P0.3 / I2SRX_MCLK.
B9	P0[7]	I/O(digital)	Port P0.7 / I2STX_MCLK.
C1	AGND	Ground	Ground for RF and Analog blocks.
C2	AGND	Ground	Ground for RF and Analog blocks.
C3	AGND	Ground	Ground for RF and Analog blocks.
C4	DGND	Ground	Ground for digital core and IO.
C5	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core (input mode @ No REG).
C6	P0[1]	I/O(digital)	Port P0.1 / I2SRX_LRCK.
C7	P0[4]	I/O(digital)	Port P0.4 / I2STX_DO.
C8	P3[0]	I/O(digital)	Port P3.0 / RXD0 / QUADXA.
C9	DVDD3V	Power	3.0V Power supply for Digital IO.
D1	RF_N	RF	Negative RF input/output signal to LNA / from PA in receive / transmit mode.
D2	AGND	Ground	Ground for RF and Analog blocks.
D3	AGND	Ground	Ground for RF and Analog blocks.
D7	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core (input mode @ No REG).
D8	P3[2]	I/O(digital)	Port P3.2 / INT0 (active low).
D9	P3[1]	I/O(digital)	Port P3.1 / TXD0 / QUADXB.
E1	RF_P	RF	Positive RF input/output signal to LNA / from PA in receive / transmit mode.
E2	AGND	Ground	Ground for RF and Analog blocks.
E3	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator.
E7	P3[3]	I/O(digital)	Port P3.3 / INT1 (active low).
E8	P3[6]	I/O(digital)	Port P3.6 / 12mA Drive capability /PWM2/RTS1/SPICLK.
E9	P3[4]	I/O(digital)	Port P3.4 /T0/RTS0/QUADYA/SPIDI.
F1	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA and LPF (input mode @ No REG).
F2	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA and LPF (input mode @ No REG).
F3	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator.
F7	DGND	Ground	Ground for digital core and IO.

Ball	Ball Name	Ball Type	Ball Description
F8	P3[7]	I/O(digital)	Port P3.7 / 12mA Drive capability /PWM3 /CTS1/SPICSN (slave only).
F9	P3[5]	I/O(digital)	Port P3.5 /T1/CTS0/QUADYB/SPIDO.
G1	RBIAS	Analog	External bias resistor.
G2	AVDD_DAC	Power	1.5V Power supply for ADC and DAC.
G3	AGND	Ground	Ground for RF and Analog blocks.
G4	MS[2]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 001:ISP Mode
G5	DGND	Ground	Ground for digital core and IO.
G6	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core (input mode @ No REG).
G7	P1[7]	O (digital)	Port P1.7 GPO / P0AND/ TRSW / Fold / Clocks / BIST Fail Indicator.
G8	P1[0]	I/O(digital)	Port P1.0 / RXD1.
G9	DVDD3V	Power	3.0V Power supply for Digital IO.
H1	ACH1	Analog	Sensor ADC input / BBA Output.
H2	ACH0	Analog	Sensor ADC input / BBA Output.
H3	AGND	Ground	Ground for RF and Analog blocks.
H4	MS[0]	I (digital)	MS[2:0](Mode Select): ▪ When using Internal Regulator of ZIC2410 000: Normal mode 100: ISP mode ▪ When NOT using Internal Regulator of ZIC2410 010:Normal mode 110: ISP mode
H5	MSV	I (digital)	Mode Select of Voltage. 0:1.5V
H6	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator.
H7	P1[6]	I/O(digital)	Port P1.6 / TRSWB.
H8	P1[2]	I/O(digital)	Port P1.2.
H9	P1[1]	I/O(digital)	Port P1.1 / TXD1.
J1	ACH3	Analog	Sensor ADC input / BBA Output.
J2	ACH2	Analog	Sensor ADC input / BBA Output.
J3	AGND	Ground	Ground for RF and Analog blocks.
J4	MS[1]	I (digital)	MS[2:0](Mode Select): 000: Normal Mode 001: ISP Mode
J5	RESETB	I (digital)	Reset (Active Low).
J6	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator.
J7	P1[5]	I/O(digital)	Port P1.5.
J8	P1[3]	I/O(digital)	Port P1.3 / QUADZA / Sleep Timer OSC Buffer Output / RTCLKOUT.
J9	P1[4]	I/O(digital)	Port P1.4 / QUADZB / Sleep Timer OSC Buffer Input.

3.2   PACKAGE INFORMATION

3.2.1   PACKAGE INFORMATION: ZIC2410QN48 (QN48pkg)
Package is 48-pin QFN type package with down-bonding.

Figure 40 – QN48 Package Drawing

Table 58 – QN48 Package Dimensions

DIM	MIN	NOM	MAX	NOTES
A	0.80	0.85	0.90	1. Dimensions and Tolerances conform to ASME Y14.5N-1994
A1	0.00		0.05	
A3		0.203 REF		2. All Dimensions are in millimeters; all angles are in degrees
b	0.18	0.25	0.30	
D		7.00 BSC		3. Dimension "b" applies to metalized terminals and is measured between 0.25 and 0.30mm from the terminal tip. Dimension L1 represents how far back the terminal may be from the package edge. Up to 0.1mm is acceptable
E		7.00 BSC		
D2	5.04	5.14	5.24	
E2	5.04	5.14	5.24	
e		0.50 BSC		
L	0.48	0.53	0.58	
L1	0.00		0.10	4. Coplanarity applies to the exposed heat slug as well as to the terminals
L2	0.35	0.40	0.45	
P		45º BSC		5. Radius of the terminals is optional
aaa		0.10		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		

3.2.1.1 CARRIER TAPE AND REEL SPECIFICATION (QN48pkg)

A	330 ±2.0
B	1.5 min
C	13.0 +0.5 −0.2
D	20.2 min
N	100±2.0
W1	16.4 +3.0 −0.0
W2	20.4±2.0
W3	17.65 +1.75 −0.75
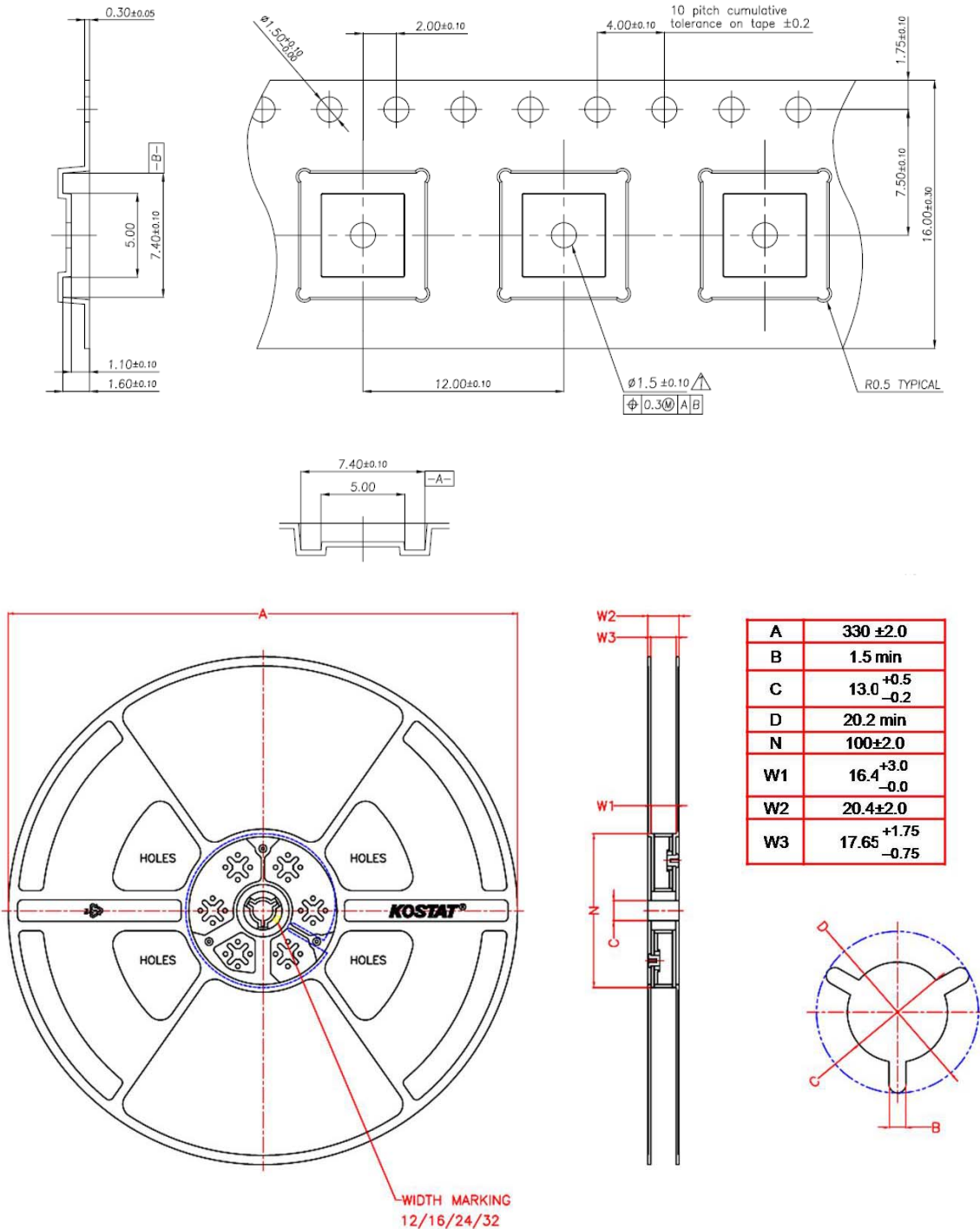
Figure 41 – QN48 Carrier Tape & Reel Specification

3.2.2   PACKAGE INFORMATION: ZIC2410FG72 (FG72pkg)

Package type is 72-pin VFBGA package with ball-bonding.
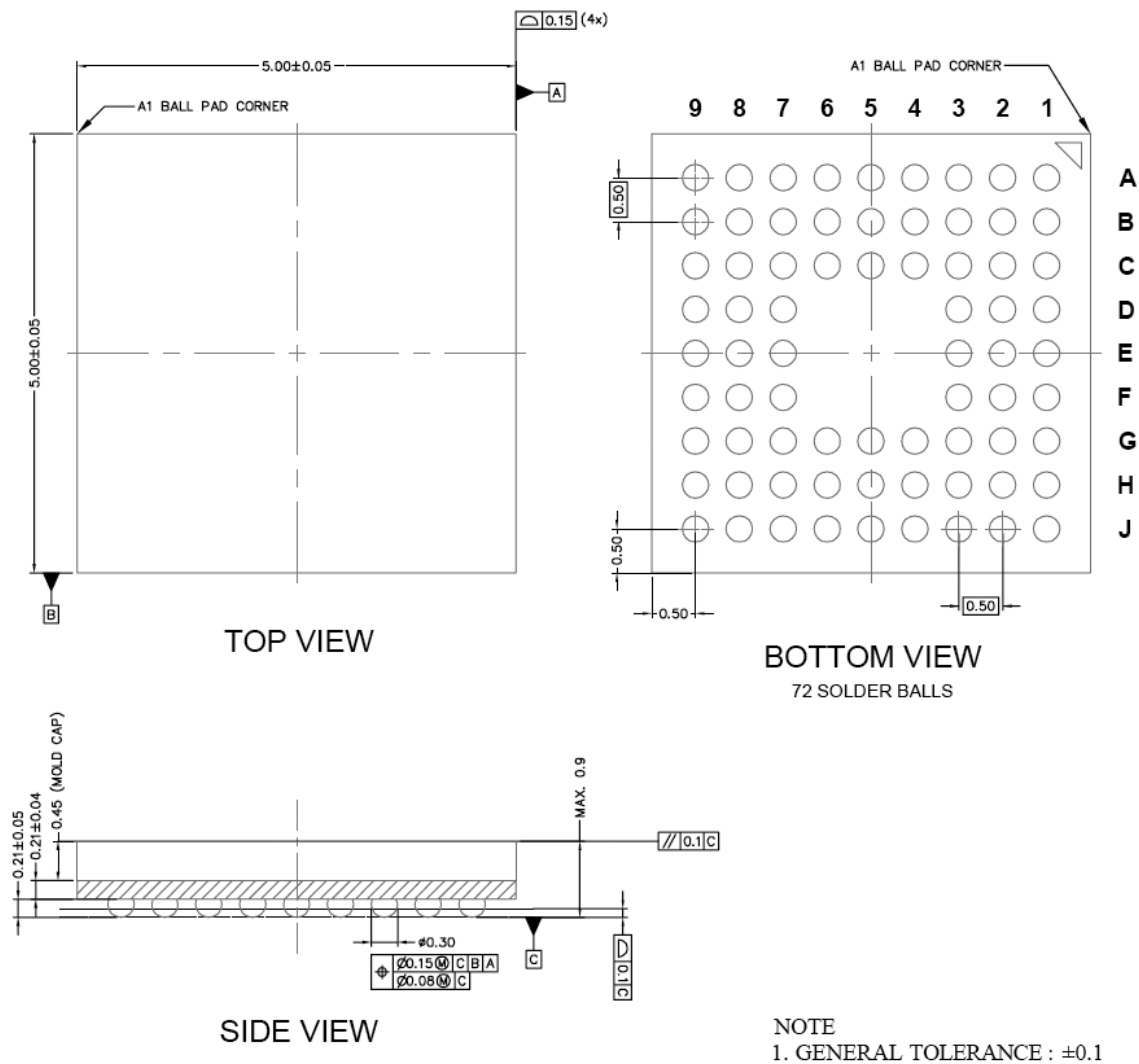
Figure 42 – FG72 Package Drawing

3.2.2.1 CARRIER TAPE AND REEL SPECIFICATION (FG72pkg)
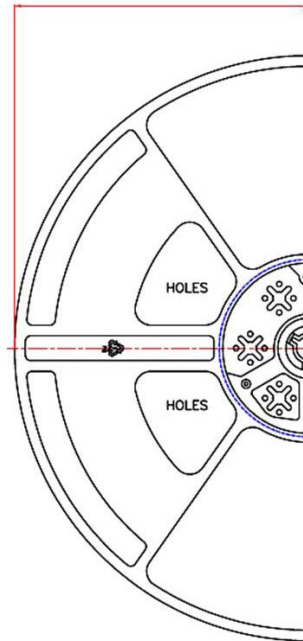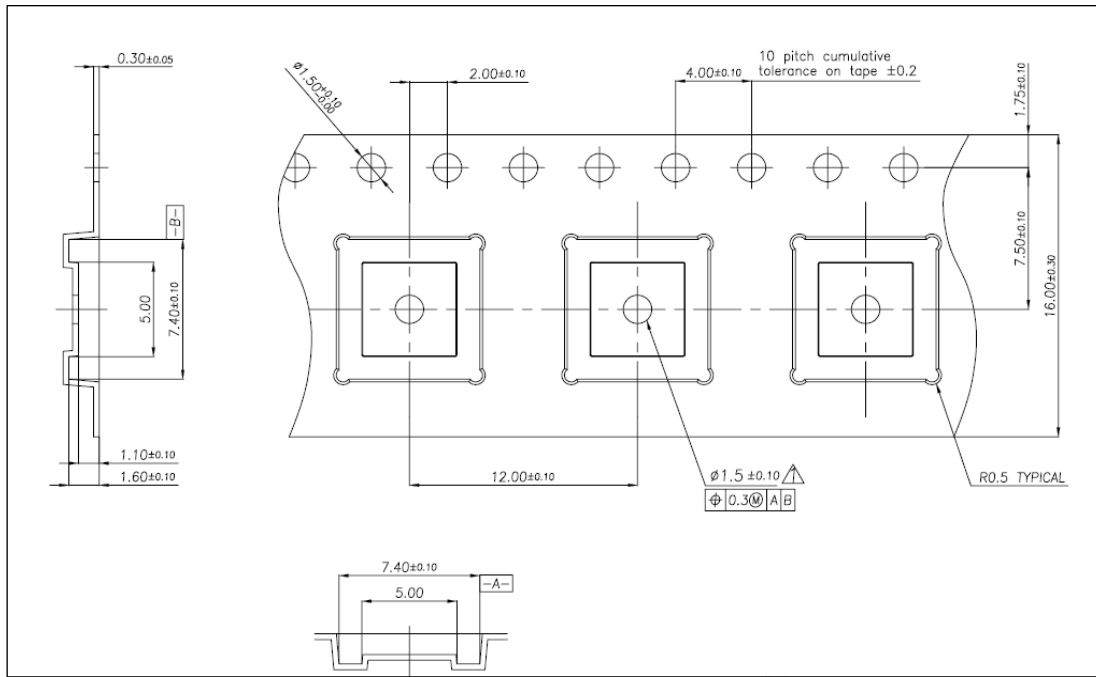
Figure 43 – FG72 Carrier Tape & Reel Specification

3.3 APPLICATION CIRCUITS

3.3.1 APPLICATION CIRCUITS (QN48 package)

The ZIC2410 operates from a single supply voltage. The core must run at 1.5V, so, if 1.5V is available, both the core and the I/O can run from 1.5V. If a higher voltage I/O is required (or higher voltage is available on the board) the ZIC2410 contains an on-chip voltage regulator that can step down a 1.9V~3.3V supply to 1.5V for the core. In this case the I/O can be run from a 1.9V to 3.3V supply.

A typical application circuit for the ZIC2410QN48 using 1.9V~3.3V as the I/O power through the internal regulator is shown in Figure 44.
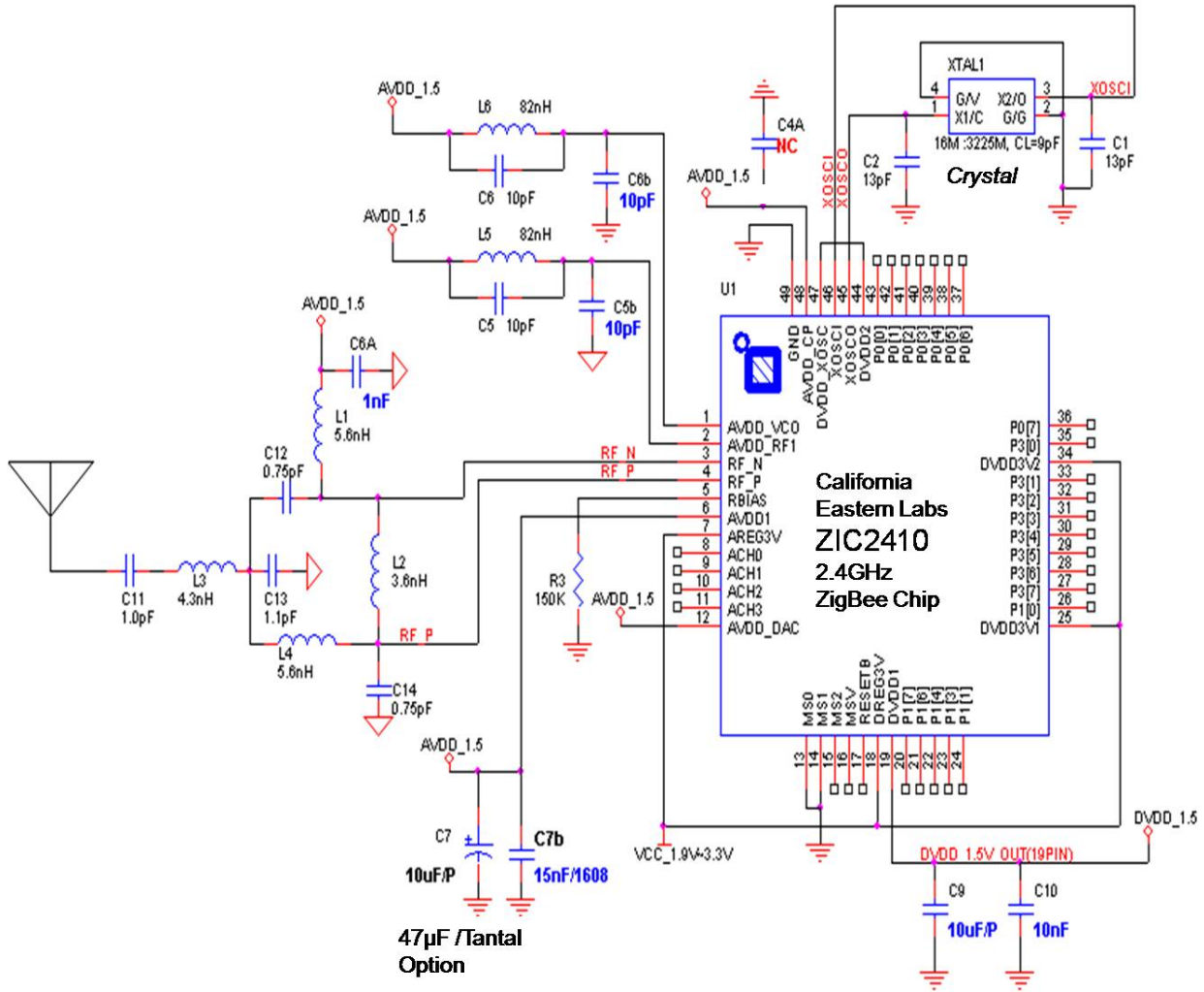
*** GND is bottom pad (down-bonding pad) in the above schematic

Figure 44 – ZIC2410QN48 Typical Application Circuit (I/O Power: 1.9V~3.3V , MS[1]=0)

Figure 45 shows the application circuit of the ZIC2410QN48 when using 1.5V as the I/O power and not using the internal regulator. In this case, a software setting is needed to turn off the internal regulator of the device.

*** *GND is bottom pad (down-bonding pad) in the above schematic*
Figure 45 – the ZIC2410QN48 Application Circuit (I/O Power: 1.5V , MS[1]=1)

NOTE: When the ZIC2410 is operated below minimum operating voltage, a reset error will occur because of the unstable voltage. For more detailed information, refer to the Note of **'Section 1.3 RESET'**.

3.3.2 APPLICATION CIRCUITS (FG72 package)

The ZIC2410 operates from a single supply voltage. The core must run at 1.5V, so, if 1.5V is available, both the core and the I/O can run from 1.5V. If a higher voltage I/O is required (or higher voltage is available on the board) the ZIC2410 contains an on-chip voltage regulator that can step down a 1.9V~3.3V supply to 1.5V for the core. In this case the I/O can be run from a 1.9V to 3.3V supply.

A typical application circuit for the ZIC2410FG72 using 1.9V~3.3V as the I/O power through the internal regulator is shown in Figure 46.
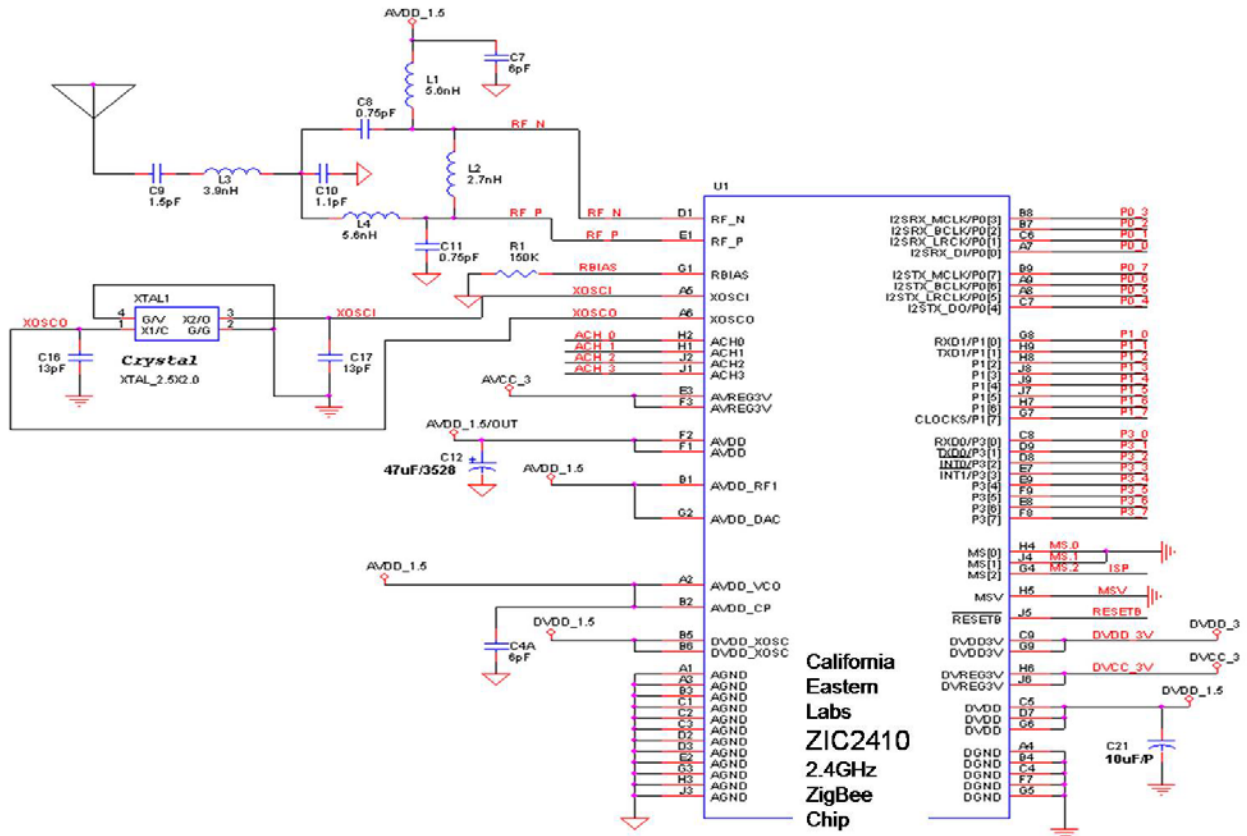
Figure 46 – ZIC2410FG72 Application Circuit (I/O Voltage: 1.9V~3.3V , MS[1]=0)

Figure 47 shows the application circuit of the ZIC2410FG72 when using 1.5V as the I/O power and not using the internal regulator. In this case, a software setting is needed to turn off the internal regulator of the device.
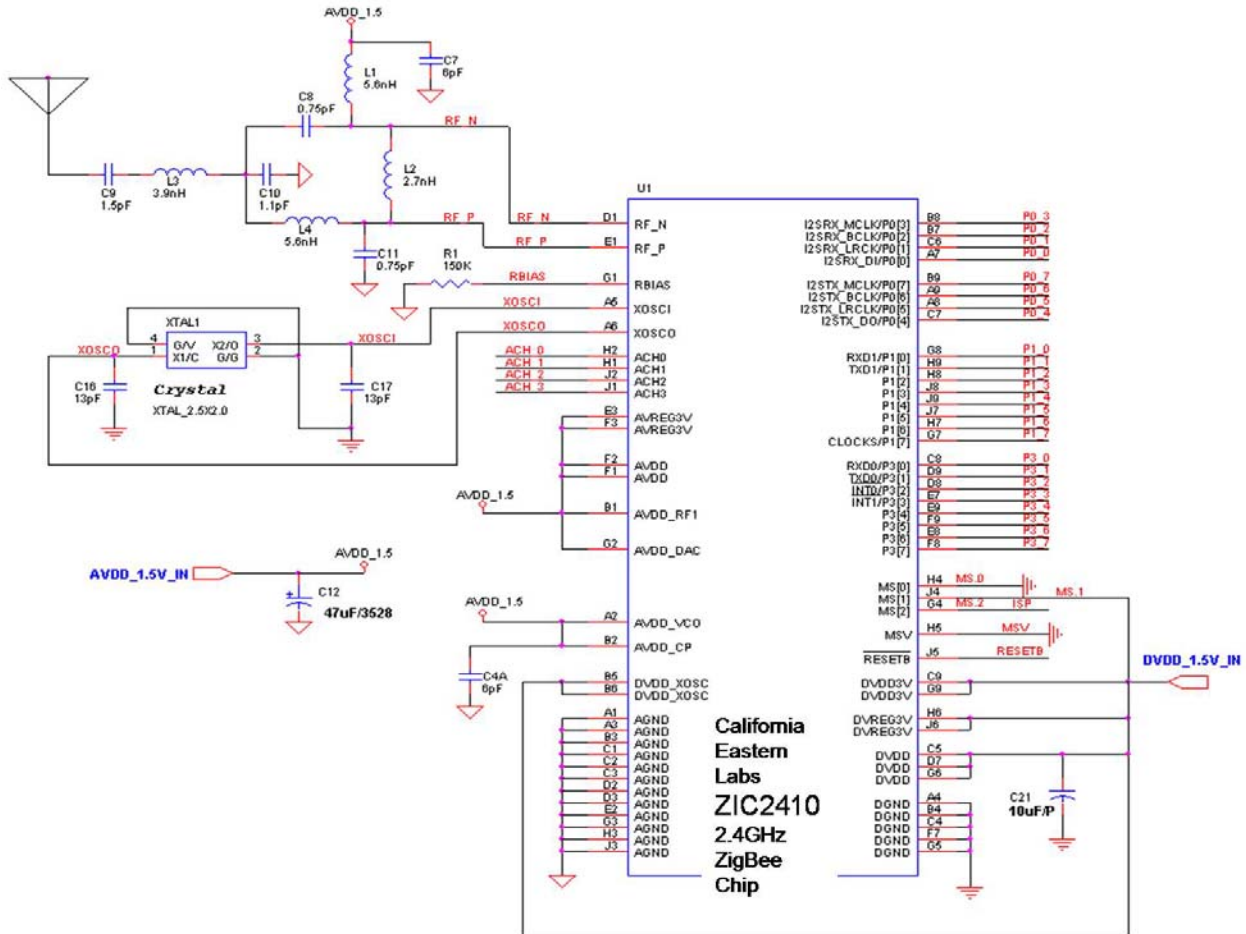
Figure 47 – ZIC2410FG72 Application Circuit (I/O Voltage: 1.5V , MS[1]=1)

NOTE: When the ZIC2410 is operated below minimum operating voltage, a reset error will occur because of the unstable voltage. For more detailed information, refer to the Note of **'Section 1.3 RESET'**.

4 REFERENCES

4.1 TABLE OF TABLES

4.2 TABLE OF FIGURES

4.3 TABLE OF EQUATIONS

5 REVISION HISTORY

Revision	Date	Description
A	20Jun08	Released