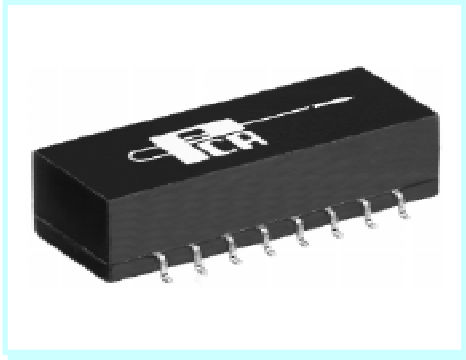


# High Speed LAN Interface Module

## EPF8010GM



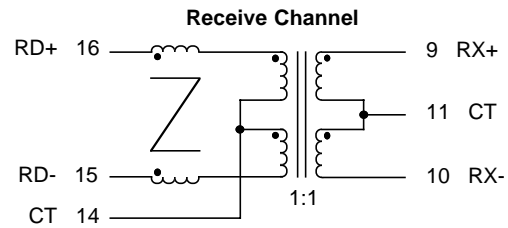
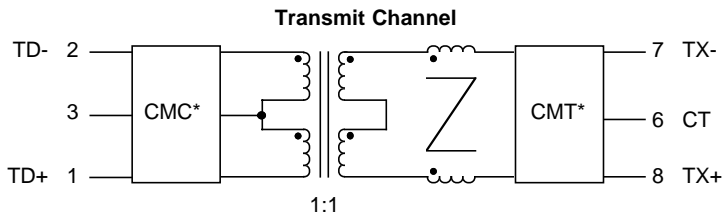
- Recommended for 10/100, 100 BX, 155 Mb/s applications • (requiring 1:1 magnetics)
- Guaranteed to operate with 8 mA DC bias at 70°C •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

### Electrical Parameters @ 25° C

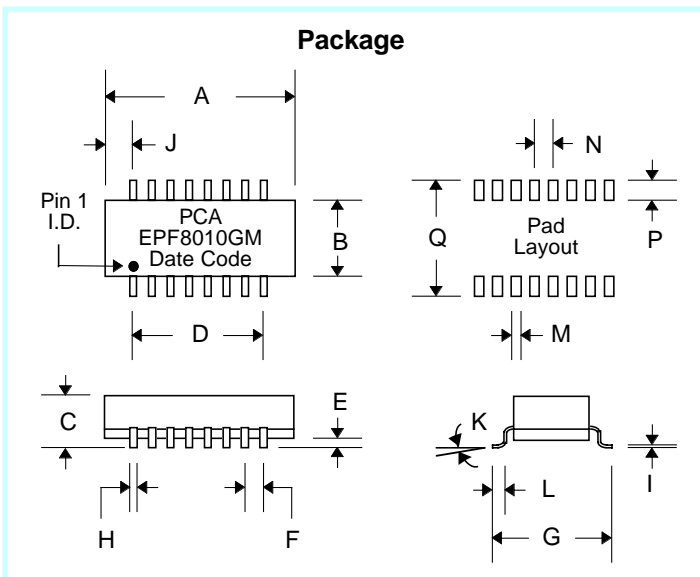
OCL @ 70°C	Insertion Loss (dB Max.)						Return Loss (dB Min.)						Common Mode Rejection (dB Min.)						Crosstalk (dB Min.) [Between Channels]	
	1-80 MHz		80-100 MHz		100-150 MHz		1-30 MHz		30-60 MHz		60-100 MHz		1-30 MHz		30-100 MHz		100-500 MHz		5-10 MHz	10-100 MHz
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv		
100 KHz, 0.1 Vrms 8 mA DC Bias																				
350μH	-1	-1	-2	-2	-3	-3	-18	-18	-12	-12	-10	-10	-38	-38	-38	-38	-10	-10	-40	-40

- Isolation : 1500 Vrms • Impedance : 100 Ω • Rise Time : 3.0 nS Max. •

### Schematic



### Package



### Dimensions

Dim.	(Inches)			(Millimeters)		
	Min.	Max.	Nom.	Min.	Max.	Nom.
A	.970	.990		24.64	25.15	
B	.380	.400		9.65	10.16	
C	.225	.245		5.72	6.22	
D	.700	Typ.		17.78	Typ.	
E	.005	.015		.127	.381	
F	.100	Typ.		2.54	Typ.	
G	.500	.520		12.7	13.20	
H	.018	.022		.457	.559	
I	.008	.012		.203	.305	
J	.090	Typ.		2.28	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.030			.762
N			.100			2.54
P			.092			2.34
Q			.560			14.22

\*CMC or CMT optional.

## EPF8010GM

The circuit below is a guideline for interconnecting PCA's EPF8010GM with a typical 100 BX PHY chip for 100 Mb/s applications over UTP cable. Further details of system design, such as chip pin-out, etc. should be obtained from the specific chip manufacturer.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 100/155 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the specific chip preset template control resistors to get at least 2.12V pk-pk across the transmit side input pins.

It is recommended that system designers do not ground the receiver side center tap, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75  $\Omega$  shown from the center taps of the secondary may be taken to chassis ground via a suitable cap. This depends upon the user's design, EMI margin, etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8010GM. There need not be any ground plane beyond this point.

For best results, the PCB designer should design the outgoing traces preferably to be 50  $\Omega$ , balanced and well coupled to achieve minimum radiation from these traces.

### Typical Application Circuit for 100 BX over UTP

