Agilent HSDL-3603
IrDA® Data Compliant
4 Mbit/s Infrared Transceiver
Data Sheet

Description

The HSDL-3603 is a low profile infrared transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data-link. The module is fully compliant to IrDA Date Physical Layer Specifications v1.4 Fct Infrared (FIR) and IEC825-Class I Eye Safe.

The HSDL-3603 can be shut down completely to achieve very low power consumption. In the shutdown mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. Such features are ideal for mobile devices that require low power consumption.

Applications

- **Digital imaging**
  - **Digital still cameras**
  - **Photo-imaging printers**
- **Data communication**
  - **Notebook computers**
  - **Desktop PCs**
  - **WinCE handheld products**
  - **Personal Digital Assistants**
  - **Printers**
  - **Auto PCs**
  - **Dongles**
  - **Set-top box**
- **Digital imaging**
  - **Digital cameras**
  - **Photo-imaging printers**
- **Telecommunication products**
  - **Mobile phones**
  - **Pagers**
- **Electronic wallet**
- **Small industrial and medical instrumentation**
  - **General data collection devices**
  - **Patient and pharmaceutical data collection devices**
- **IR LANs**

Features

- **Fully compliant to IrDA 1.4 Fast Infrared (FIR) from 9.6 kbit/s to 4 Mbit/s**
- **Typical link distance > 1.5 m**
- **Miniature package**
  - **Height: 3.90 mm**
  - **Width: 9.80 mm**
  - **Depth: 4.65 mm**
- **Guaranteed temperature performance, -25 to 70°C**
  - **Critical parameters are guaranteed over temperature and supply voltage**
- **Low power consumption**
  - **Low shutdown current (10 nA typical)**
  - **Complete shutdown of TXD, RXD, and PIN diode**
- **Withstands >100 mV_{p-p} power supply ripple typically**
- **V_{CC} supply 2.7 to 5.25 volts**
- **Integrated EMI shield**
- **LED stuck-high protection**
- **Designed to accommodate light loss with cosmetic windows**
- **IEC 825-Class 1 eye safe**
- **Interface to various super I/O and controller devices**

Functional Block Diagram

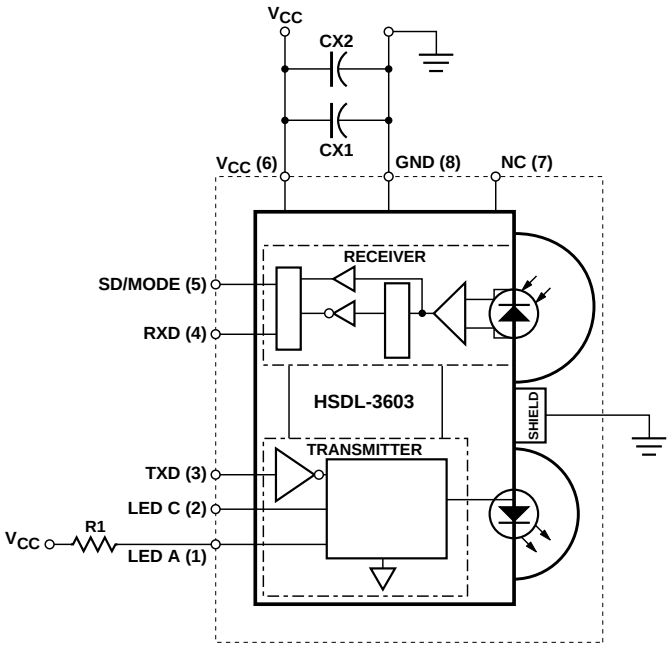


Figure 1. HSDL-3603 functional block diagram.

Pinout

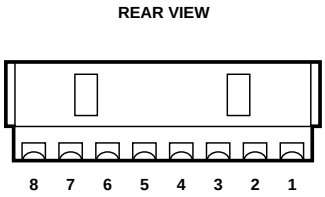


Figure 2. Rear view diagram with pin-out.

Ordering Information

Part Number	Packaging Type	Package	Quantity
HSDL-3603-007	Tape and Reel	Front View	1800

Marking Information

The unit is marked with 3603yyww on the shield.

3603 = Product name
yy = year
ww = work week

Application Support Information

The Application Engineering Group is available to assist you with the application designs associated with the HSDL-3603 infrared transceiver module. You can contact them through your local sales representatives for additional details.

I/O Pins Configuration Table

Pin	Symbol	Description	I/O Type	Function
1	LED A	LED Anode	Input	This pin can be connected directly to V_{CC} (i.e., without series resistor) at less than 3 V. Please refer to Table 1 for V_{CC} versus Series Resistor, R1.
2	LED C	LED Cathode	Output	Leave this pin unconnected.
3	TXD	Transmit Data	Input, Active High	This pin is used to transmit serial data when SD/Mode pin is low. If this pin is held high longer than ~100 μs, the LED would be turned off when used in conjunction with the SD/Mode pin. TXD is low at initialization.
4	RXD	Receive Data	Output, Active Low	This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. It is in tri-state mode when the transceiver is in shutdown mode and during digital serial programming operations. RXD is high at initialization.
5	SD/Mode	Shutdown/ Mode Select	Input, Active High	The transceiver is in shutdown mode if this pin is high for more than 400 μs. On the falling edge of this signal, the state of the TXD pin sampled and used to set receiver low bandwidth (TXD=low) or high bandwidth (TXD=high) mode. See Figure 2 for bandwidth selection timings. SD is low at initialization.
6	V_{CC}	Supply Voltage	Supply Voltage	Regulated, 2.7 to 5.25 Volts.
7	NC	No Connect	No Connect	
8	GND	Ground	Ground	Connect to system ground.
–	Shield	EMI Shield	EMI Shield	Connect to system ground via a low inductance trace. For best performance, do not connect directly to the transceiver pin GND.

Recommended Application Circuit Components

Component	Recommended Value	Notes
R1	0 Ω ± 5%, 0.5 Watt, for 2.7 V 1.8 Ω ± 5%, 0.5 Watt, for 3.0 V 4.7 Ω ± 5%, 0.5 Watt, for 3.3 V 6.8 Ω ± 5%, 0.5 Watt, for 3.5 V	
CX1	0.47 μF ± 20%, X7R Ceramic	1
CX2	6.8 μF ± 20%, Tantalum	2

Notes:

1. CX1 must be placed within 0.7 cm of the HSDL-3603 to obtain optimum noise immunity.
2. In environments with noisy power supplies, supply rejection performance can be enhanced by including CX2, as shown in Figure 1: "HSDL-3603 Functional Block Diagram" on Page 2.

Bandwidth Selection Timing

The transceiver is in default SIR/MIR mode when powered on. User needs to apply the following programming sequence to both the SD and TXD inputs to enable the transceiver to operate at FIR mode.

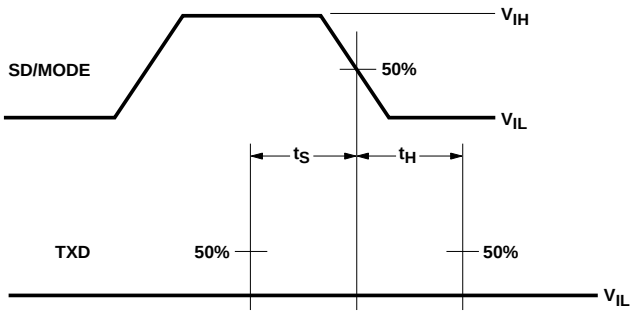


Figure 3. Bandwidth selection timing at SIR/MIR mode.

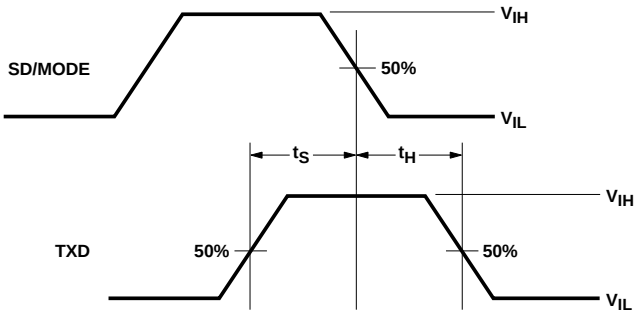


Figure 4. Bandwidth selection timing at FIR mode.

Setting the transceiver to SIR/MIR Mode (9.6 kb/s to 1.152 Mbit/s)

1. Set SD/Mode input to logic HIGH
2. TXD input should remain at logic LOW
3. After waiting for $t_S \geq 25$ ns, set SD/Mode to logic LOW, the HIGH to LOW negative edge transition will determine the receiver bandwidth
4. Ensure that TXD input remains low for $t_H \geq 100$ ns, the receiver is now in SIR/MIR mode
5. SD input pulse width for mode selection should be > 50 ns.

Setting the transceiver to FIR (4.0 Mbit/s) Mode

1. Set SD/Mode input to logic HIGH
2. After SD/Mode input remains HIGH at > 25ns, set TXD input to logic HIGH, wait $t_S \geq 25$ ns (from 50% of TXD rising edge till 50% of SD falling edge)
3. Then set SD/Mode to logic LOW, the HIGH to LOW negative edge transition will determine the receiver bandwidth
4. After waiting for $t_H \geq 100$ns, set the TXD input to logic LOW
5. SD input pulse width mode selection should be > 50ns.

Transceiver I/O Truth Table

Inputs			Outputs		
TXD	**Light Input to Receiver**	**SD**	**LED**	**RXD**	**Notes**
High	Don't Care	Low	On	Not Valid	
Low	High	Low	Off	Low	1, 2
Low	Low	Low	Off	High	
Don't Care	Don't Care	High	Off	High	

Notes:
1. In-band IrDA signals and data rates ≤ 4Mbit/s.
2. RXD logic low is a pulsed response. The condition is maintained for a duration dependent on pattern and strength of the incident intensity.

Caution: *The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.*

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	–40	100	°C	
Operating Temperature	T_A	–25	70	°C	
LED Anode Voltage	V_{LEDA}	0	6.5	V	
Supply Voltage	V_{CC}	0	6.5	V	
Input Voltage: TXD, SD/Mode	V_I	0	6.5	V	
Output Voltage: RXD	V_O	0	6.5	V	
DC LED Transmit Current	I_{LED} (DC)		150	mA	
Average Transmit Current	I_{LED} (PK)		650	mA	3

Note:

3. ≤ 25% duty cycle, ≤ 90 μs pulse width.

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature		T_A	–25		70	°C	
Supply Voltage		V_{CC}	2.7		5.25	V	
Logic Input Voltage	Logic High	V_{IH}	2/3 V_{CC}		V_{CC}	V	
for TXD, SD/Mode	Logic Low	V_{IL}	0		1/3 V_{CC}	V	
Receiver Input Irradiance	Logic High	EI_H	0.0036		500	mW/cm^2	For in-band signals ≤ 115.2 kbit/s[4]
			0.0090		500	mW/cm^2	0.576 Mbit/s ≤ in-band signals ≤ 4 Mbit/s[4]
	Logic Low	EI_L			0.3	μW/cm^2	For in-band signals ≤ 115.2 kbit/s[4]
LED (Logic High) Current Pulse Amplitude		I_{LEDA}	400		600	mA	
Receiver Data Rate			0.0096		4.0	Mbit/s	

Note:

4. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

Electrical and Optical Specifications

Specifications (Min. and Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C with V_{CC} set to 3.0 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver							
Viewing Angle		2θ	30			°	
Peak Sensitivity Wavelength		λp		880		nm	
RXD Output Voltage	Logic High	V_{OH}	$V_{CC} - 0.2$		V_{CC}	V	I_{OH} = –200 μA, EI ≤ 0.3 μW/cm²
	Logic Low	V_{OL}	0		0.4	V	I_{OL} = 200 μA, EI ≥ 3.6 μW/cm²
RXD Pulse Width (SIR)		t_{PW} (SIR)	1		4.0	μs	$\theta \le 15°$, C_L = 12 pF[5]
RXD Pulse Width (MIR)		t_{PW}(MIR)	100		500	ns	$\theta \le 15°$, C_L = 12 pF [6]
RXD Pulse Width (FIR)		t_{PW}(FIR)	80		165	ns	$\theta \le 15°$, C_L = 12 pF[7]
RXD Rise and Fall Times		t_r, t_f		25		ns	C_L =12 pF
Receiver Latency Time		t_L		10	150	μs	
Receiver Wake Up Time		t_{rw}		10	150	μs	
Transmitter							
Radiant Intensity		IE_H	100	180		mW/Sr	I_{LEDA} = 400 mA, $\theta \le 15°$, $V_{TXD} \ge V_{IH}$ T = 25 °C
Viewing Angle		2θ	30		60	°	
Peak Wavelength		λ_P		875		nm	
Spectral Line Half Width		$\Delta\lambda$		35		nm	
TXD Logic Levels	High	V_{IH}	2/3 V_{CC}		V_{CC}	V	
	Low	V_{IL}	0		1/3 V_{CC}	V	
TXD Input Current	High	I_H		0.02	10	μA	$V_I \ge V_{IH}$
	Low	I_L	–10	–0.02	10	μA	$0 \le V_I \le V_{IL}$
LED Current	On	I_{VLED}		400	600	mA	V_I(TXD) ≥ V_{IH}
	Shutdown	I_{VLED}		20	1000	nA	V_I(SD) ≥ V_{IH}, T_A = 25°C
TXD Pulse Width (SIR)		t_{PW} (SIR)	1.5	1.6	1.8	μs	t_{PW} (TXD) = 1.6 μs at 115.2 kbit/s
TXD Pulse Width (MIR)		t_{PW}(MIR)	148	217	260	ns	t_{PW} (TXD) = 217 ns at 1.152 Mbit/s
TXD Pulse Width (FIR)		t_{PW}(FIR)	115	125	135	ns	t_{PW} (TXD) = 125 ns at 4.0 Mbit/s
Maximum Optical PW		$t_{PW(max.)}$		60	100	μs	
TXD Rise and Fall Time (Optical)		t_r, t_f			40	ns	t_{PW} (TXD) = 125 ns at 4.0 Mbit/s
Transceiver							
Supply Current	Shutdown	I_{CC1}		10	1000	nA	$V_{SD} \ge 2/3\ V_{CC}$, T_A = 25°C
	Idle	I_{CC2}		1.8	3.0	mA	V_I(TXD) ≤ V_{IL}, EI = 0
	Active	I_{CC3}		2.5		mA	EI = 10 mW/cm²

Notes:

5. For in-band signals ≤ 115.2 kbit/s where 3.6 μW/cm² ≤ EI ≤ 500 mW/cm².
6. For in-band signals at 1.152 Mbit/s where 9.0 μW/cm² ≤ EI ≤ 500 mW/cm².
7. For in-band signals of 125 ns pulse width, 4 Mbit/s, 4 PPM at recommended 400 mA drive current.

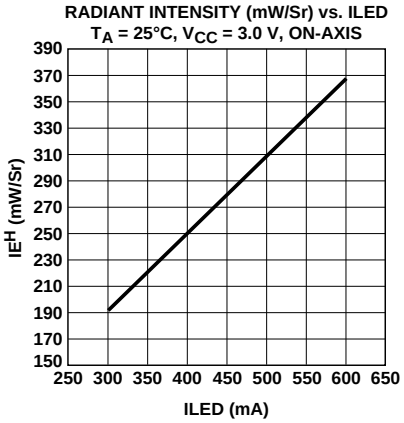


Figure 5. IR LOP vs. ILED.

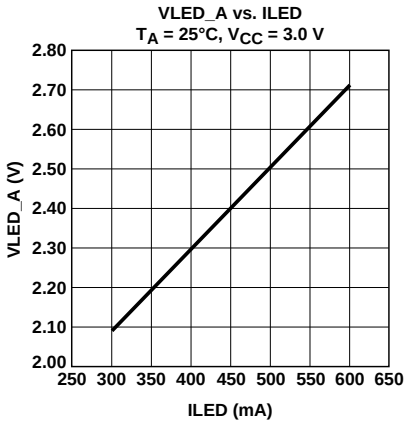


Figure 6. IR VLED vs. ILED.

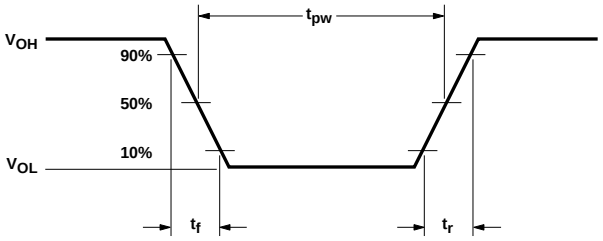


Figure 7. RXD output waveform.

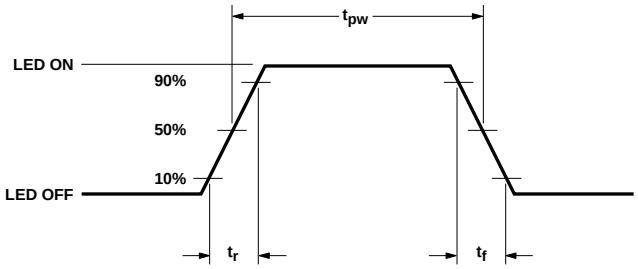


Figure 8. LED optical waveform.

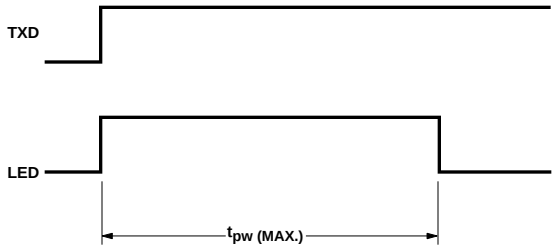


Figure 9. TXD 'stuck on' waveform.

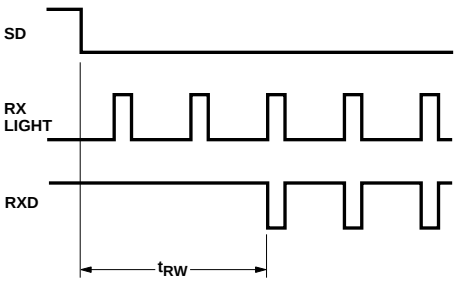


Figure 10. Receiver wakeup time waveform.

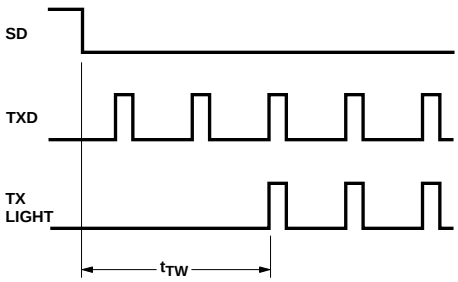


Figure 11. TXD wakeup time waveform.

HSDL-3603 Package Outline Dimensions

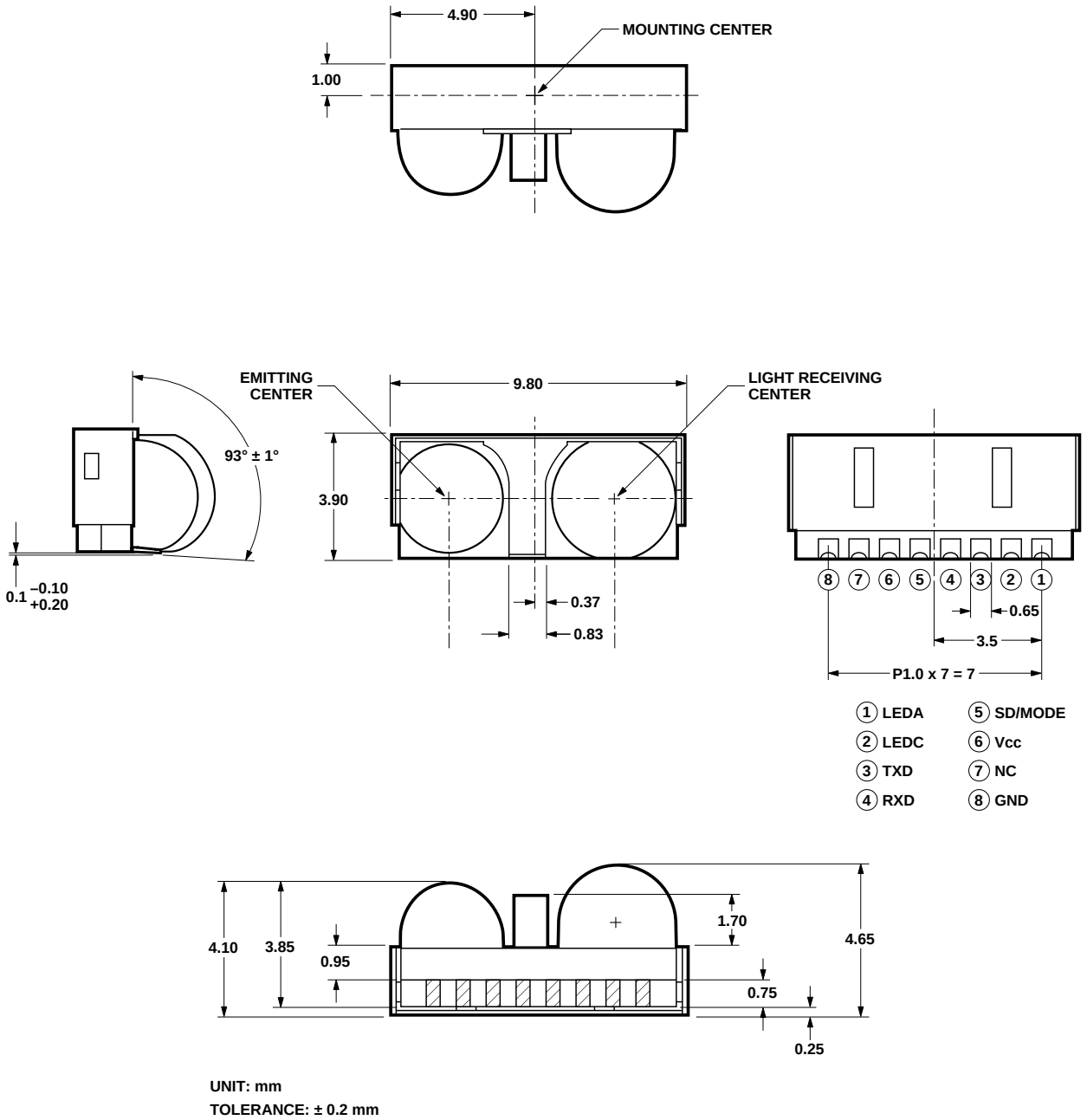


Figure 12. Package outline dimensions.

HSDL-3603 Tape and Reel Dimensions

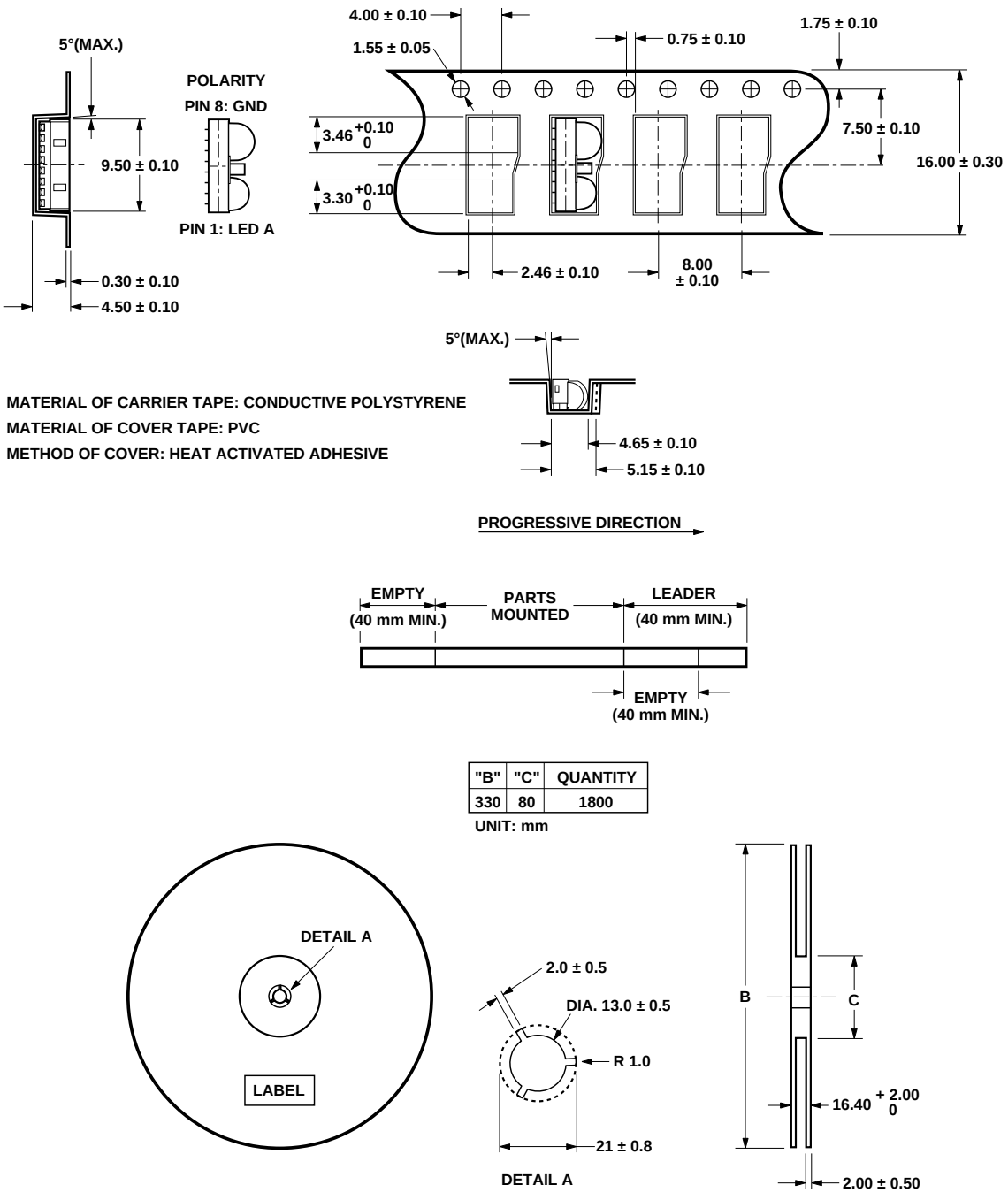


Figure 13. Tape and reel dimensions.

Moisture Proof Packaging

All HSDL-3603 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC level 4.

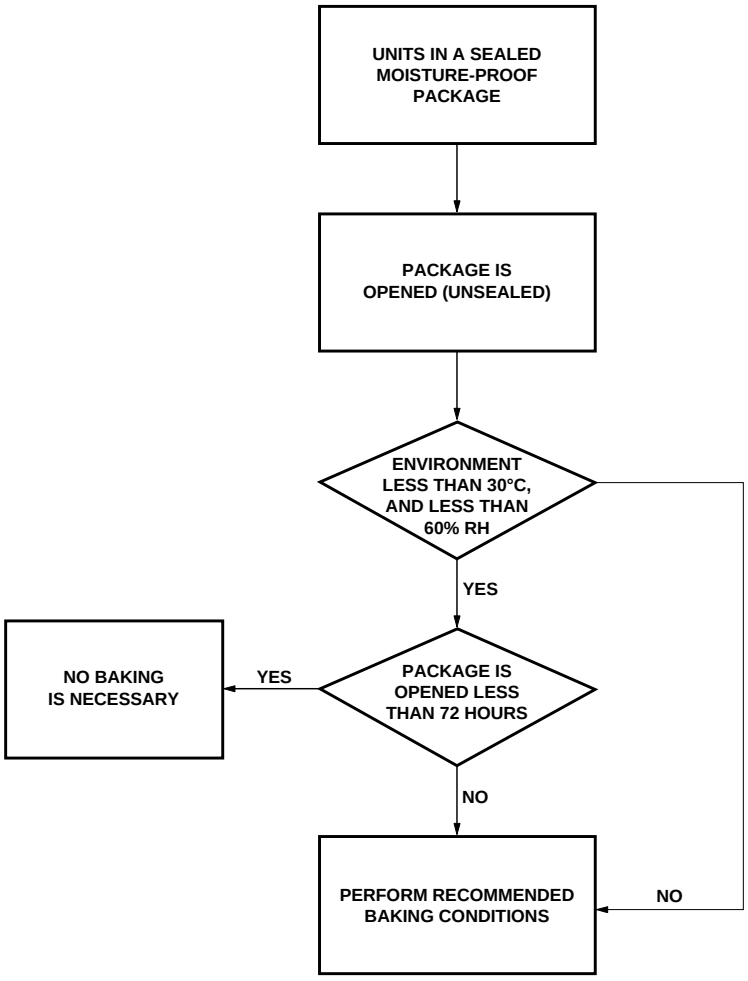


Figure 14. Baking conditions.

Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temperature	Time
In Reels	60˚C	≥ 48 hours
In Bulk	100˚C	≥ 4 hours
	125˚C	≥ 2 hours
	150˚C	≥ 1 hour

Baking should only be done once.

Recommended Storage Conditions	
Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within three days if stored at the recommended storage conditions. If times longer than two days are needed, the parts must be stored in a dry box.

Reflow Profile

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the following table. The temperatures are measured at the component to printed circuit board connections.

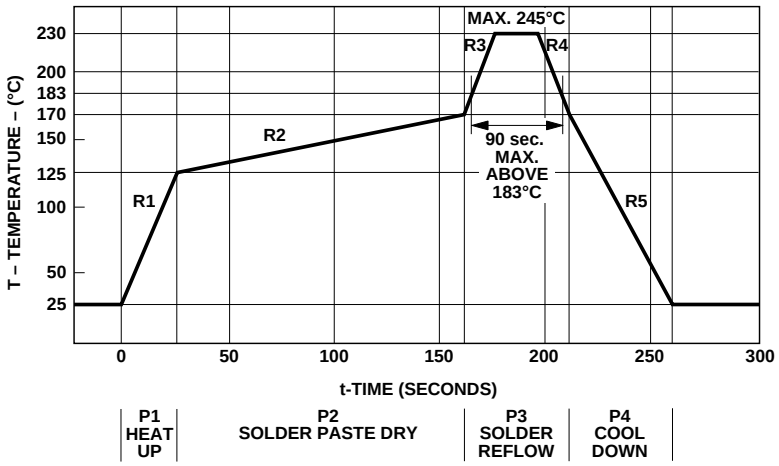


Figure 15. Reflow graph.

Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3	170°C to 230°C (245°C max.)	4°C/s
	P3, R4	230°C to 170°C	–4°C/s
Cool Down	P4, R5	170°C to 25°C	–3°C/s

In **process zone P1**, the PC board and HSDL-3603 castellation I/O pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3603 castellation I/O pins.

Process zone P2 should be of sufficient time duration (> 60 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed -3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3603 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3603 transceiver.

Appendix A: HSDL-3603 SMT Assembly Application Note

1.0. Solder Pad, Mask, and Metal Solder Stencil Aperture

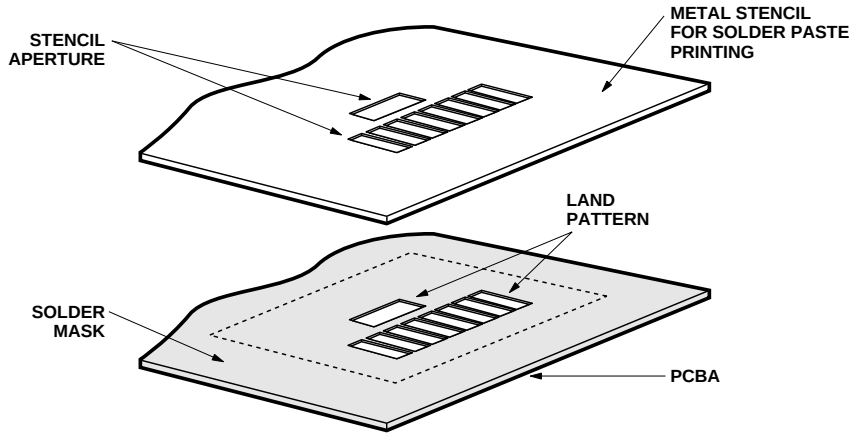


Figure 16. Stencil and PCBA.

1.1. Recommended Land Pattern for HSDL-3603

Dimension	mm	inches
a	2.00	0.079
b	0.70	0.028
c (pitch)	1.00	0.039
d	2.50	0.098
e	1.51	0.059
f	3.09	0.122
g	2.84	0.112

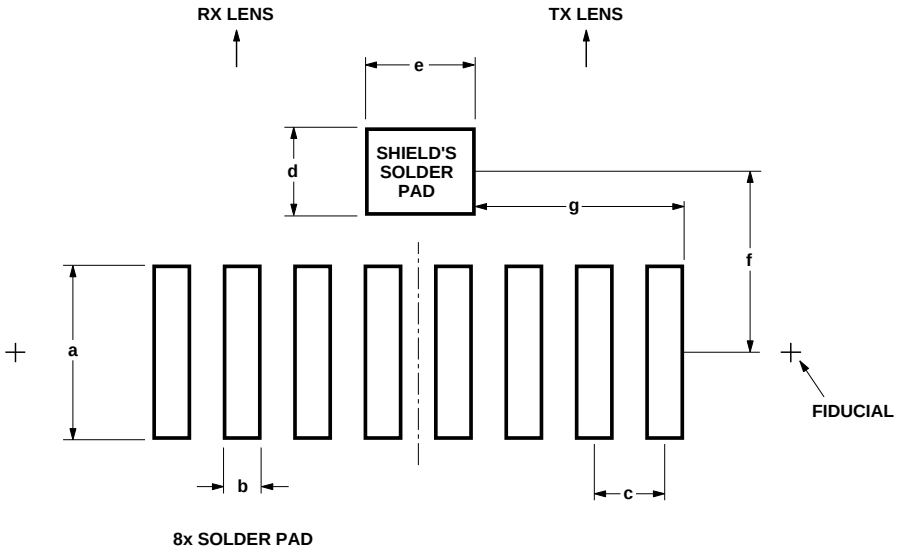


Figure 17. Top view of land pattern.

1.2. Adjacent Land Keep-out and Solder Mask Areas

Dimension	mm	inches
h	min. 0.2	min. 0.008
j	10.8	0.425
k	5.1	0.201
l	3.2	0.126

- **Adjacent land keep-out** is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.
- "**h**" is the minimum solder resist strip width required to avoid solder bridging adjacent pads.
- It is recommended that 2 fiducial cross be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid photo-imagineable solder resist/mask is recommended.

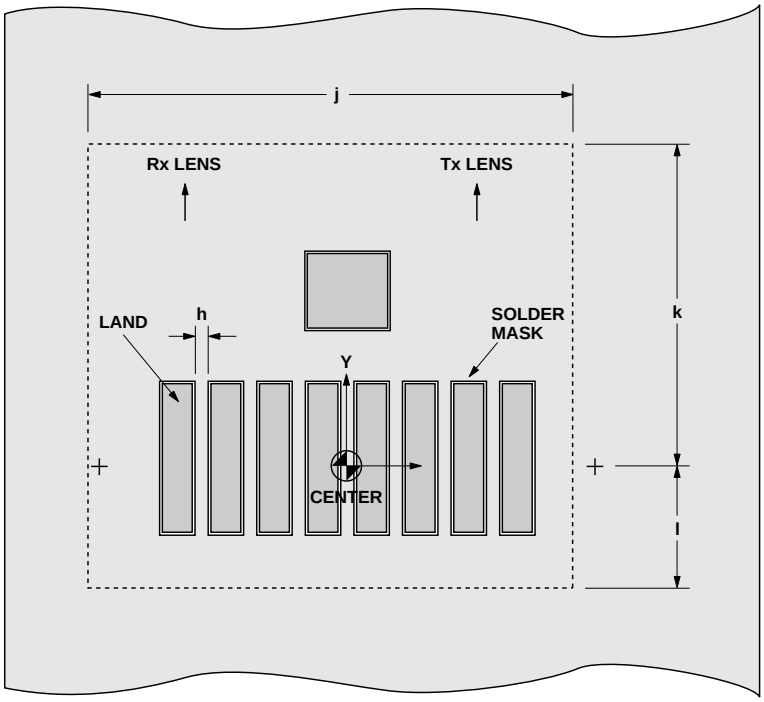


Figure 18. PCBA – Adjacent land keep-out and solder mask.

1.3. Recommended Metal Solder Stencil Aperture

It is recommended that only 0.152 mm (0.006 inches) or 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. The following combination of metal stencil aperture and metal stencil thickness should be used:

See Figure 18			
t, nominal stencil thickness		**l, length of aperture**	
mm	**inches**	**mm**	**inches**
0.152	0.006	2.0 ± 0.05	0.12 ± 0.002
0.127	0.005	2.0 ± 0.05	0.15 ± 0.002
w, the width of aperture is fixed at 0.70 mm (0.027 inches)			
Aperture opening for shield pad is 2.50 mm x 1.51 mm as per land dimension.			

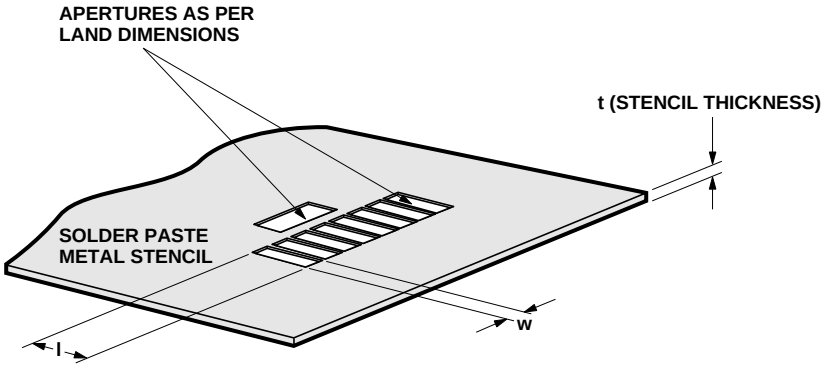


Figure 19. Solder paste stencil aperture.

Appendix B: PCB Layout Suggestion

The following PCB layout guidelines should be followed to obtain a good PSRR and EM immunity, resulting in good electrical performance. Things to note:

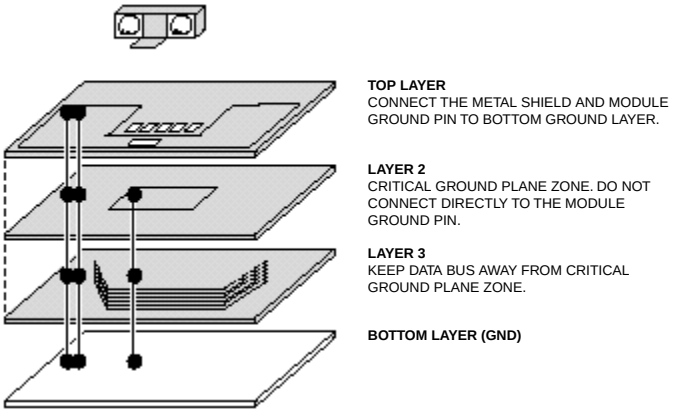
1. The AGND pin should be connected to the ground plane.

2. C1 and C2 are optional supply filter capacitors; they may be left out if a clean power supply is used.

3. VLED can be connected to either unfiltered or unregulated power supply. If VLED and V_{CC} share the same power supply and C1 is used, the connection should be before the current limiting resistor R1. In a noisy environment, including capacitor C2 can enhance supply rejection. C1 is generally a ceramic capacitor of low inductance providing a wide frequency response while C2 is a tantalum capacitor of big volume and fast frequency response. The use of a tantalum capacitor is more critical on the V_{LED} line, which carries a high current.

4. Preferably, a multi-layered board should be used to provide sufficient ground plane. Use the layer underneath and near the transceiver module as V_{CC}, and sandwich that layer between ground connected board layers.

Refer to the diagram below for an example of a 4-layer board.



The area underneath the module at the second layer, and 3 cm in all directions around the module, is defined as the critical ground plane zone. The ground plane should be maximized in this zone. Refer to application note AN1114 or the *Agilent IrDA Data Link Design Guide* for details. The layout below is based on a 2-layer PCB.

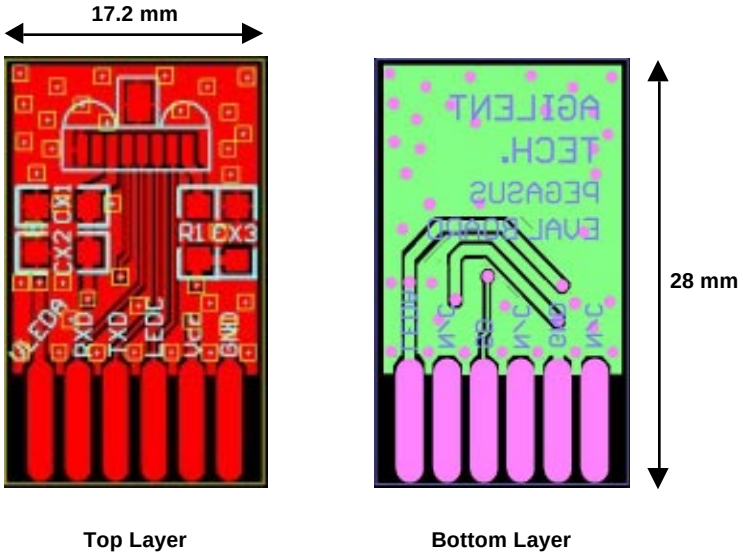


Figure 20. PCB layout suggestion.

Appendix C: General Application Guide for the HSDL-3603 Infrared IrDA® Compliant 4 Mb/s Transceiver

Description

The HSDL-3603 wide voltage operating range infrared transceiver is a low-cost and small form factor that is designed to address the mobile computing market such as notebooks, printers, and LAN access as well as small embedded mobile products such as digital cameras, cellular phones, and PDAs. It is fully compliant to IrDA 1.4 specification up to 4 Mb/s. The design of the HSDL-3603 also includes the following unique features:

- Low passive component count.
- Shutdown mode for low power consumption requirement.
- Single-receive output for all data rates.

Selection of Resistor R1

Resistor R1 should be selected to provide the appropriate peak pulse LED current over different ranges of V_{CC}. The recommended selection of R1 is tabulated in the table on page 3. The HSDL-3603 typically provides 180 mW/Sr of intensity at the recommended minimum peak pulse LED current of 400 mA.

Interface to Recommended I/O chips

The HSDL-3603's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required.

Data rate from 9.6 kb/s up to 4 Mb/s is available at the RXD pin.

Following shows the interface of HSDL-3603 with National Semiconductor's Super I/Os, and the SMC I/O chips.

(A) National Semiconductor Super I/O and Infrared Controller

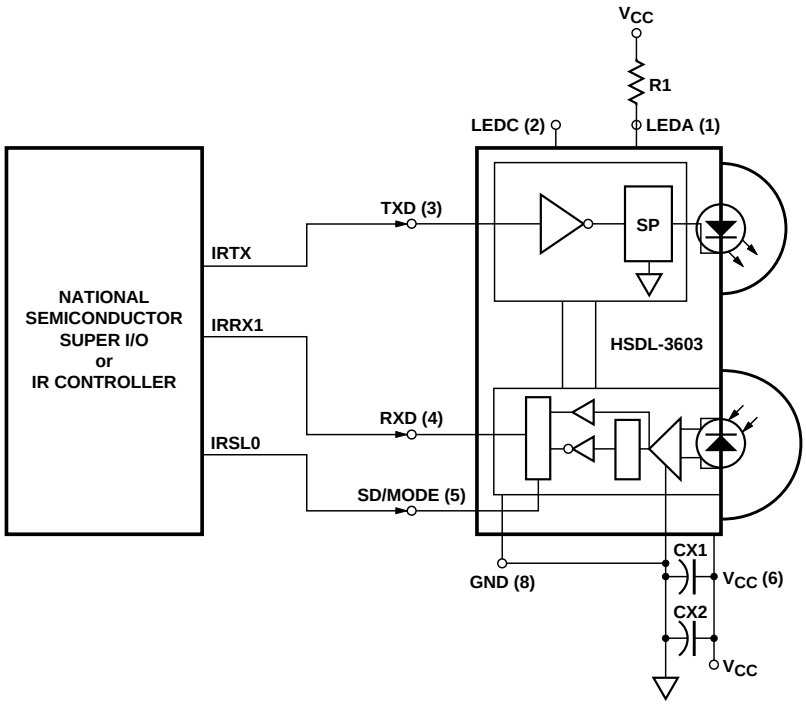
For National Semiconductor Super I/O and Infrared Controller chips, IR link can be realized with the following connections:

- Connect IRTX of the National Super I/O or IR Controller to TXD (pin 3) of the HSDL-3603.
- Connect IRRX1 of the National Super I/O or IR Controller to RXD (pin 4) of the HSDL-3603.
- Connect IRSL0 of the National Super I/O or IR Controller to SD/Mode (pin 5) of the HSDL-3603.

Please refer to the table below for the IR pin assignments for the National Super I/O and IR Controllers that support IrDA 1.4 up to 4 Mb/s:

	IRTX	IRRX1	IRSL0
PC87391/2/3/3F-VJG	70	69	68
PC97338VJG	63	65	66
PC87360/3/4/5/6	57	59	58
PC87309VLJ	44	43	100
PC8(9)7307	81	80	79
PC8(9)7317VUL	81	80	79

Please refer to the National Semiconductor data sheets and application notes for updated information.



HSDL-3603
FUNCTIONAL BLOCK DIAGRAM

Figure 21. NS Super I/O configuration circuit.

(B) Standard Micro System Corporation (SMC) Super and Ultra I/O Controllers

For SMC Super and Ultra I/O Controller chips, IR link can be realized with the following connections:

- Connect IRTX of the SMC Super or Ultra I/O Controller to TXD (pin 3) of the HSDL-3603.
- Connect IRRX of the SMC Super or Ultra I/O Controller to RXD (pin 4) of the HSDL-3603.
- Connect IRMODE of the Super or Ultra I/O Controller to SD/Mode (pin 5) of the HSDL-3603.

Please refer to the table below for the IR pin assignments for the SMC Super or Ultra I/O Controllers that support IrDA 1.4 up to 4 Mb/s:

	IRTX	IRRX	IRMODE
FDC37C669FR	89	88	23
FDC37N769	87	86	21
FDC37C957/8FR	204	203	145 or 190

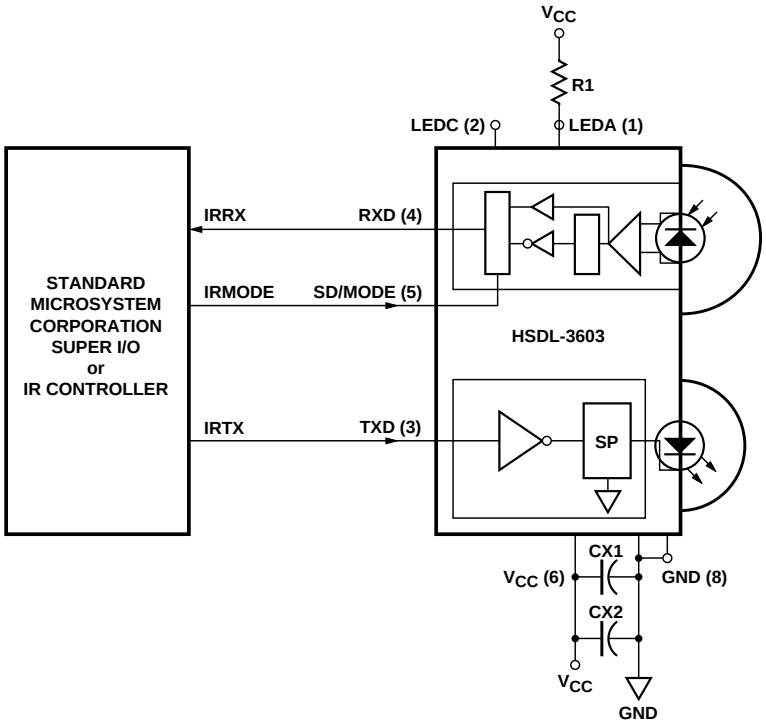


Figure 22. SMC Super I/O configuration circuit.

(C) Mobile Phone and PDA Platform

The block diagrams below show how the IrDA port fits into a mobile phone and PDA platform.

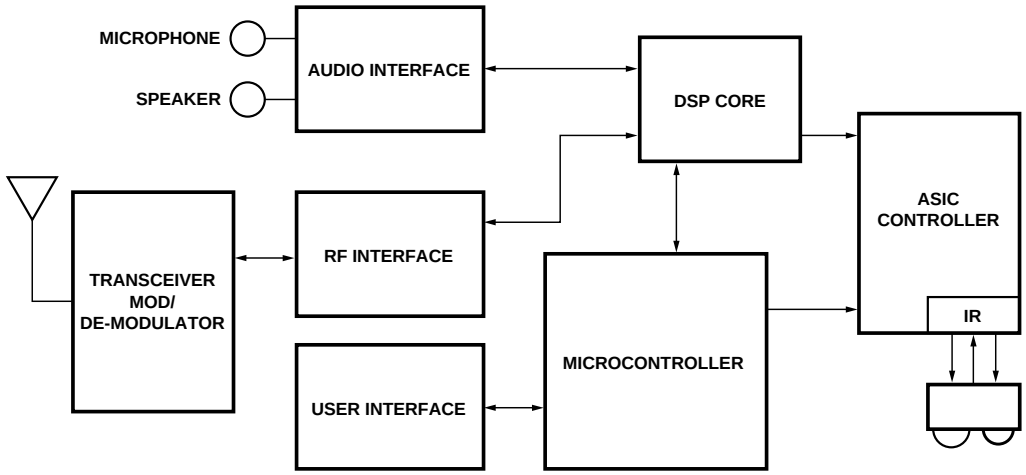


Figure 23. IR layout in mobile phone platform.

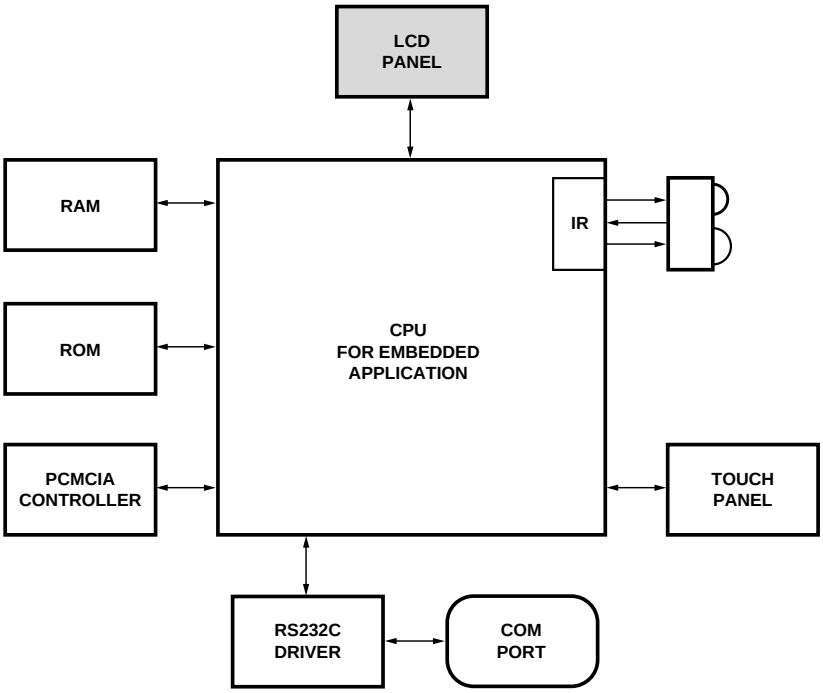


Figure 24. IR layout in PDA platform.

Appendix D: Window Design

Optical Port Dimensions for HSDL-3603:

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30° and the maximum size corresponds to a cone angle of 60°.

In the figure below, X is the width of the window, Y is the height of the window and Z is the distance from the HSDL-3603 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 7.08 mm. The equations for computing the window dimensions are as follows:

$$X = K + 2*(Z + D)*\tan A$$

$$Y = 2*(Z + D)*\tan A$$

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

$$Z' = Z + t/n$$

where 't' is the thickness of the window and 'n' is the refractive index of the window material.

The depth of the LED image inside the HSDL-3603, D, is 8 mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 15° and the maximum is 30°. Assuming the thickness of the window to be negligible, the equations result in the following tables and graphs:

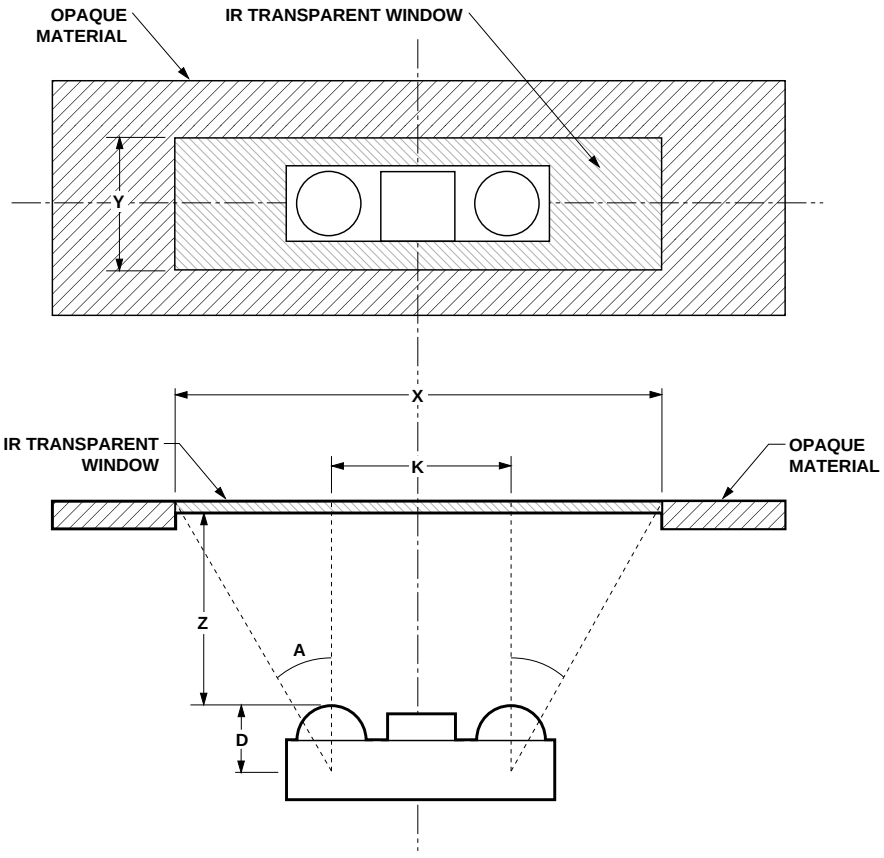


Figure 25. Window design diagram.

Module Depth, (z) mm	Aperture Width (x, mm)		Aperture Height (y, mm)	
	max.	min.	max.	min.
0	16.318	11.367	9.238	4.287
1	17.472	11.903	10.392	4.823
2	18.627	12.439	11.547	5.359
3	19.782	12.975	12.702	5.895
4	20.936	13.511	13.856	6.431
5	22.091	14.047	15.011	6.967
6	23.246	14.583	16.166	7.503
7	24.401	15.118	17.321	8.038
8	25.555	15.654	18.475	8.574
9	26.710	16.190	19.630	9.110

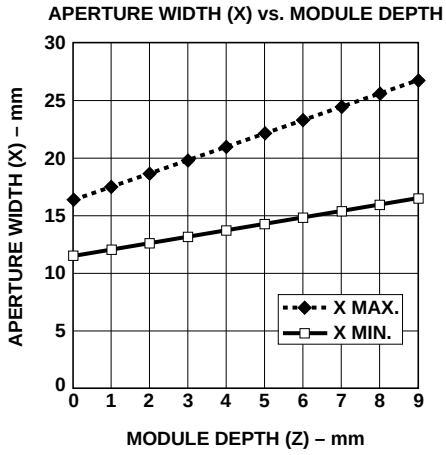


Figure 26. Aperture width (X) vs. module depth.

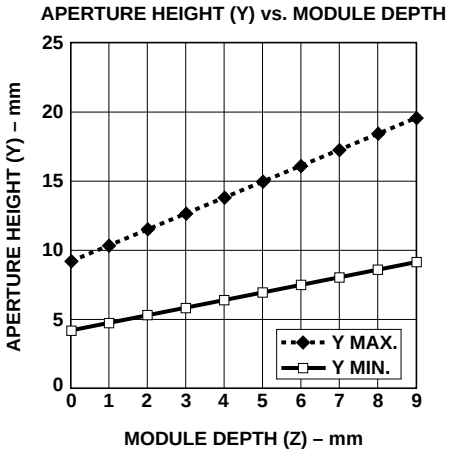


Figure 27. Aperture height (Y) vs. module depth.

Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 875 nm.

The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

Recommended Plastic Materials:

Material Number	Light Transmission	Haze	Refractive Index
Lexan 141L	88%	1%	1.586
Lexan 920A	85%	1%	1.586
Lexan 940A	85%	1%	1.586

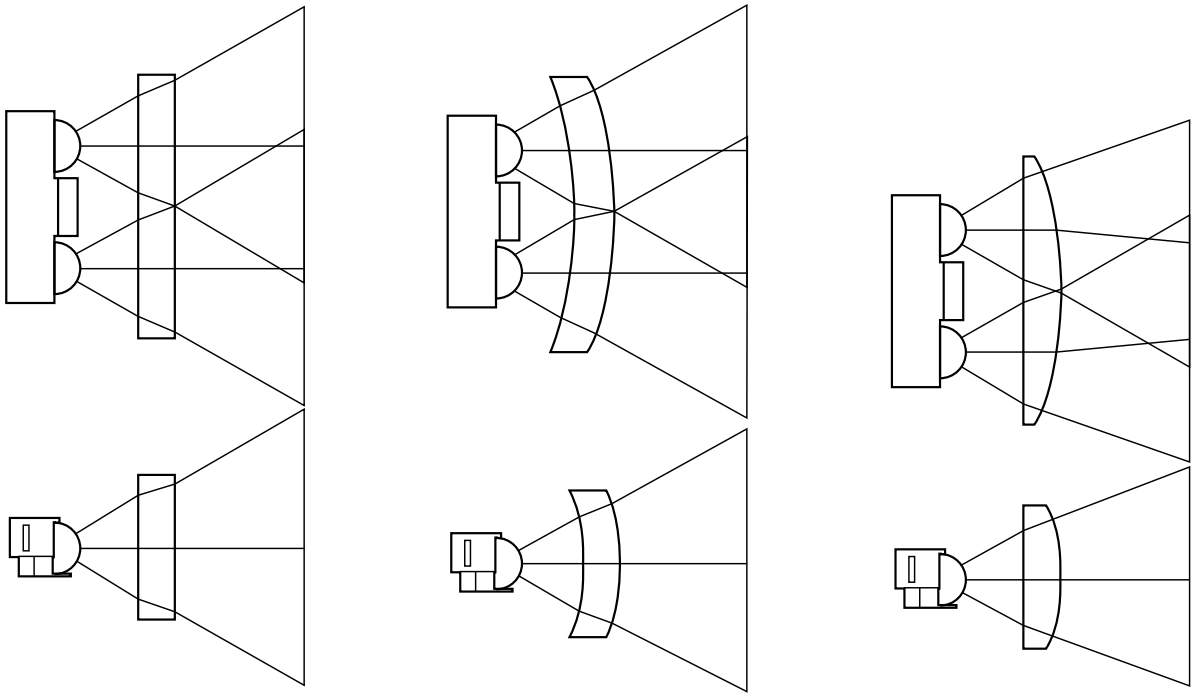
Note: 920A and 940A are more flame retardant than 141L.
Recommended Dye: Violet #21051 (IR transmissant above 625 nm).

Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.



Flat Window (First Choice)

Curved Front and Back (Second Choice)

Curved Front, Flat Back (Do Not Use)

Figure 28. Window design choices.

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Data subject to change.

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