PCA9509

Level translating I²C-bus/SMBus repeater

1. General description

The PCA9509 is a level translating I²C-bus/SMBus repeater that enables processor low voltage 2-wire serial bus to interface with standard I²C-bus or SMBus I/O. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling the I²C-bus or SMBus maximum capacitance of 400 pF on the higher voltage side. Port A allows a voltage range from 1.0 V (as low as 0.95 V in special cases) to $V_{CC(B)} - 1.0$ V and requires no external pull-up resistors due to the internal current source. Port B allows a voltage range from 3.0 V to 5.5 V and is overvoltage tolerant. Both port A and port B SDA and SCL pins are high-impedance when the PCA9509 is unpowered.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. Port A uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on the port A accommodating smaller voltage swings. The output pull-down on the port A internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables port B to connect to any other I²C-bus devices or buffer.

The PCA9509 drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

2. Features

- Bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (1 V [0.95 V in special cases] to $V_{CC(B)} - 1.0$ V) to port B (3.0 V to 5.5 V)
- Requires no external pull-up resistors on lower voltage port A
- Active HIGH repeater enable input
- Open-drain inputs/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins

■ Operating supply voltage range of 1.0 V (0.95 V in special cases) to $V_{CC(B)} - 1.0$ V on port A, 3.0 V to 5.5 V on port B

■ 5 V tolerant port B SCL, SDA and enable pins

■ 0 Hz to 400 kHz clock frequency

Remark: The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

■ ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101

■ Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

■ Packages offered: TSSOP8, SO8, XQFN8

3. Ordering information

Table 1.   Ordering information

Type number	Topside mark	Package		
		Name	**Description**	**Version**
PCA9509D	PCA9509	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9509DP	9509	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9509GM	P9X[1]	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body $1.6 \times 1.6 \times 0.5$ mm	SOT902-1

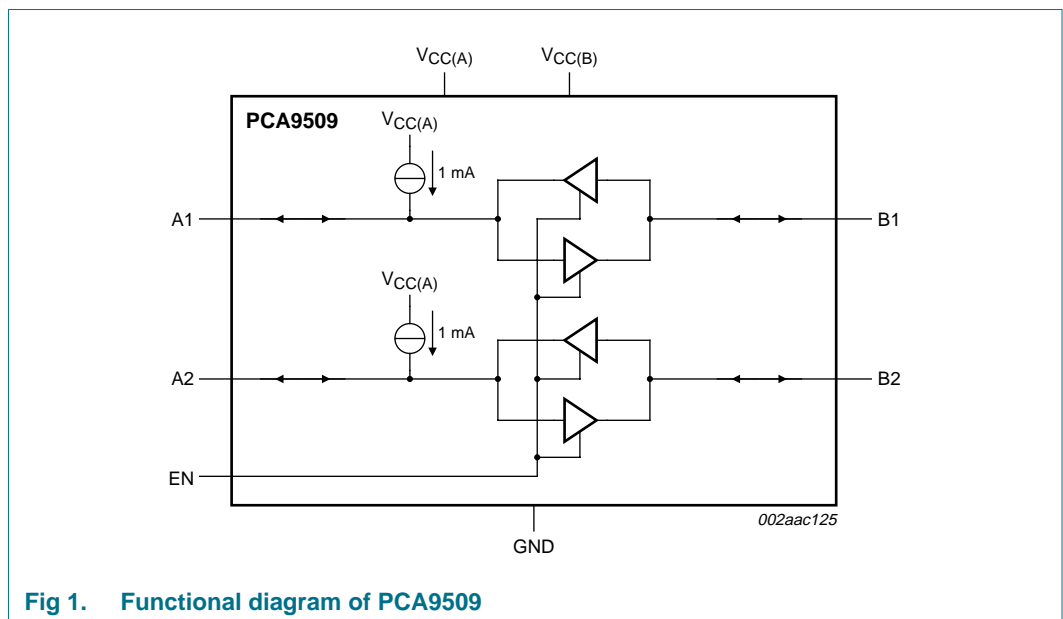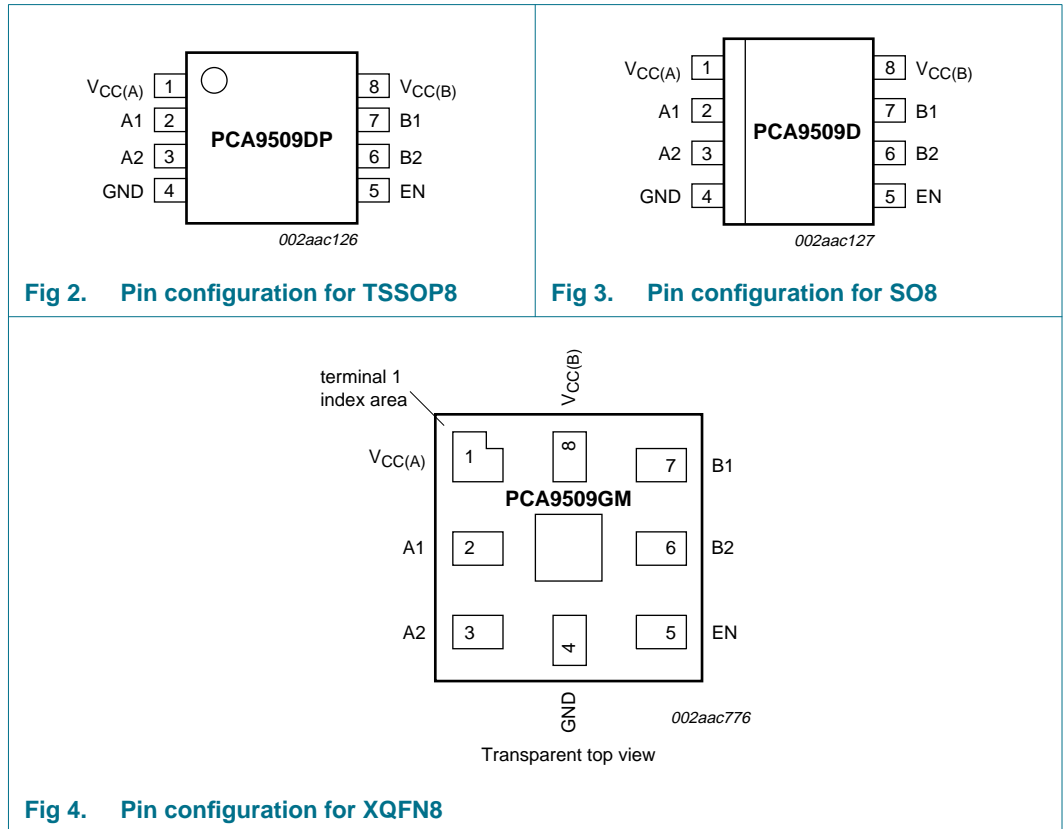[1]   'X' will change based on date code.

4. Functional diagram

Fig 1.   Functional diagram of PCA9509

PCA9509_5

Product data sheet **Rev. 05 — 10 July 2009** **2 of 19**

5. Pinning information

5.1 Pinning

Fig 2. **Pin configuration for TSSOP8**

Fig 3. **Pin configuration for SO8**

Fig 4. **Pin configuration for XQFN8**

5.2 Pin description

Table 2. **Pin description**

Symbol	Pin	Description
$V_{CC(A)}$	1	port A power supply
A1[1]	2	port A (lower voltage side)
A2[1]	3	port A (lower voltage side)
GND	4	ground (0 V)
EN	5	enable input (active HIGH)
B2[1]	6	port B (SMBus/I²C-bus side)
B1[1]	7	port B (SMBus/I²C-bus side)
$V_{CC(B)}$	8	port B power supply

[1] Port A and port B can be used for either SCL or SDA.

6. Functional description

Refer to Figure 1 "Functional diagram of PCA9509".

The PCA9509 enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 1.0 V (as low as 0.95 V in special cases) without degradation of system performance. The PCA9509 contains 2 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage and 3.3 V SMBus or 5 V I²C-bus. The port B I/Os are over-voltage tolerant to 5.5 V even when the device is unpowered.

The PCA9509 includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.5 V and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up. After power-up and with the EN pin HIGH, a LOW level on port A (below approximately 0.15 V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0 V. When port A rises above approximately 0.15 V, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below $0.3V_{CC(B)}$, the port A driver is turned on and port A pulls down to 0.2 V (typical). The port B pull-down is not enabled unless the port A voltage goes below V_{ILc}. If the port A low voltage goes below V_{ILc}, the port B pull-down driver is enabled until port A rises above approximately 0.15 V (V_{ILc}), then port B, if not externally driven LOW, will continue to rise being pulled up by the external pull-up resistor.

Remark: Ground offset between the PCA9509 ground and the ground of devices on port A of the PCA9509 must be avoided.

The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less (R = E / I). Such a driver will share enough current with the port A output pull-down of the PCA9509 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILc} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV.

Bus repeaters that use an output offset are not interoperable with the port A of the PCA9509 as their output LOW levels will not be recognized by the PCA9509 as a LOW. If the PCA9509 is placed in an application where the V_{IL} of port A of the PCA9509 does not go below its V_{ILc} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided.

Port B is interoperable with all I²C-bus slaves, masters and repeaters.

6.1 Enable

The EN pin is active HIGH and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled.

The enable pin should only change state when the bus and the repeater port are in an idle state to prevent system failures.

6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system. Each of the port A I/Os has an internal pull-up current source and does not require the external pull-up resistor. Port B is designed to work with Standard-mode and Fast-mode I²C-bus devices in addition to SMBus devices. Standard-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

7. Application design-in information

A typical application is shown in Figure 5. In this example, the CPU is running on a 1.1 V I²C-bus while the master is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.
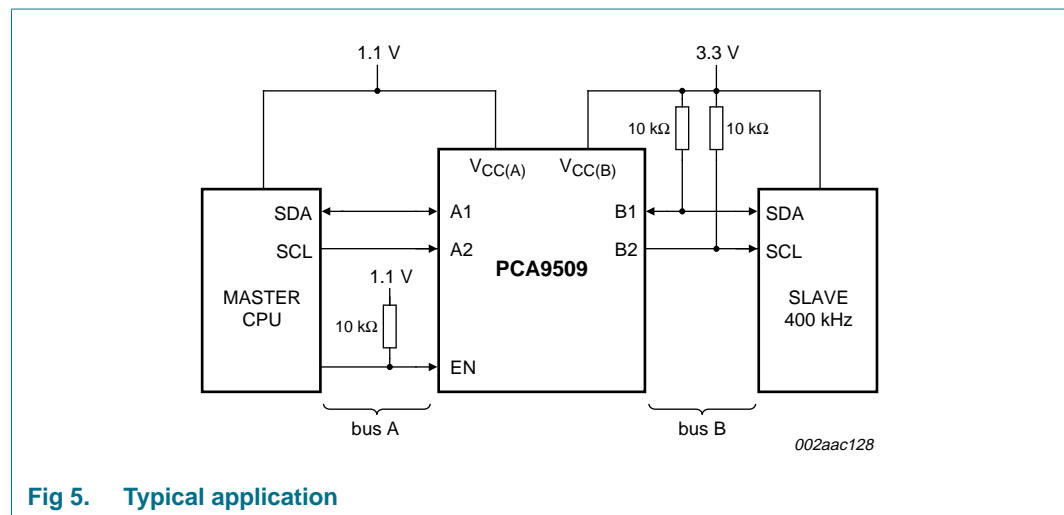

Fig 5.   Typical application

When port B of the PCA9509 is pulled LOW by a driver on the I²C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PCA9509 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 6 and Figure 7. If the bus master in Figure 5 were to write to the slave through the PCA9509, waveforms shown in Figure 6 would be observed on the B bus. This looks like a normal I²C-bus transmission.

On the A bus side of the PCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9509. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9509 for a short delay while the B bus side rises above $0.5V_{CC(B)}$, then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the A bus side at the input of the PCA9509 (V_{IL}) is below V_{ILc} to be recognized by the PCA9509 and then transmitted to the B bus side.
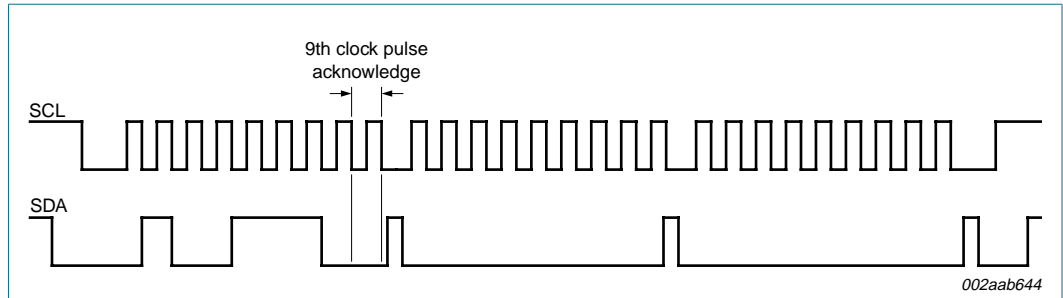
PCA9509_5

Product data sheet **Rev. 05 — 10 July 2009** 5 of 19

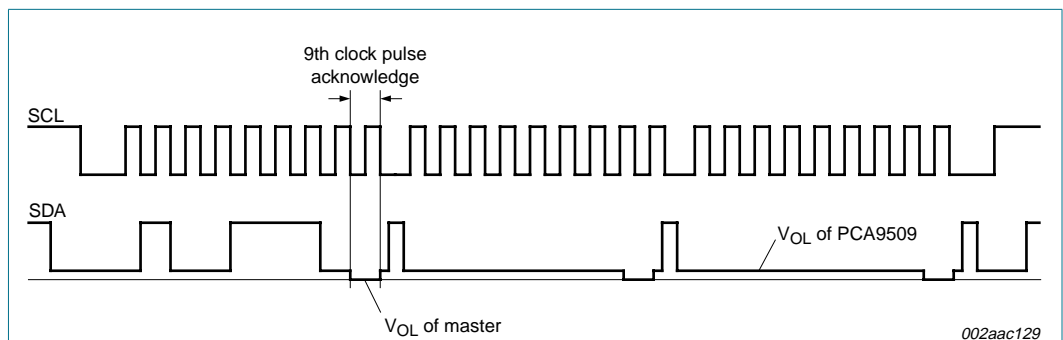**Fig 6.** **Bus B SMBus/I²C-bus waveform**

Fig 7. **Bus A lower voltage waveform**

8. Limiting values

Table 3. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(B)}$	supply voltage port B		−0.5	+6.0	V
$V_{CC(A)}$	supply voltage port A		−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin	port A	−0.5	+6.0	V
		port B; enable pin (EN)	−0.5	+6.0	V
$I_{I/O}$	input/output current		-	±20	mA
I_I	input current		-	±20	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating in free air	−40	+85	°C
T_j	junction temperature		-	+125	°C
T_{sp}	solder point temperature	10 s max.	-	300	°C

PCA9509_5

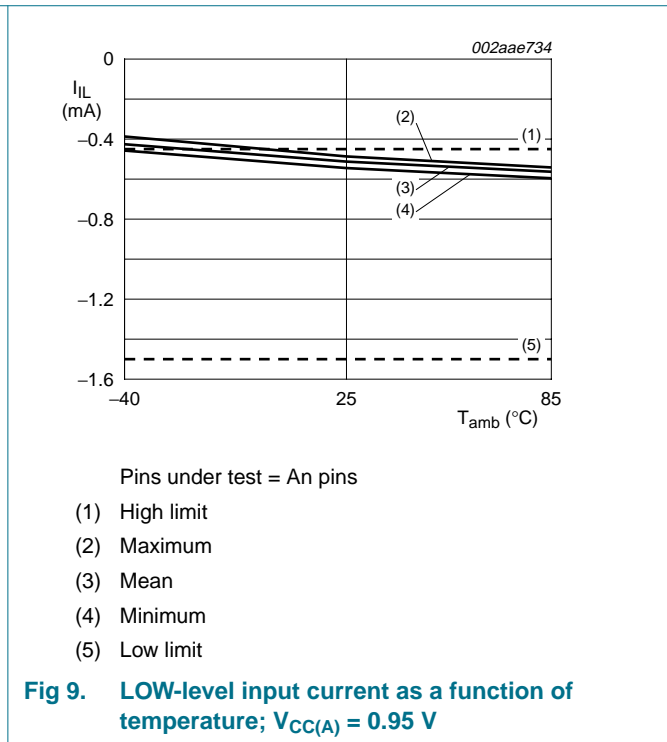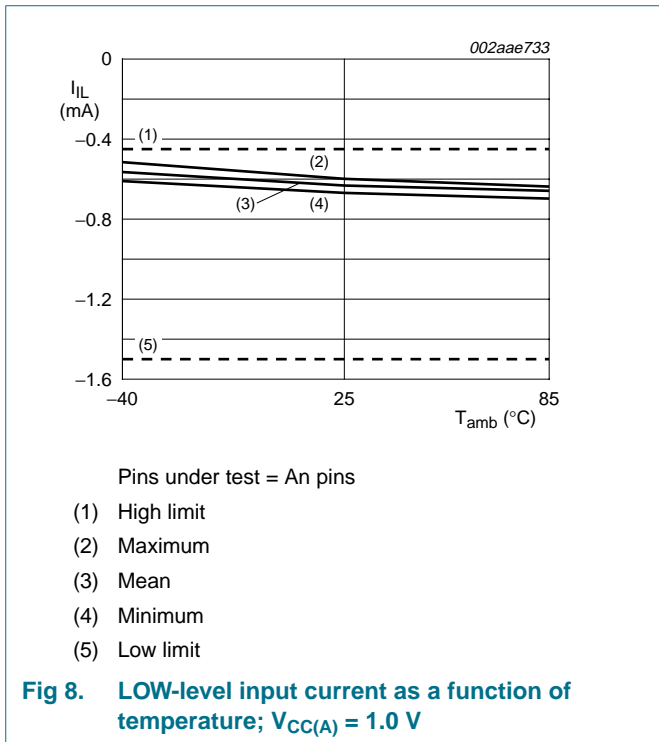**Product data sheet** Rev. 05 — 10 July 2009 6 of 19

9. Static characteristics

Table 4. Static characteristics

GND = 0 V; $T_{amb} = -40\,°C$ to $+85\,°C$; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supplies							
$V_{CC(B)}$	supply voltage port B			3.0	-	5.5	V
$V_{CC(A)}$	supply voltage port A			1.0[2]	-	$V_{CC(B)} - 1$	V
$I_{CC(A)}$	supply current port A	all port A static HIGH		0.25	0.45	0.9	mA
		all port A static LOW		1.25	3.0	5	mA
$I_{CC(B)}$	supply current port B	all port B static HIGH		0.5	0.9	1.1	mA
Input and output of port A (A1 to A2)							
V_{IH}	HIGH-level input voltage	port A		$0.7V_{CC(A)}$	-	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	port A	[3]	−0.5	-	+0.3	V
V_{ILc}	contention LOW-level input voltage		[3]	−0.5	+0.15	-	V
V_{IK}	input clamping voltage	$I_L = -18$ mA		−1.5	-	−0.5	V
I_{LI}	input leakage current	$V_I = V_{CC(A)}$		-	-	±1	µA
I_{IL}	LOW-level input current		[4]	−1.5	−1.0	−0.45	mA
V_{OL}	LOW-level output voltage	$V_{CC(A)} = 0.95$ V to 1.2 V	[5]	-	0.18	0.25	V
		$V_{CC(A)} = > 1.2$ V to $(V_{CC(B)} - 1$ V)	[5]	-	0.2	0.3	V
$V_{OL}-V_{ILc}$	difference between LOW-level output and LOW-level input voltage contention		[6]	-	50	-	mV
I_{LOH}	HIGH-level output leakage current	$V_O = 1.1$ V		-	-	10	µA
C_{io}	input/output capacitance			-	6	7	pF
Input and output of port B (B1 to B2)							
V_{IH}	HIGH-level input voltage	port B		$0.7V_{CC(B)}$	-	$V_{CC(B)}$	V
V_{IL}	LOW-level input voltage	port B		−0.5	-	$+0.3V_{CC(B)}$	V
V_{IK}	input clamping voltage	$I_L = -18$ mA		−1.5	-	−0.5	V
I_{LI}	input leakage current	$V_I = 3.6$ V		−1.0	-	+1.0	µA
I_{IL}	LOW-level input current	$V_I = 0.2$ V		-	-	10	µA
V_{OL}	LOW-level output voltage	$I_{OL} = 6$ mA		-	0.1	0.2	V
I_{LOH}	HIGH-level output leakage current	$V_O = 3.6$ V		-	-	10	µA
C_{io}	input/output capacitance			-	3	5	pF
Enable							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.1V_{CC(A)}$	V
V_{IH}	HIGH-level input voltage			$0.9V_{CC(A)}$	-	$V_{CC(B)}$	V
$I_{IL(EN)}$	LOW-level input current on pin EN	$V_I = 0.2$ V, EN; $V_{CC} = 3.6$ V		−1	-	+1	µA
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance	$V_I = 3.0$ V or 0 V		-	2	3	pF

[1] Typical values with $V_{CC(A)} = 1.1$ V, $V_{CC(B)} = 5.0$ V.

[2] If the PCA9509 is not being enabled or disabled, the $V_{CC(A)}$ minimum is 0.95 V with a corresponding decrease in the I_{IL}, which will drop below the minimum specification of −450 μA at cold temperature (see Figure 8 and Figure 9). This will not significantly change the rise and fall times of the signals on port A since the I_{IL} value represents the current source pull-up current, so a lower current into the same capacitance will result in a slower rise time and a longer transition time in general, however since the lower current is also associated with a lower voltage swing the delay is somewhat compensated. The key point of the graphs is that the current has a temperature dependence, and the output driver will also have the same temperature dependency so that the output offset of ~200 mV on port A is nearly temperature independent. Even though the I_{IL} parameter indicates that at $V_{CC(A)}$ of 0.95 V the PCA9509 can only sink up to 400 μA instead of 450 μA at cold temperature, the output is designed to be somewhat resistive such that under nominal conditions (1.1 V) the current source pull-up will source 1 mA and the output pull-down will sink the 1 mA at ~200 mV, so as the current source current decreases the output pull-down resistance increases in order to maintain the offset.

[3] V_{IL} specification is for the falling edge seen by the port A input. V_{ILc} is for the static LOW levels seen by the port A input resulting in port B output staying LOW.

[4] The port A current source has a typical value of about 1 mA, but varies with both $V_{CC(A)}$ and $V_{CC(B)}$. Below $V_{CC(A)}$ of about 0.7 V the port A current source current drops to 0 mA. The current source current dropping across the internal pull-down driver resistance of about 200 Ω defines the V_{OL}.

[5] As long as the chip ground is common with the input ground reference the driver resistance may be as large as 120 Ω. However, ground offset will rapidly decrease the maximum allowed driver resistance.

[6] Guaranteed by design.

Pins under test = An pins

(1) High limit
(2) Maximum
(3) Mean
(4) Minimum
(5) Low limit

Fig 8. LOW-level input current as a function of temperature; $V_{CC(A)}$ = 1.0 V

Pins under test = An pins

(1) High limit
(2) Maximum
(3) Mean
(4) Minimum
(5) Low limit

Fig 9. LOW-level input current as a function of temperature; $V_{CC(A)}$ = 0.95 V

10. Dynamic characteristics

Table 5.   Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V$_{CC(A)}$ = 1.1 V; V$_{CC(B)}$ = 3.3 V							
t$_{PLH}$	LOW to HIGH propagation delay	port B to port A	[1]	69	109	216	ns
t$_{PHL}$	HIGH to LOW propagation delay	port B to port A	[1]	63	86	140	ns
t$_{TLH}$	LOW to HIGH output transition time	port A	[1]	14	22	96	ns
t$_{THL}$	HIGH to LOW output transition time	port A	[1]	5	8.1	16	ns
t$_{PLH}$	LOW to HIGH propagation delay	port A to port B	[1]	−69	−91	−139	ns
t$_{PLH2}$	LOW to HIGH propagation delay 2	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	[1]	91	153	226	ns
t$_{PHL}$	HIGH to LOW propagation delay	port A to port B	[1]	73	122	183	ns
t$_{TLH}$	LOW to HIGH output transition time	port B	[1][2]	-	61	-	ns
t$_{THL}$	HIGH to LOW output transition time	port B	[1]	15	24	40	ns
t$_{su}$	set-up time	EN HIGH before START condition		100	-	-	ns
t$_h$	hold time	EN HIGH after STOP condition		100	-	-	ns
V$_{CC(A)}$ = 1.9 V; V$_{CC(B)}$ = 5.0 V							
t$_{PLH}$	LOW to HIGH propagation delay	port B to port A	[1]	69	105	216	ns
t$_{PHL}$	HIGH to LOW propagation delay	port B to port A	[1]	63	86	140	ns
t$_{TLH}$	LOW to HIGH output transition time	port A	[1]	14	27	96	ns
t$_{THL}$	HIGH to LOW output transition time	port A	[1]	5	8	35	ns
t$_{PLH}$	LOW to HIGH propagation delay	port A to port B	[1]	−69	−89	−139	ns
t$_{PLH2}$	LOW to HIGH propagation delay 2	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	[1]	91	131	226	ns
t$_{PHL}$	HIGH to LOW propagation delay	port A to port B	[1]	73	99	183	ns
t$_{TLH}$	LOW to HIGH output transition time	port B	[1][2]	-	65	-	ns
t$_{THL}$	HIGH to LOW output transition time	port B	[1]	15	31	40	ns
t$_{su}$	set-up time	EN HIGH before START condition		100	-	-	ns
t$_h$	hold time	EN HIGH after STOP condition		100	-	-	ns

[1]   Load capacitance = 50 pF; load resistance on port B = 1.35 kΩ.

[2]   Value is determined by RC time constant of bus line.

PCA9509_5

Product data sheet **Rev. 05 — 10 July 2009** **9 of 19**
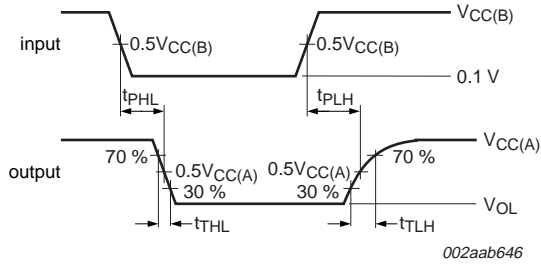
10.1 AC waveforms

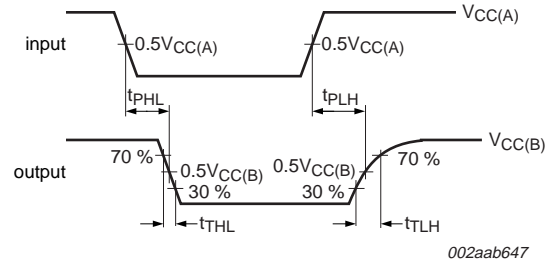**Fig 10. Propagation delay and transition times; port B to port A**

Fig 11. Propagation delay and transition times; port A to port B
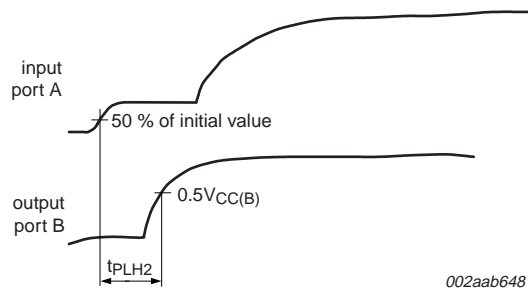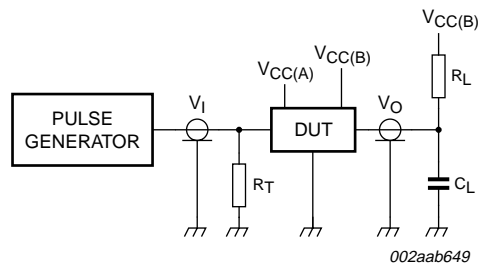

Fig 12. Propagation delay from the port A's external driver switching off to port B LOW-to-HIGH transition; port A to port B

11. Test information

R_L = load resistor; 1.35 kΩ on port B

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 13. Test circuit for open-drain outputs

Level translating I2C-bus/SMBus repeater

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				99-12-27 03-02-18

Fig 14. Package outline SOT96-1 (SO8)

PCA9509_5

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm   **SOT505-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D[1]	E[2]	e	H_E	L	L_p	v	w	y	Z[1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						99-04-09 03-02-18
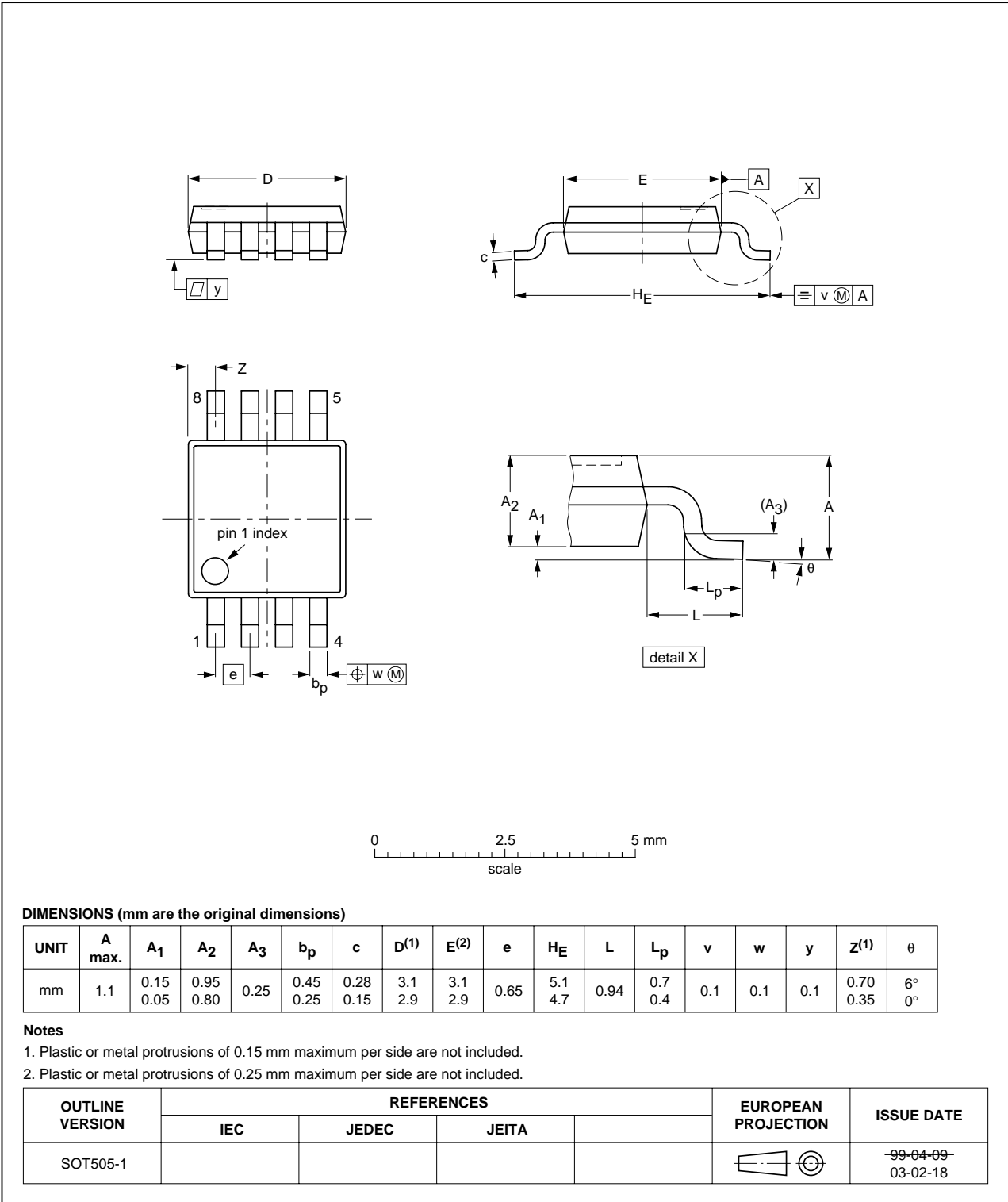
Fig 15. Package outline SOT505-1 (TSSOP8)

XQFN8U: plastic extremely thin quad flat package; no leads;
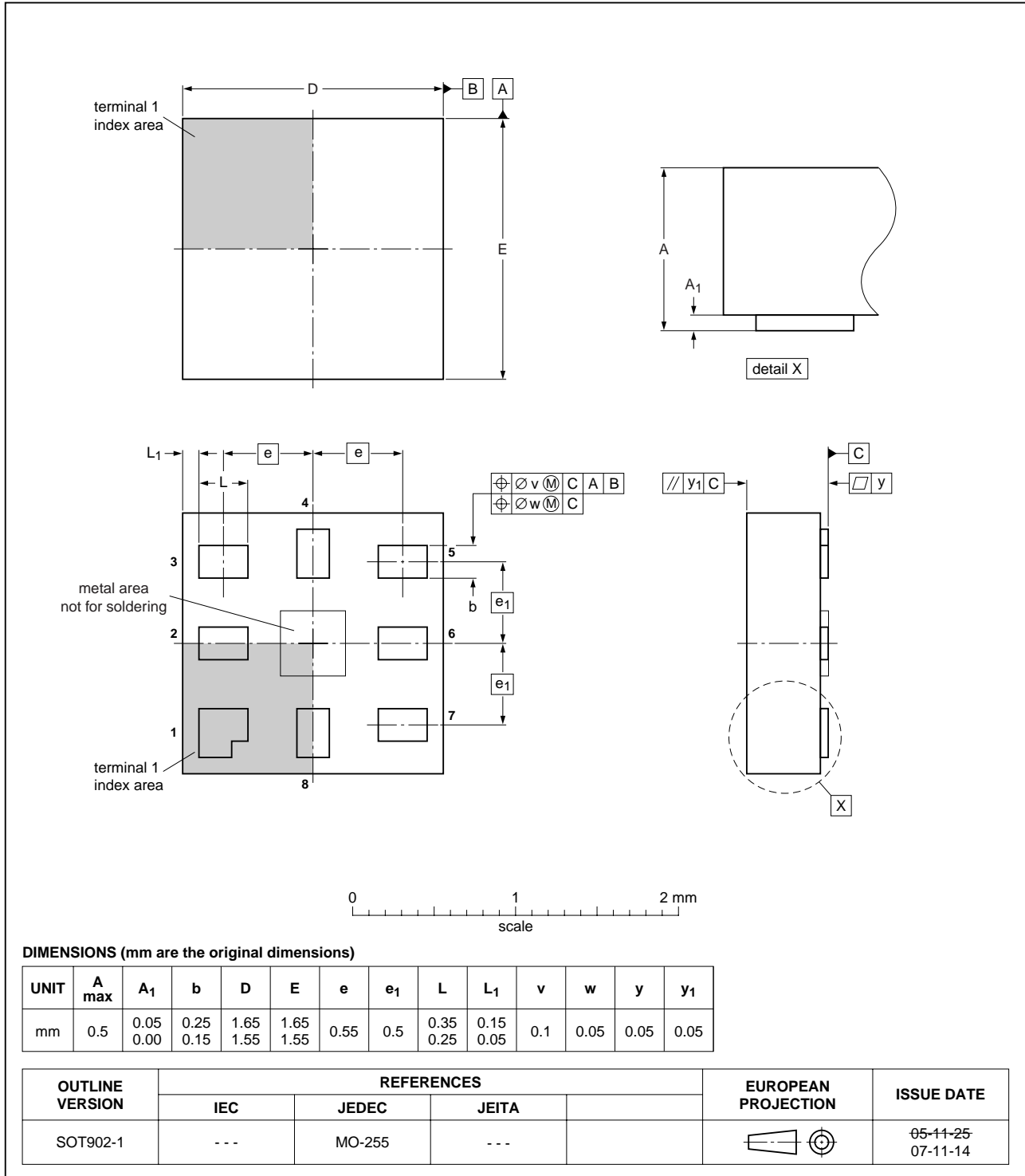**8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm**

SOT902-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A₁	b	D	E	e	e₁	L	L₁	v	w	y	y₁
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT902-1	- - -	MO-255	- - -		05-11-25 07-11-14

Fig 16.   Package outline SOT902-1 (XQFN8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6 and 7

Table 6. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.

MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components
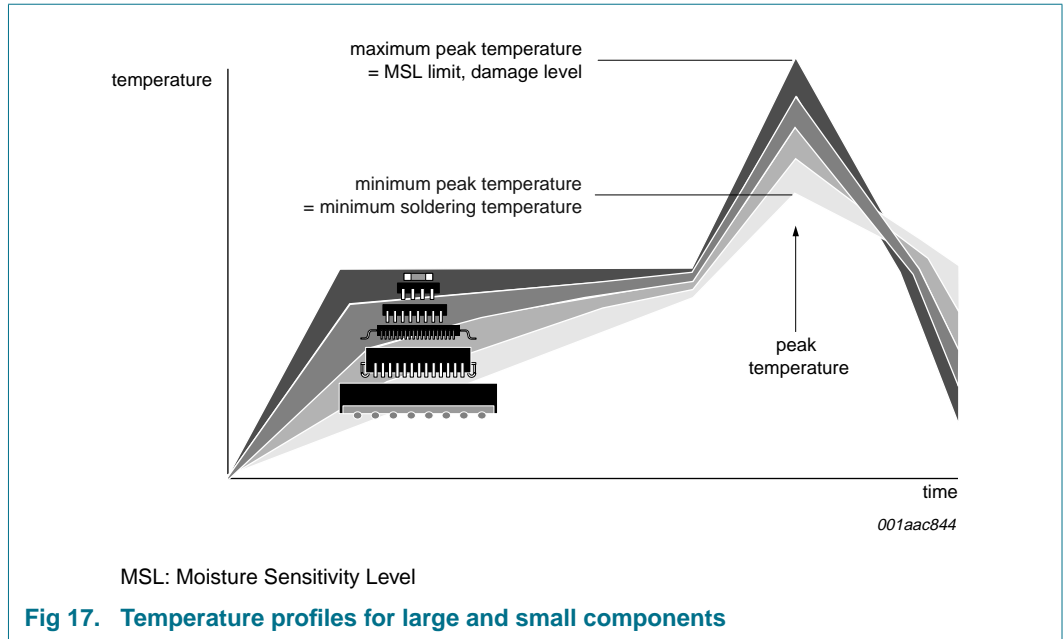
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 8. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
MM	Machine Model
NMOS	Negative-channel Metal-Oxide Semiconductor
RC	Resistor-Capacitor network
SMBus	System Management Bus

15. Revision history

Table 9.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9509_5	20090710	Product data sheet	-	PCA9509_4
Modifications:	• Table 4 "Static characteristics", sub-section "Input and output of port A (A1 to A2), symbol V_{OL} is split according to 2 different supply voltage conditions			
PCA9509_4	20090617	Product data sheet	-	PCA9509_3
PCA9509_3	20090611	Product data sheet	-	PCA9509_2
PCA9509_2	20070629	Product data sheet	-	PCA9509_1
PCA9509_1	20060627	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

PCA9509_5

Product data sheet **Rev. 05 — 10 July 2009** **18 of 19**

18. Contents

founded by

PHILIPS