CY8CLED02

EZ-Color™ HB LED Controller

Features

■ HB LED Controller
- ❒ Configurable Dimmers Support up to 2 Independent LED Channels
- ❒ 8-32 Bits of Resolution per Channel
- ❒ Dynamic Reconfiguration Enables LED Controller plus other Features; Battery Charging, Motor Control

■ Visual Embedded Design
- ❒ LED-Based Drivers
  - • Binning Compensation
  - • Temperature Feedback
  - • Optical Feedback
  - • DMX512

■ PrISM Modulation Technology
- ❒ Reduces Radiated EMI
- ❒ Reduces Low Frequency Blinking

■ Powerful Harvard Architecture Processor
- ❒ M8C Processor Speeds to 24 MHz
- ❒ 3.0 to 5.25V Operating Voltage
- ❒ Operating Voltages down to 1.0V using On-Chip Switch Mode Pump (SMP)
- ❒ Industrial Temperature Range: -40°C to +85°C

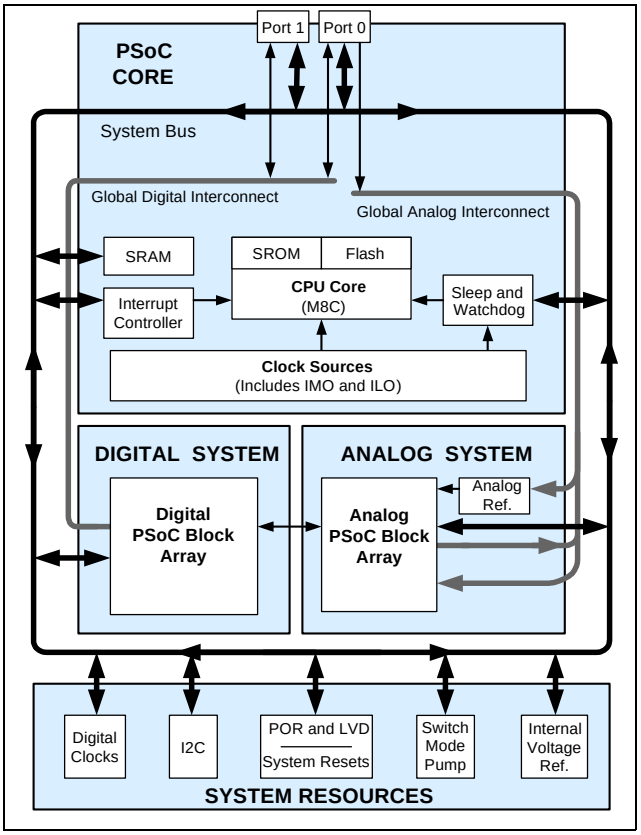
■ Flexible On-Chip Memory
- ❒ 4K Flash Program Storage 50,000 Erase/Write Cycles
- ❒ 256 Bytes SRAM Data Storage
- ❒ In-System Serial Programming (ISSP)
- ❒ Partial Flash Updates
- ❒ Flexible Protection Modes
- ❒ EEPROM Emulation in Flash

■ Advanced Peripherals (PSoC Blocks)
- ❒ 4 Digital PSoC Blocks Provide:
  - • 8 to 32-Bit Timers, Counters, and PWMs
  - • Full-Duplex UART
  - • Multiple SPI Masters or Slaves
  - • Connectable to all GPIO Pins
- ❒ 4 Rail-to-Rail Analog PSoC Blocks Provide:
  - • Up to 14-Bit ADCs
  - • Up to 9-Bit DACs
  - • Programmable Gain Amplifiers
  - • Programmable Filters and Comparators
- ❒ Complex Peripherals by Combining Blocks

■ Programmable Pin Configurations
- ❒ 25 mA Sink, 10 mA Source on all GPIO
- ❒ Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
- ❒ Up to 12 Analog Inputs on GPIO
- ❒ Four 30 mA Analog Outputs on GPIO
- ❒ Configurable Interrupt on all GPIO

■ Complete Development Tools
- ❒ Free Development Software
  - • PSoC Designer™
- ❒ Full featured, In-Circuit Emulator and Programmer
- ❒ Full Speed Emulation
- ❒ Complex Breakpoint Structure
- ❒ 128 KBytes Trace Memory

Logic Block Diagram



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EZ-Color™ Functional Overview

Cypress's EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip™); with Cypress' PrISM (precise illumination signal modulation) drive technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports a range of independent LED channels from 4 channels at 32 bits of resolution each, up to 16 channels at 8 bits of resolution each. This enables lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature, optical, and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enables the simple integration of features in addition to intelligent lighting, such as Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress's best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

- LCD Backlight
- Large Signs
- General Lighting
- Architectural Lighting
- Camera/Cell Phone Flash
- Flashlights

The PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and an IMO (internal main oscillator) and an ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful, four MIPS, 8-bit Harvard architecture microprocessor with speeds up to 24 MHz.

System Resources provide additional capability, such as digital clocks to increase the flexibility of the PSoC; I2C functionality for implementing an I2C master, slave, or multi-master; an internal voltage reference that provides an absolute value of 1.3V to a number of PSoC subsystems; a switch mode pump (SMP) that generates normal operating voltages off a single battery cell; and various system resets supported by the M8C.

The Digital System is composed of an array of digital blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global busses that can route any signal to any pin, freeing designers from the constraints of a fixed peripheral controller.

The Analog System consists of four analog blocks, supporting comparators, and analog-to-digital conversion up to 10 bits of precision.

The Digital System

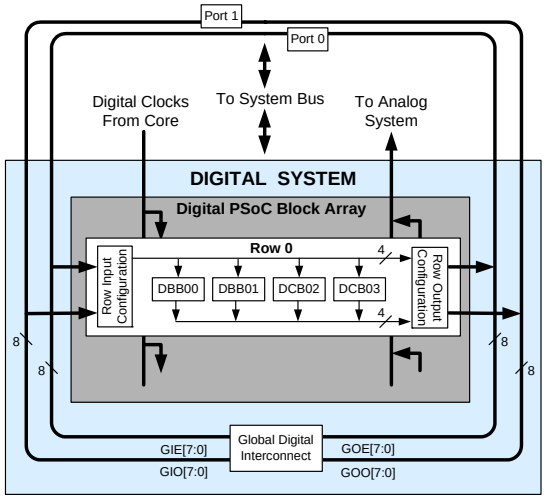
The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include those listed below.

- PrISM (8 to 32 bit)
- PWMs (8 to 32 bit)
- PWMs with dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave, master, multi-master (1 available as a System Resource)
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA (up to 4)
- Generators (8 to 32 bit)

Connect the digital blocks to any GPIO through a series of global busses that can route any signal to any pin. The busses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.

Figure 1. Digital System Block Diagram



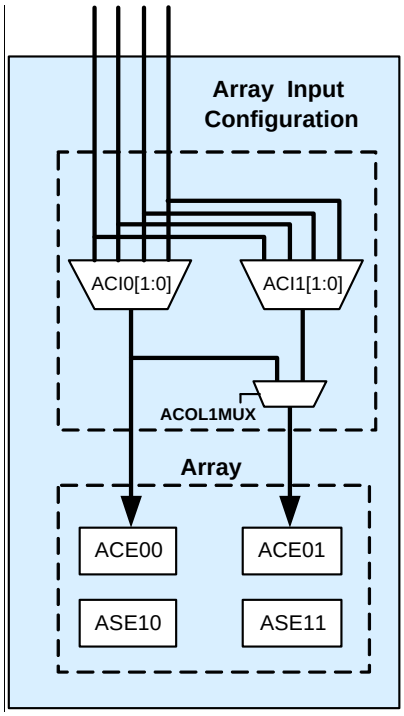
The Analog System

The analog system is composed of four configurable blocks that enable creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (single or dual, with 10-bit resolution)
- Pin-to-pin comparators (1)
- Single-ended comparators (up to 2) with absolute (1.3V) reference or 8-bit DAC reference
- 1.3V reference (as a System Resource)

In most PSoC based devices, analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks. This particular EZ-Color device provides limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital blocks as clock dividers.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table

Table 1. EZ-Color Device Characteristics

Part Number	LED Channels	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense
CY8CLED02	2	16	1	4	8	0	2	4	256 Bytes	4K	No
CY8CLED04	4	56	1	4	48	2	2	6	1K	16K	Yes
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	44	4	16	12	4	4	12	2K	32K	No

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest device data sheets on the web at http://www.cypress.com/ez-color.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com/store, click Lighting & Power Control to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to http://www.cypress.com/techtrain.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located at the center of the web page, and select CYPros Consultants.

Technical Support

Application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support.

Application Notes

A long list of application notes will assist you in every aspect of your design effort. To view the application notes, go to the http://www.cypress.com web site and select Application Notes under the Documentation tab.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Designer. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional Integrated Development Environment (IDE) based on PSoC Designer. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose I/O
I/O	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
PWM	pulse width modulator
ROM	read only memory
SC	switched capacitor
SMP	switch mode pump
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 9 on page 13 lists all the abbreviations used to measure the devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Pin Information

Pinouts

This section describes, lists, and illustrates the CY8CLED02 EZ-Color device pins and pinout configurations. The CY8CLED02 device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, SMP, and XRES are not capable of Digital I/O.

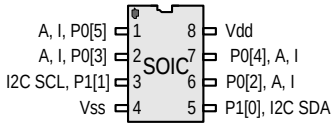
8-Pin Part Pinout

Table 3. 8-Pin Part Pinout (SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input.
2	I/O	I	P0[3]	Analog column mux input.
3	I/O		P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
4	Power		Vss	Ground connection.
5	I/O		P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
6	I/O	I	P0[2]	Analog column mux input.
7	I/O	I	P0[4]	Analog column mux input.
8	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. 8-Pin EZ-Color Device



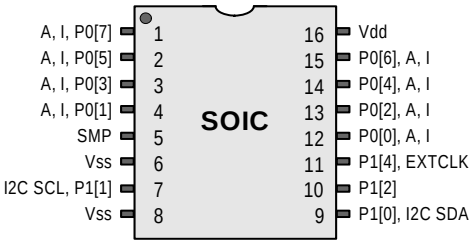
16-Pin Part Pinout

Table 4. 16-Pin Part Pinout (SOIC)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input.
2	I/O	I	P0[5]	Analog column mux input.
3	I/O	I	P0[3]	Analog column mux input.
4	I/O	I	P0[1]	Analog column mux input.
5	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
6	Power		Vss	Ground connection.
7	I/O		P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
8	Power		Vss	Ground connection.
9	I/O		P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
10	I/O		P1[2]	
11	I/O		P1[4]	Optional External Clock Input (EXTCLK).
12	I/O	I	P0[0]	Analog column mux input.
13	I/O	I	P0[2]	Analog column mux input.
14	I/O	I	P0[4]	Analog column mux input.
15	I/O	I	P0[6]	Analog column mux input.
16	Power		Vdd	Supply voltage.

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. 16-Pin EZ-Color Device



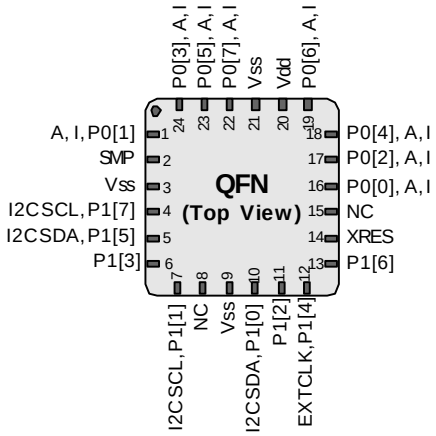
24-Pin Part Pinout

Table 5. 24-Pin Part Pinout (QFN)[2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	Analog column mux input.
2	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
3	Power		Vss	Ground connection.
4	I/O		P1[7]	I2C Serial Clock (SCL).
5	I/O		P1[5]	I2C Serial Data (SDA).
6	I/O		P1[3]	
7	I/O		P1[1]	I2C Serial Clock (SCL), ISSP-SCLK[1].
8			NC	No connection.
9	Power		Vss	Ground connection.
10	I/O		P1[0]	I2C Serial Data (SDA), ISSP-SDATA[1].
11	I/O		P1[2]	
12	I/O		P1[4]	Optional External Clock Input (EXTCLK).
13	I/O		P1[6]	
14	Input		XRES	Active high external reset with internal pull down.
15			NC	No connection.
16	I/O	I	P0[0]	Analog column mux input.
17	I/O	I	P0[2]	Analog column mux input.
18	I/O	I	P0[4]	Analog column mux input.
19	I/O	I	P0[6]	Analog column mux input.
20	Power		Vdd	Supply voltage.
21	Power		Vss	Ground connection.
22	I/O	I	P0[7]	Analog column mux input.
23	I/O	I	P0[5]	Analog column mux input.
24	I/O	I	P0[3]	Analog column mux input.

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. 24-Pin EZ-Color Device



Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset).
2. The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Register Reference

Register Conventions

This section lists the registers of the CY8CLED02 EZ-Color device.

The register conventions specific to this section are listed in the following table.

Table 6. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Table 7. Register Map Bank 0: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 7. Register Map Bank 0: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Register Map Bank 1

Table 8. Register Map Bank 1: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 8. Register Map Bank 1: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

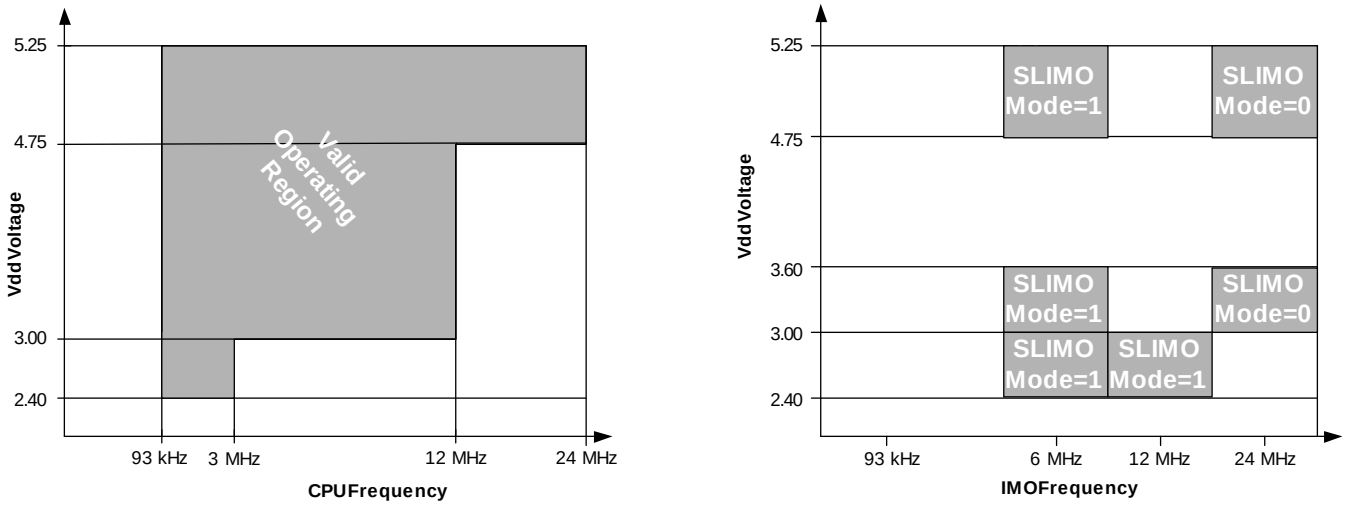
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED02 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/ez-color.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Refer to Table 22 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 6. Voltage versus CPU Frequency, and Voltage versus IMO Frequency



The following table lists the units of measure that are used in this data sheet.

Table 9. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	^{o}C	Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25^{o}C ± 25^{o}C. Extended duration storage temperatures above 65^{o}C will degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	^{o}C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up Current	–	–	200	mA	

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	^{o}C	
T_J	Junction Temperature	-40	–	+100	^{o}C	The temperature rise from ambient to junction is package specific. See “Thermal Impedances” on page 33. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 12. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	2.40	–	5.25	V	See DC POR and LVD specifications, Table 20 on page 20.
I_{DD}	Supply Current, IMO = 24 MHz	–	3	4	mA	Conditions are Vdd = 5.0V, 25°C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply Current, IMO = 6 MHz	–	1.2	2	mA	Conditions are Vdd = 3.3V, 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply Current, IMO = 6 MHz	–	1.1	1.5	mA	Conditions are Vdd = 2.55V, 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	Vdd = 2.55V, 0°C to 40°C.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	Vdd = 3.3V, -40°C ≤ T_A ≤ 85°C.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate Vdd. Vdd = 3.0V to 5.25V.
V_{REF27}	Reference Voltage (Bandgap)	1.16	1.30	1.330	V	Trimmed for appropriate Vdd. Vdd = 2.4V to 3.0V.
AGND	Analog Ground	V_{REF} - 0.003	V_{REF}	V_{REF} + 0.003	V	

DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 13. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget.
I_{OH}	High Level Source Current	10	–	–	mA	VOH = Vdd-1.0V. See the limitations of the total current in the Note for VOH.
I_{OL}	Low Level Sink Current	25	–	–	mA	VOL = 0.75V. See the limitations of the total current in the Note for VOL.
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 2.7V at 25°C and are for design guidance only.

Table 14. 2.7V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 0.4	–	–	V	IOH = 2.5 mA (6.25 typical), Vdd = 2.4 to 3.0V (16 mA maximum, 50 mA typical combined IOH budget).
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 10 mA, Vdd = 2.4 to 3.0V (90 mA maximum combined IOL budget).
I_{OH}	High Level Source Current	2.5	–	–	mA	VOH = Vdd-0.4V. See the limitations of the total current in the Note for VOH.
I_{OL}	Low Level Sink Current	10	–	–	mA	VOL = 0.75V. See the limitations of the total current in the Note for VOL.
V_{IL}	Input Low Level	–	–	0.75	V	Vdd = 2.4 to 3.0.
V_{IH}	Input High Level	2.0	–	–	V	Vdd = 2.4 to 3.0.
V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 15. 5V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd - 1	V	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	μA	

Table 16. 3.3V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.

Table 16. 3.3V DC Amplifier Specifications (continued)

V_{CMOA}	Common Mode Voltage Range	0	–	Vdd - 1	V	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	µA	

Table 17. 2.7V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd - 1	V	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	µA	

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 18. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Switch Mode Pump Specifications

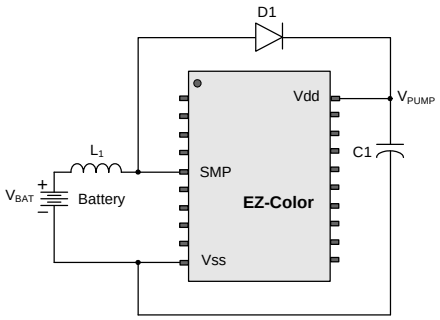
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 19. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP5V}	5V Output Voltage from Pump	4.75	5.0	5.25	V	Configuration of footnote.[3] Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V_{PUMP3V}	3.3V Output Voltage from Pump	3.00	3.25	3.60	V	Configuration of footnote.[3] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
V_{PUMP2V}	2.6V Output Voltage from Pump	2.45	2.55	2.80	V	Configuration of footnote.[3] Average, neglecting ripple. SMP trip voltage is set to 2.55V.
I_{PUMP}	Available Output Current V_{BAT} = 1.8V, V_{PUMP} = 5.0V V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.3V, V_{PUMP} = 2.55V	 5 8 8	 – – –	 – – –	 mA mA mA	Configuration of footnote.[3] SMP trip voltage is set to 5.0V. SMP trip voltage is set to 3.25V. SMP trip voltage is set to 2.55V.
V_{BAT5V}	Input Voltage Range from Battery	1.8	–	5.0	V	Configuration of footnote.[3] SMP trip voltage is set to 5.0V.
V_{BAT3V}	Input Voltage Range from Battery	1.0	–	3.3	V	Configuration of footnote.[3] SMP trip voltage is set to 3.25V.
V_{BAT2V}	Input Voltage Range from Battery	1.0	–	2.8	V	Configuration of footnote.[3] SMP trip voltage is set to 2.55V.
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.2	–	–	V	Configuration of footnote.[3] 0°C ≤ T_A ≤ 100. 1.25V at T_A = -40°C.
ΔV_{PUMP_Line}	Line Regulation (over Vi range)	–	5	–	$\%V_O$	Configuration of footnote.[3] V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 20 on page 20.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$	Configuration of footnote.[3] V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 20 on page 20.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on cap/load)	–	100	–	mVpp	Configuration of footnote.[3] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[3] Load is 5 mA. SMP trip voltage is set to 3.25V.
E_2	Efficiency	35	80	–	%	For I load = 1mA, V_{PUMP} = 2.55V, V_{BAT} = 1.3V, 10 µH inductor, 1 µF capacitor, and Schottky diode.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

Note
3. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 7 on page 20.

Figure 7. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 20. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b		2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[4]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[5]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	Vdd Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[6]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[7]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
4. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
5. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.
6. Always greater than 50 mV above V_{LVD0}.
7. Always greater than 50 mV above V_{LVD3}.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 21. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Notes

8. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 2.4V to 3.0V, 3.0V to 3.6V, and 4.75V to 5.25V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 22. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6[10,11,12]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[10,11,12]	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.093	24	24.6[10,11]	MHz	24 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.093	12	12.3[11,12]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.2[10,11,13]	MHz	Refer to the AC Digital Block Specifications below.
F_{BLK33}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	24.6[11,13]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	–	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the *PSoC Technical Reference Manual* for details on timing this.
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Jitter32k	32 kHz RMS Period Jitter	–	100	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–	ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[9,11]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Peak-to-Peak Period Jitter (IMO)	–	300		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	Power up from 0V. See the System Resets section of the *PSoC Technical Reference Manual*.

Table 23. 2.7V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	Internal Main Oscillator Frequency for 12 MHz	11.5	12	12.7[10,11,12]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[10,11,12]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.093	3	3.15[10,11]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC Block Frequency (2.7V Nominal)	0	12	12.5[10,11,12]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	–	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the *PSoC Technical Reference Manual* for details on timing this.
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Jitter32k	32 kHz RMS Period Jitter	–	150	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–	ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	Power up from 0V. See the System Resets section of the *PSoC Technical Reference Manual*.

Figure 8. 24 MHz Period Jitter (IMO) Timing Diagram

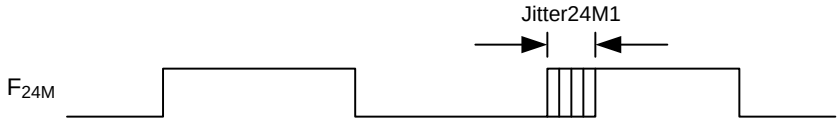
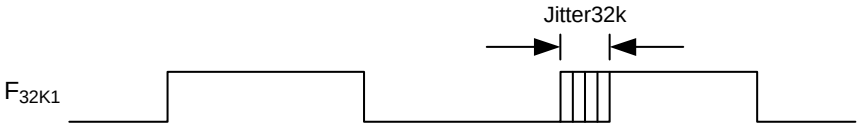


Figure 9. 32 kHz Period Jitter (ILO) Timing Diagram



Notes
10. 4.75V < Vdd < 5.25V.
11. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
12. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
13. See the individual user module data sheets for information on maximum frequencies for user modules.

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

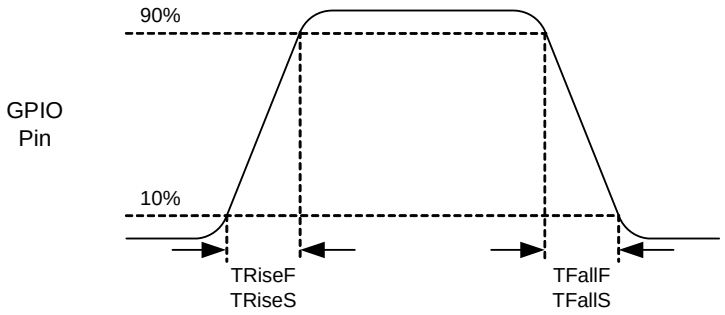
Table 24. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Table 25. 2.7V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%

Figure 10. GPIO Timing Diagram



AC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 26. 5V and 3.3V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP1}	Comparator Mode Response Time, 50 mVpp Signal Centered on Reference			100	ns	
T_{COMP2}	Comparator Mode Response Time, 2.5V Input, 0.5V Overdrive			300	ns	

Table 27. 2.7V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP1}	Comparator Mode Response Time, 50 mVpp Signal Centered on Ref			600	ns	
T_{COMP2}	Comparator Mode Response Time, 1.5V Input, 0.5V Overdrive			300	ns	

AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 28. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 29. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24.6	MHz	3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50[14]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With or Without Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50	–	–	ns	
	Disable Mode	50	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

Note
14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 30. 2.7V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			12.7	MHz	2.4V < Vdd < 3.0V.
Timer	Capture Pulse Width	100[15]	–	–	ns	
	Maximum Frequency, With or Without Capture	–	–	12.7	MHz	
Counter	Enable Pulse Width	100	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	12.7	MHz	
	Maximum Frequency, Enable Input	–	–	12.7	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	100	–	–	ns	
	Disable Mode	100	–	–	ns	
	Maximum Frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
SPIM	Maximum Input Clock Frequency	–	–	6.35	MHz	Maximum data rate at 3.17 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	100	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 31. 5V AC External Clock SpecificationsC

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Note
15. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Table 32. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 33. 2.7V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	6.06	MHz	Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	12.12	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	83.4	–	5300	ns	
–	Low Period with CPU Clock divide by 1	83.4	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 34. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	80	–	ms	
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	180[16]	ms	0°C ≤ T_J ≤ 100°C
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	360[16]	ms	-40°C ≤ T_J ≤ 0°C

AC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 35. AC Characteristics of the I2C SDA and SCL Pins for Vcc . 3.0V

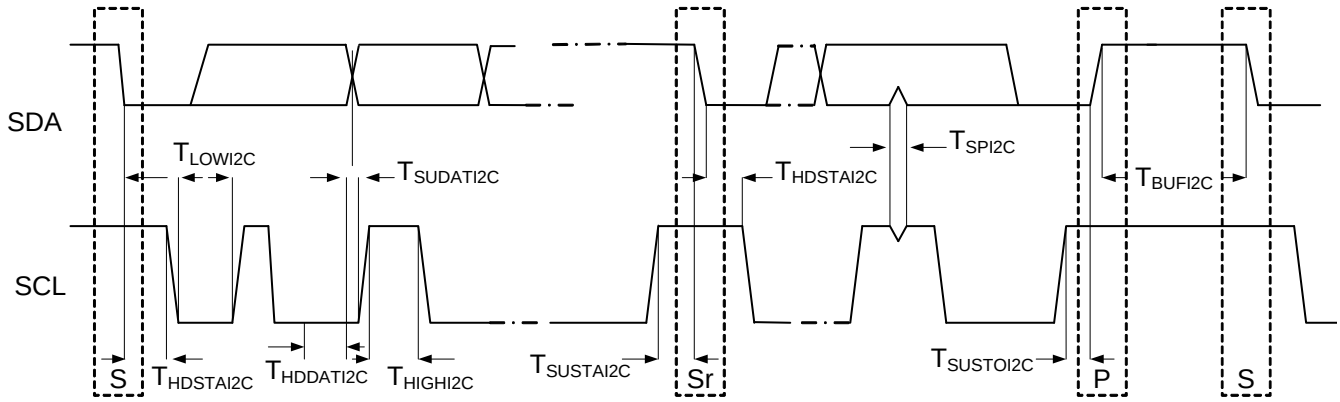
Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[17]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Note
16. For the full industrial range, the user must employ a Temperature Sensor User Module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

Table 36. 2.7V AC Characteristics of the I2C SDA and SCL Pins (Fast-Mode not Supported)

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	–	–	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	–	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	–	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	–	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	–	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	–	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	–	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns	

Figure 11. Definition for Timing for Fast-/Standard-Mode on the I^2C Bus



Note

17. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

Packaging Dimensions

This section illustrates the packaging specifications for the CY8CLED02 EZ-Color device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 12. 8-Pin (150-Mil) SOIC

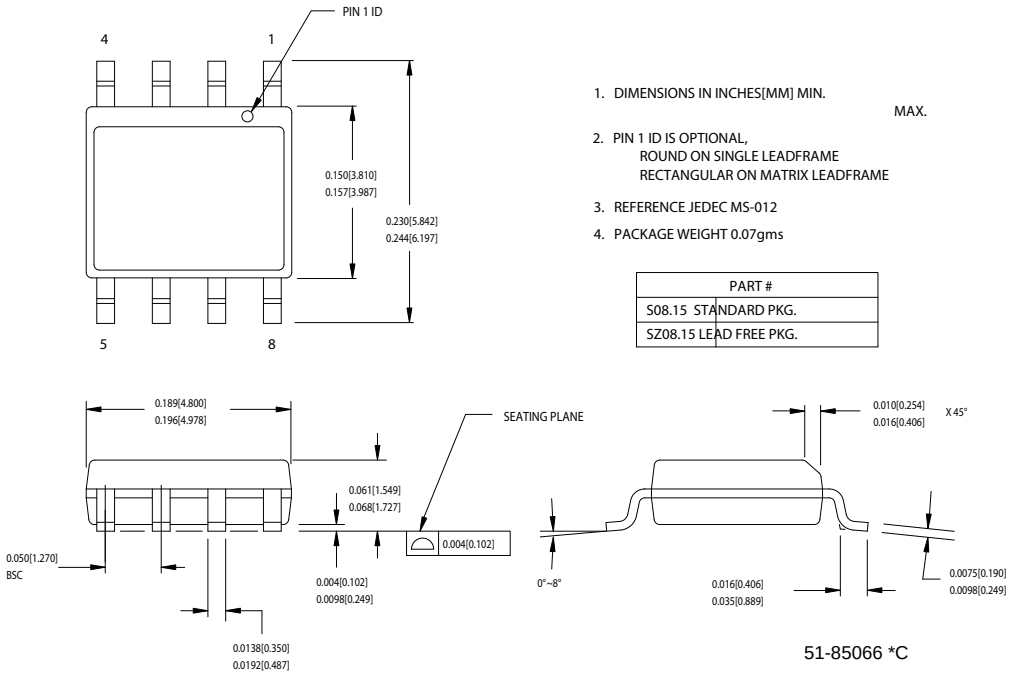
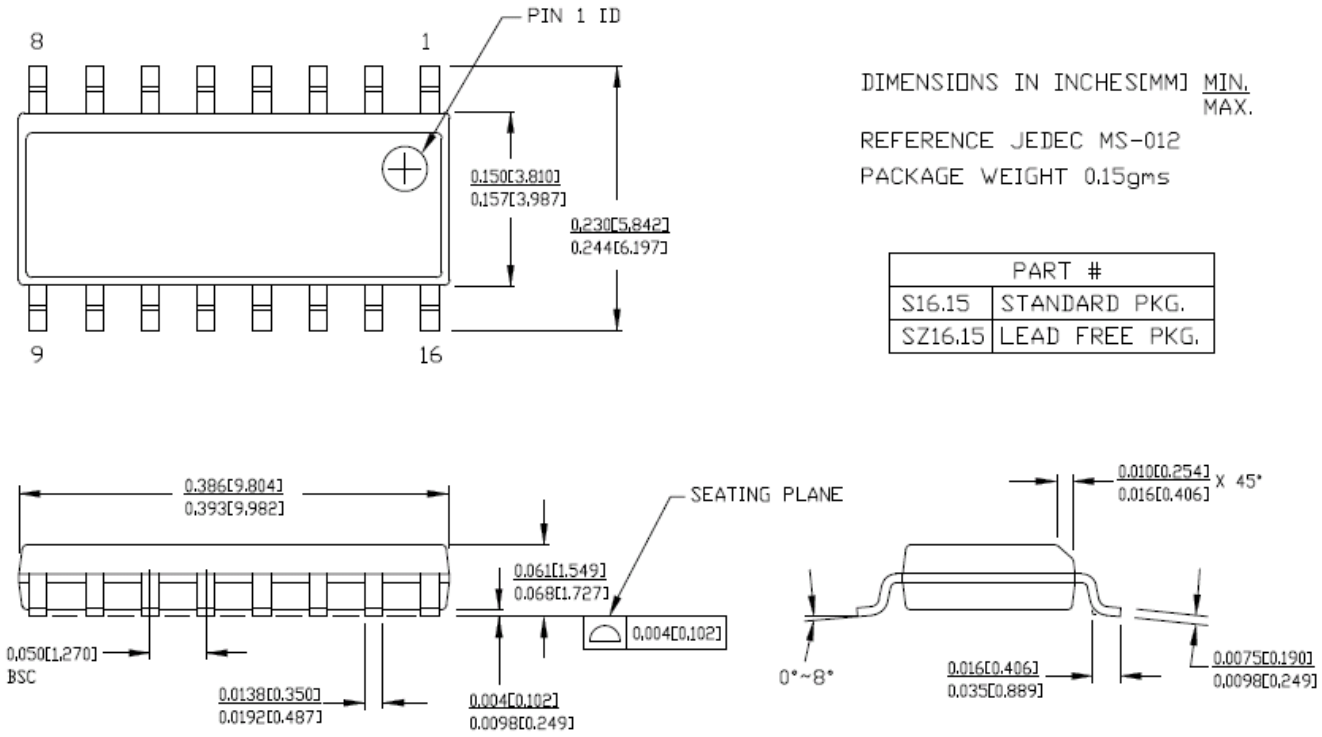
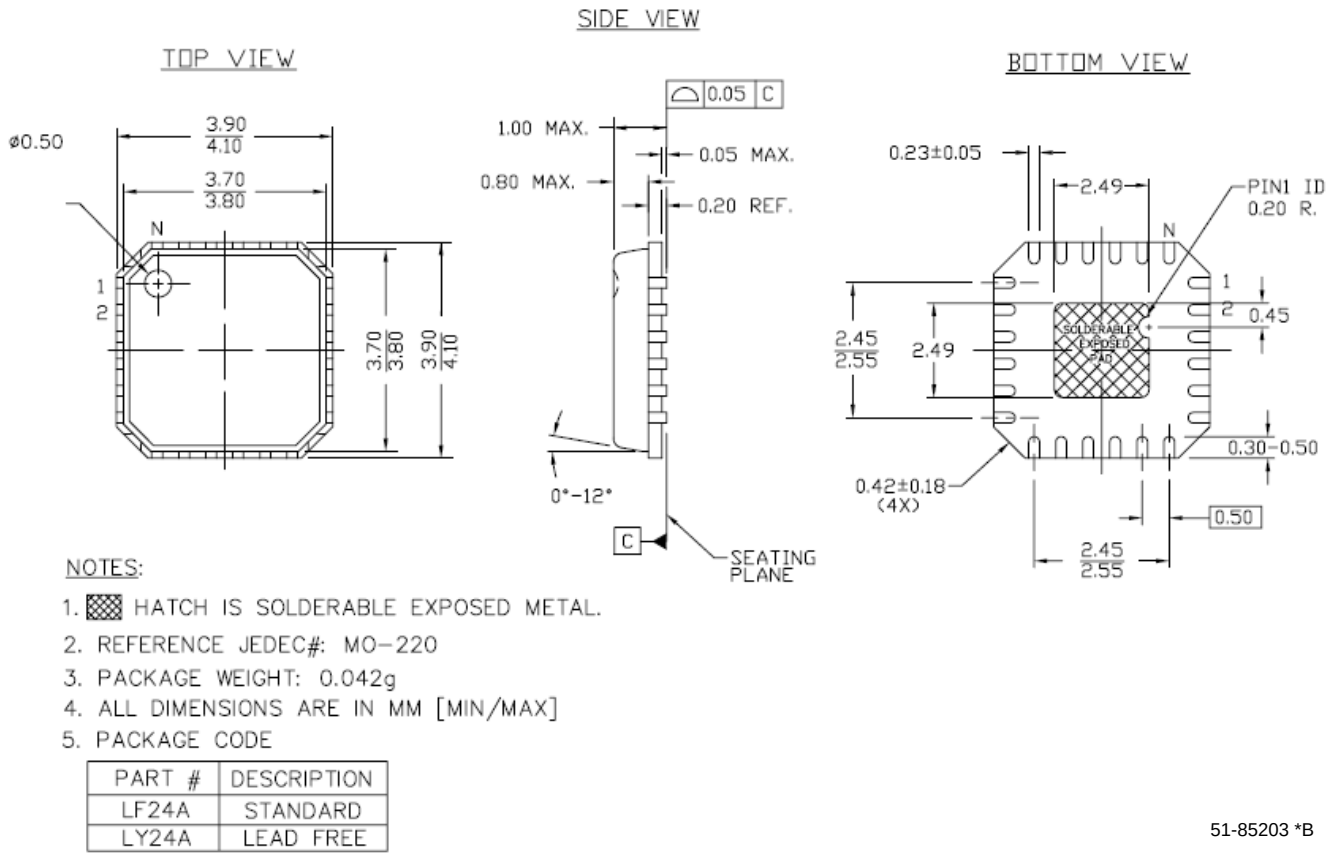


Figure 13. 16-Pin (150-Mil) SOIC



51-85068 *C

Figure 14. 24-Pin (4x4) QFN



Important Note For information about the preferred dimensions for mounting the QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power 24-, 32-, and 48-pin QFN EZ-Color devices.

Thermal Impedances

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [18]
8 SOIC	186 °C/W
16 SOIC	125 °C/W
24 QFN[19]	40 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 38. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[20]	Maximum Peak Temperature
8 SOIC	240°C	260°C
16 SOIC	240°C	260°C
24 QFN	240°C	260°C

Notes
18. $T_J = T_A + POWER \times \theta_{JA}$
19. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
20. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications

Development Tool Selection

This section presents the development tools available for all current PSoC based devices including the CY8CLED02 EZ-Color family.

Software Tools

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free ofcharge at http://www.cypress.com/psocprogrammer.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC based devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the device on the target board and performs full speed (24 MHz) operation.

I2C to USB Bridge

The I2C to USB Bridge is a quick and easy link from any design or application's I2C bus to a PC via USB for design testing, debugging and communication.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free ofcharge at http://www.cypress.com/psocprogrammer.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3261A-RGB EZ-Color RGB Kit

The CY3261A-RGB board is a preprogrammed HB LED color mix board with seven pre-set colors using the CY8CLED16 EZ-Color HB LED Controller. The board is accompanied by a CD containing the color selector software application, PSoC Designer, PSoC Programmer, and a suite of documents, schematics, and firmware examples. The color selector software application can be installed on a host PC and is used to control the EZ-Color HB LED controller using the included USB cable. The application enables you to select colors via a CIE 1931 chart or by entering coordinates. The kit includes:

- Training Board (CY8CLED16)
- One mini-A to mini-B USB Cable
- PSoC Designer CD-ROM
- Design Files and Application Installation CD-ROM

To program and tune this kit via PSoC Designer you must use a Mini Programmer Unit (CY3217 Kit) and a CY3240-I2CUSB kit.

CY3263-ColorLock Evaluation Kit

The CY3263-ColorLock evaluation board demonstrates the ability of the EZ-Color device to use real-time optical feedback to control three primary, high brightness LEDs and create accurate, mixed-color output. The kit includes:

- CY3263-ColorLock Evaluation Board
- Tools CD, which includes:
  - PSoC Programmer
  - .NET Framework 2.0 (for Windows 2000 and Windows XP)
  - PSoC Designer
  - ColorLock Express Pack
  - CY3263-ColorLock EZ-Color Kit CD
  - ColorLock Monitor Application
  - Kit Documents (Quick Start, Kit Guide, Release Note, Application Note, Data Sheets, Schematics, and Layouts)
  - Firmware
- Retractable USB Cable (A to Mini-B)
- PSoC MiniProg Programmer
- Power Supply Adapter

CY3265-RGB EZ-Color Evaluation Kit

The CY3265-RGB evaluation board demonstrates the ability of the EZ-Color device to use real-time temperature feedback to control three primary, high brightness LEDs and create accurate, mixed-color output. There are three variations of the kit available, depending on the LED manufacturer of the LEDs on the board: CY3265C-RGB (Cree LEDs), CY3265N-RGB (Nichia LEDs), or CY3265O-RGB (OSRAM LEDs). The kit includes:

- CY3265C-RGB Evaluation Board
- Tools CD, which includes:
  - PSoC Programmer
  - PSoC Designer
  - .NET Framework 2.0 (Windows XP 32 bit)
- Kit Documents (Quick Start, Kit Guide, Release Note, Application Note, Data Sheets, Schematics, and Layouts) Firmware
- Blue PCA Enclosure/Case
- 12V 1A Power Supply
- Retractable USB Cable (A to Mini-B)
- PSoC MiniProg Programmer
- Quick Start Guide

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC based devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 39. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[21]	Foot Kit[22]	Adapter[23]
CY8CLED02-8SXI	8 SOIC	CY3250-LED02	CY3250-8SOIC-FK	Adapters can be found at http://www.emulation.com.
CY8CLED02-16SXI	16 SOIC	CY3250-LED02	CY3250-16SOIC-FK	
CY8CLED02-24LFXI	24 QFN	CY3250-LED02QFN	CY3250-24QFN-FK	

Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Design Support >> Development Kits/Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323”. Table 40 on page 37 lists the CY8CLED08 EZ-Color devices’ key package features and ordering codes.

Notes
21. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
22. Foot kit includes surface mount feet that can be soldered to the target PCB.
23. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

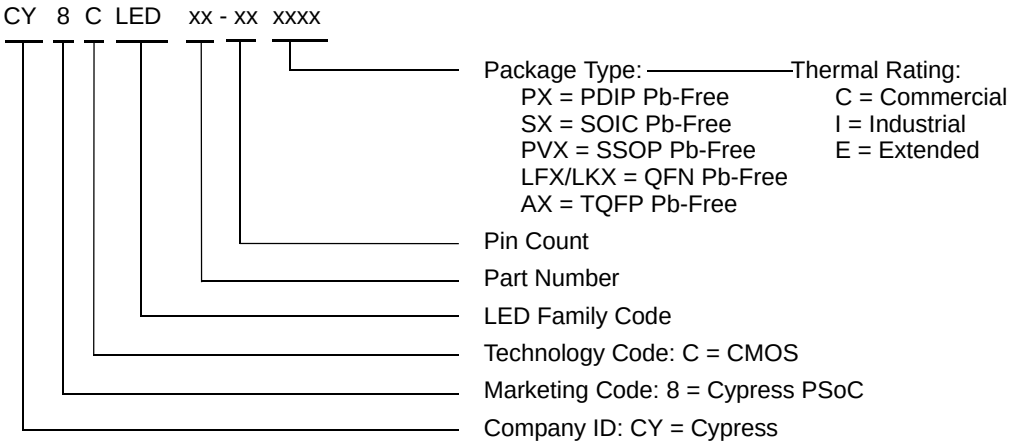
Key Device Features

The following table lists the CY8CLED02 EZ-Color devices' key package features and ordering codes.

Table 40. Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (150-Mil) SOIC	CY8CLED02-8SXI	4K	256	No	-40°C to +85°C	4	4	6	4	0	No
8 Pin (150-Mil) SOIC (Tape and Reel)	CY8CLED02-8SXIT	4K	256	No	-40°C to +85°C	4	4	6	4	0	No
16 Pin (150-Mil) SOIC	CY8CLED02-16SXI	4K	256	Yes	-40°C to +85°C	4	4	12	8	0	No
16 Pin (150-Mil) SOIC (Tape and Reel)	CY8CLED02-16SXIT	4K	256	Yes	-40°C to +85°C	4	4	12	8	0	No
24 Pin (4x4) QFN	CY8CLED02-24LFXI	4K	256	Yes	-40°C to +85°C	4	4	16	8	0	Yes
24 Pin (4x4) QFN (Tape and Reel)	CY8CLED02-24LFXIT	4K	256	Yes	-40°C to +85°C	4	4	16	8	0	Yes

Ordering Code Definitions



Document History Page

Document Title: CY8CLED02 EZ-Color™ HB LED Controller Document Number: 001-13704				
Revision	**ECN #**	**Submission Date**	**Origin of Change**	**Description of Change**
**	1383443	See ECN	SFVTMP3/AESA	New document
*A	2732564	07/09/2009	CGX	Converted from Preliminary to Final
*B	2794355	10/28/2009	XBM	Added "Contents" on page 2 Updated "Development Tools" on page 6. Corrected FCPU1 and FCPU2 parameters in Table 22, "5V and 3.3V AC Chip-Level Specifications," on page 22 and Table 23, "2.7V AC Chip-Level Specifications," on page 23
*C	2850593	01/14/2010	FRE	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 and TWRITE specifications. Replaced TRAMP (time) specification with SRPOWER_UP (slew rate) specification. Added note to Flash Endurance specification. Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. Corrected the Pod Kit part numbers. Updated Development Tool Selection. Updated copyright and Sales, Solutions, and Legal Information URLs. Updated 24-Pin QFN package diagram.

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