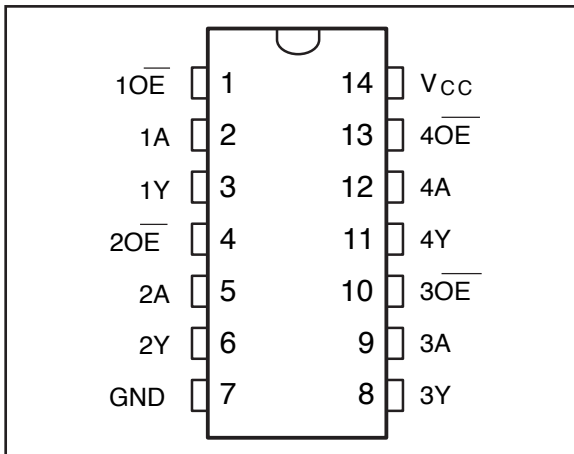


74 Series GHz Logic

FEATURES:	DESCRIPTION:
<ul style="list-style-type: none"> . Patented technology . Operating frequency up to 1.125GHz with 2pf load . Operating frequency up to 550MHz with 5pf load . Operating frequency up to 300MHz with 15pf load . VCC Operates from 1.65V to 3.6V . Propagation delay < 1.5ns max with 15pf load . Low input capacitance: 4pf typical . Available in 14pin 150mil wide SOIC package 	<p>Potato Semiconductor's PO74G125A is designed for world top performance using submicron CMOS technology to achieve 1.125GHz TTL /CMOS output frequency with less than 1.5ns propagation delay. This quadruple bus buffer gate is designed for 1.65-V to 3.6-V VCC operation.</p> <p>The PO74G125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.</p> <p>Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.</p>

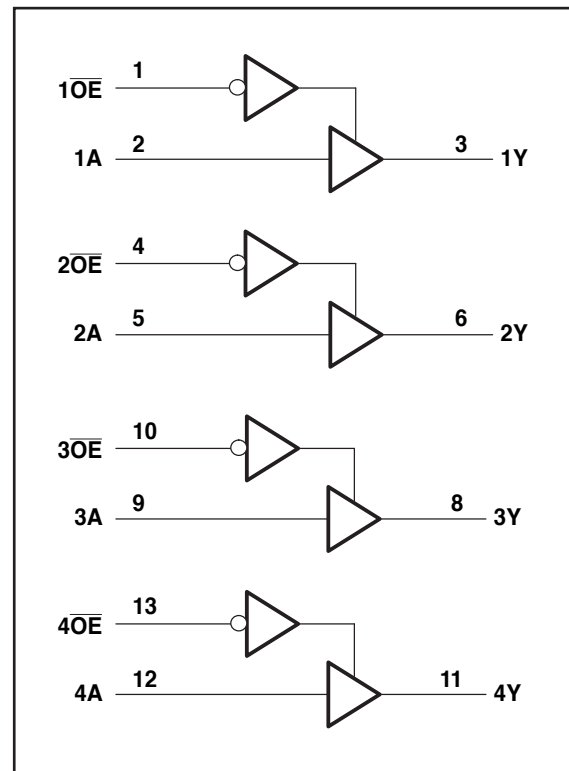
Pin Configuration



Pin Description

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

Logic Block Diagram



74 Series GHz Logic

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to V _{cc} +0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	V _{cc} =3V Vin=V _{IH} or V _{IL} , I _{OH} = -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	V _{cc} =3V Vin=V _{IH} or V _{IL} , I _{OH} =12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	V _{cc} = 3.6V and Vin = 5.5V	-	-	50	uA
I_{IL}	Input Low current	V _{cc} = 3.6V and Vin = 0V	-	-	-50	uA
V_{IK}	Clamp diode voltage	V _{cc} = Min. And I _{IN} = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{cc} = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. V_{OH} = V_{cc} - 0.6V at rated current

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Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{ccQ}	Quiescent Power Supply Current	V _{cc} =Max, V _{in} =V _{cc} or GND	-	0.1	30	uA
ΔI_{cc}	Power Supply Current per Input High	V _{cc} =Max, V _{in} = V _{cc} -0.6V	-	50	300	uA

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{cc} = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = V_{cc} – 0.6V at rated current

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Unit
C_{in}	Input Capacitance	V _{in} = 0V	4	pF
C_{out}	Output Capacitance	V _{out} = 0V	6	pF

Notes:

- 1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

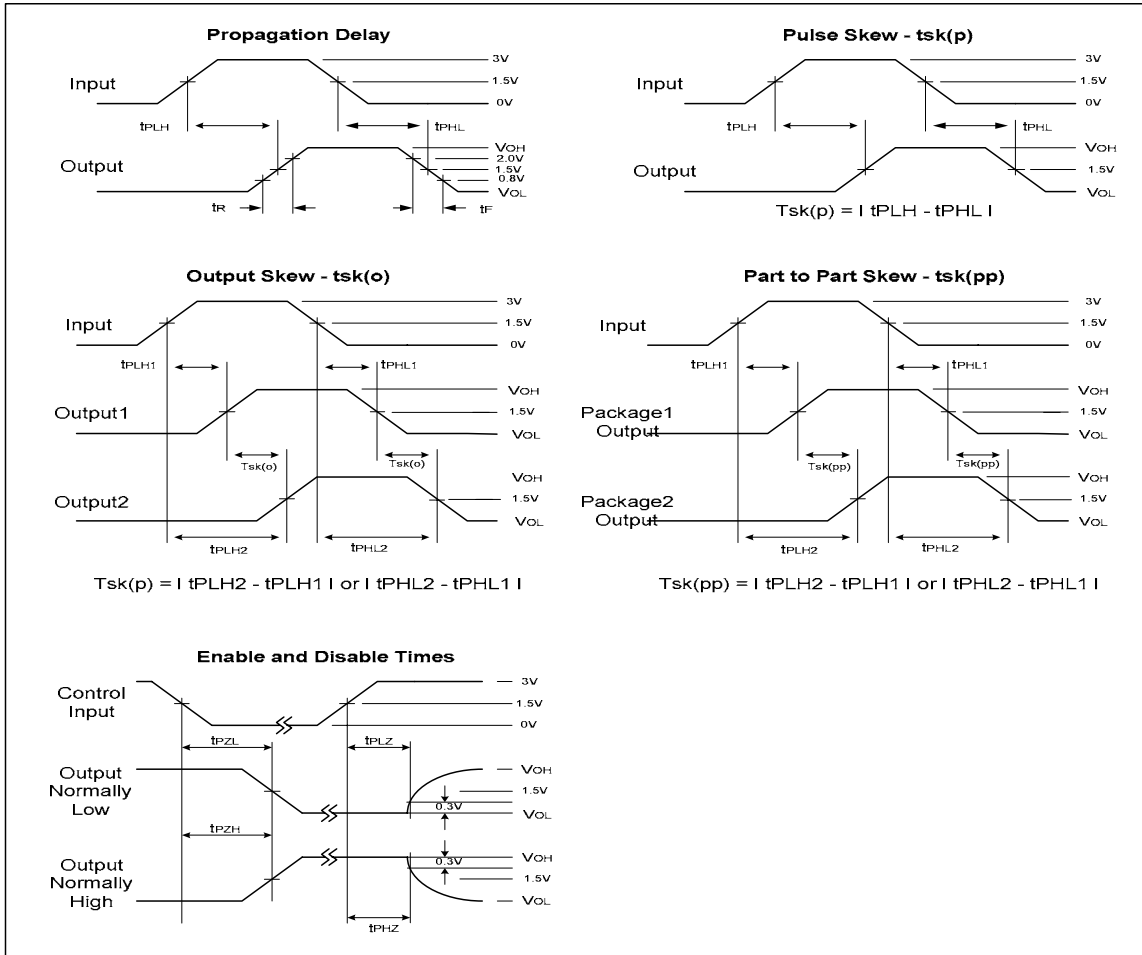
Symbol	Description	Test Conditions (1)	Max	Unit
t_{PLH}	Propagation Delay A to Y	CL = 15pF	1.5	ns
t_{PHL}	Propagation Delay A to Y	CL = 15pF	1.5	ns
t_{PZH} or t_{PZL}	Output Enable Time	CL = 15pF	2.5	ns
t_{PHZ} or t_{PLZ}	Output Disable Time	CL = 15pF	2.5	ns
t_r/t_f	Rise/Fall Time	0.8V – 2.0V	0.8	ns
f_{max}	Input Frequency	CL =15pF	300	MHz
f_{max}	Input Frequency	CL = 5pF	550	MHz
f_{max}	Input Frequency	CL = 2pF	1125	MHz

Notes:

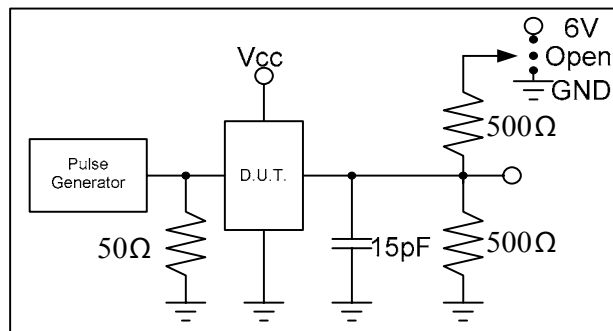
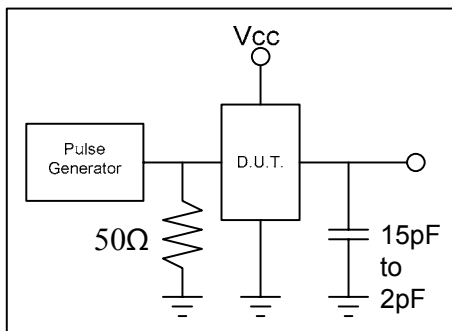
1. See test circuits and waveforms.
2. t_{PLH}, t_{PHL}, t_{sk(p)}, and t_{sk(o)} are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

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Test Waveforms

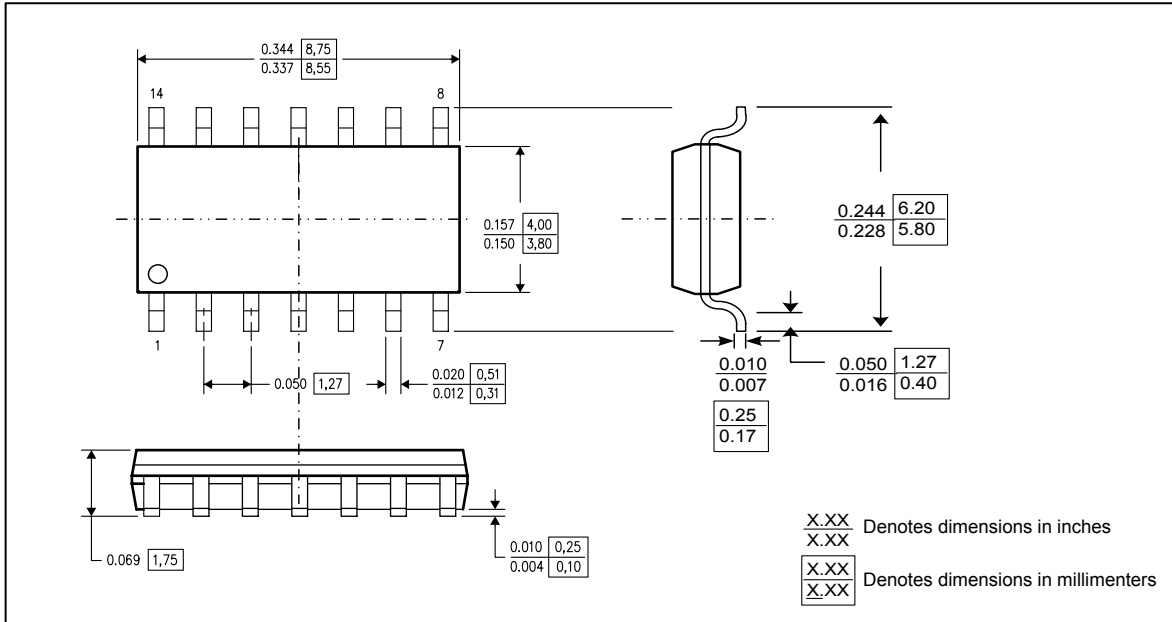


Test Circuit



74 Series GHz Logic

Packaging Mechanical Drawing: 14 pin 150mil SOIC



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Ordering Information

Ordering Code	Package			Top-Marking	T _A
PO74G125ASU	14pin SOIC	Tube	Pb-free & Green	PO74G125AS	-40°C to 85°C
PO74G125ASR	14pin SOIC	Tape and reel	Pb-free & Green	PO74G125AS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
S	SOIC 14	16	8	Top Left Corner	39 (12")	3000	64 (20")	55