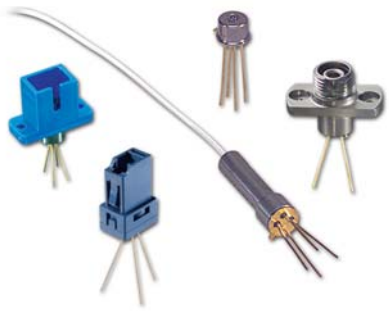
Access PIN-TIA Receivers for 155 Mb/s and 622 Mb/s

EDR 51xx Series



Applications

- Single mode 155 Mb/s (EDR 512x) and 622 Mb/s (EDR 515x) ATM receivers
- Campus network backbone
  - Add/drop multiplexers
  - Digital loop carriers
  - Digital crossconnects
  - Optical networking
- Enterprise network backbone

Key Features

- **Electro-optical**
  - **InGaAs PIN photodiode with silicon transimpedance amplifier**
  - **Operate on single supply**
    - **EDR 512x (5 V)**
    - **EDR 515x (3.3 V or 5 V)**
  - **Three standard pin-out configurations**
    - **EDR 51xB - single-ended output**
    - **EDR 51xC - single-ended output with photodiode access**
    - **EDR 51xD - differential output**
  - **Cost effective in receiver designs where sensitivity is limited by the post-amplifier**
  - **Shielded pre-amplifier makes it immune to crosstalk with transmitter or to other EMI**
  - **-40 to +85°C operating range**
- **Packaging**
  - **Integrated 4-pin coaxial package**
  - **Connector receptacle (panel or PCB mount) and fiber pigtailed versions**
  - **Case grounded versions**

The EDR 51xx Series incorporates a 75 µm InGaAs PIN photodetector coupled with a low cost BiCMOS transimpedance amplifier (TIA) designed to operate at 155 Mb/s (EDR 512x) or 622 Mb/s (EDR 515x). The PIN transduces optical power into current with high efficiency. The TIA converts the current signal into a voltage signal with a very low input noise current contribution. The EDR 512x TIA also integrates an automatic gain control (AGC) circuit which decreases the light to voltage conversion factor when the average incident optical power is relatively high.

The EDR 51xx Series are assembled in rugged coaxial packages. They are available with a connector receptacle or as a single mode fiber pigtail. Standard choices for connector receptacles are LC, SC and FC. In addition, the EDR 51xx Series are available in several standard pin-out configurations. The EDR 51xB is the simplest configuration and provides a single ended output. The EDR 51xC provides access to the photodiode current for those customers who need to design an alarm circuit. The EDR 51xD provides a differential output for higher gain performance without sacrifice to sensitivity and bandwidth.

Typical Applications

The EDR 51xx Series are designed for many applications, including single mode 155 Mb/s (EDR 512x) and 622 Mb/s (EDR 515x) ATM receivers. The EDR 51xx Series exceed Long Reach OC-3 (EDR 512x) and OC-12 (EDR 515x) SONET receiver specifications and are ideal for transceiver designs or board level discrete designs. Applications include receivers for digital cross connects, digital loop carriers, add/drop multiplexers, optical network units and switches and routers for LAN and WAN backbones.

External Circuitry

When designing the EDR 51xx Series into an optical receiver, standard high speed printed circuit board design practices should be observed. For example, bypassing of the power supply is recommended so as to reduce noise that appears at the output of the PIN-TIA.

If signal traces are relatively long, use impedance matching techniques to maximize power transfer from the PIN-TIA to its load: for microstrip design, assume 70 ohms (EDR 512x) and 60 ohms (EDR 515x) as the output impedance for the PIN-TIA. Note as well that the output of the PIN-TIA is DC-coupled. Since most applications require AC-coupled stages, a high-Q RF chip capacitor should be placed on the output of the module. To eliminate oscillations, the PIN-TIA should be mounted on a circuit board with a large, low impedance ground plane. All the PIN-TIA leads should be made as short as possible in order to reduce excess inductances. As a general rule, receiver bandwidth requirements need only be greater than about 1/3 of the bit rate at which they are intended to operate. A receiver for a 155 Mb/s system must have a bandwidth greater than 110 MHz. A receiver for a 622 Mb/s system must have a bandwidth greater than 415 MHz. On the other hand, any frequency component above 110 MHz for 155 Mb/s systems or above 415 MHz for 622 Mb/s systems contributes excess noise to the output. The excess noise needlessly reduces the sensitivity of the receiver. The receiver designer may therefore improve the PIN-TIA sensitivity by placing a low pass noise filter on the output.

Performance Highlights

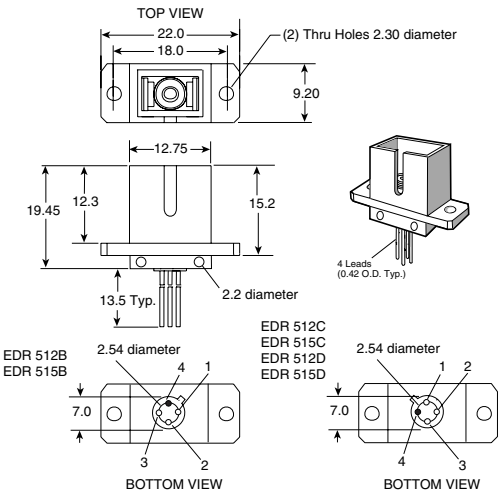
The EDR 51x Series offer a sensitivity of better than -36 dBm (EDR 512x) or -30 dBm (EDR 515x) with appropriate filtering and a minimum overload of 0 dBm (EDR 512x) or -7 dBm (EDR 515x). This large dynamic range makes these products ideal for both long and short range applications. A time constant of 4 milliseconds makes the AGC circuit of the EDR 512x models very stable, even during reception of the longest streams of high or low logic levels. The EDR 51x Series operate over -40 to +85°C.

The EDR 51x Series provide significant benefits over hybrid designs and 14-pin receivers. Integration of the TIA with the PIN detector onto the TO-46 header reduces parasitic capacitances and lead inductances. The TO-52 cap hermetically seals the hybrid and provides EMI shielding especially from the transmitter circuit. These advantages improve sensitivity over designs that place the amplifier outside the capsule and away from the detector. The EDR 51x Series, which have four pins, are advantageous over 14-pin receivers because they require less board space and fewer electrical connections. In addition, the EDR 51xx Series operate from a single power supply, even in the pin-out configuration which provides photodiode current monitoring. The smaller form factor and the need for a single power supply make the EDR 51x Series a less expensive, high performance alternative to other kinds of optical receivers.

Dimensions Diagram

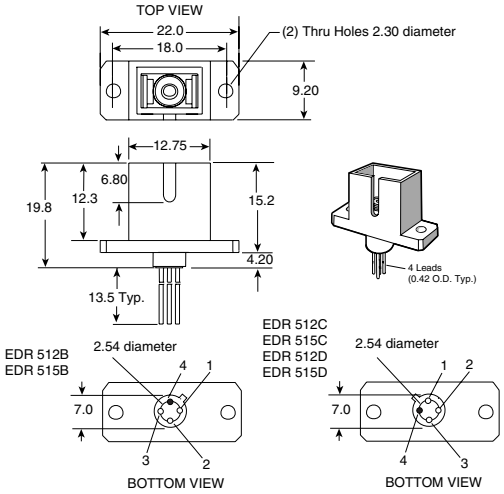
(Specifications in mm unless otherwise noted.)

EDR 51xx RSC-DM



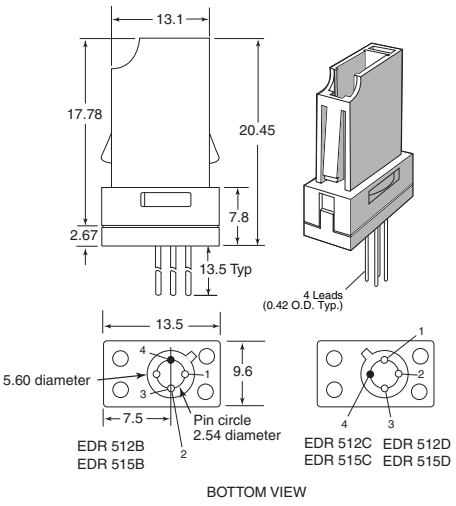
Note: Critical dimensions meet NTT specifications.
Other dimensions subject to revision.

EDR 51xx RSC-FM

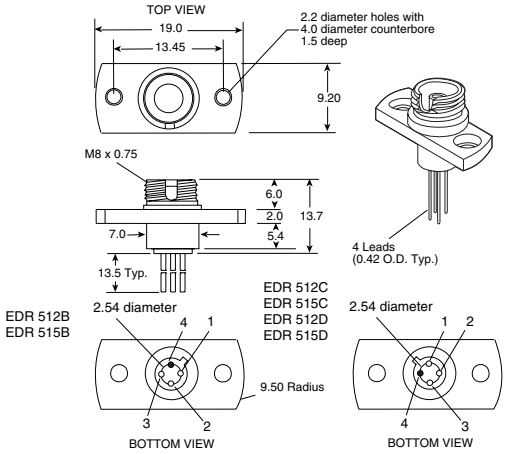


Note: Critical dimensions meet NTT specifications.
Other dimensions subject to revision.

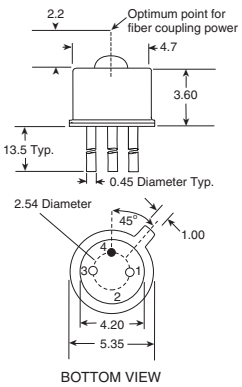
EDR 51xx RLC



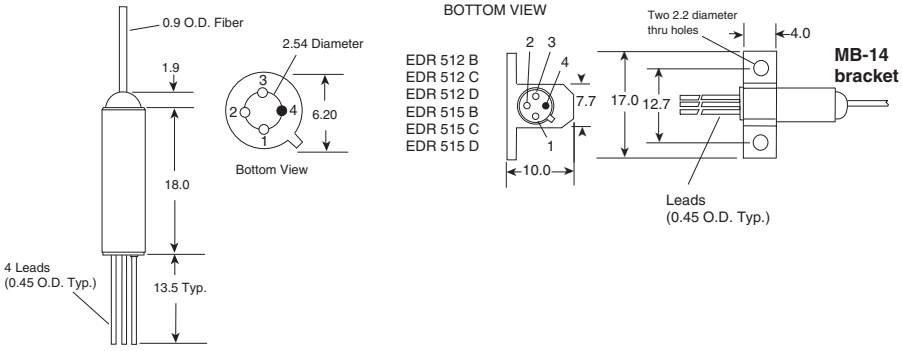
EDR 51xx RFC2



EDR 51xx TL



EDR 51xx FJS with Bracket Option



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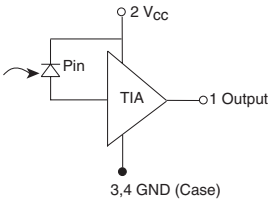
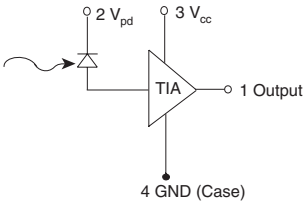
Electrical Schematics

EDR 512B, EDR 515B

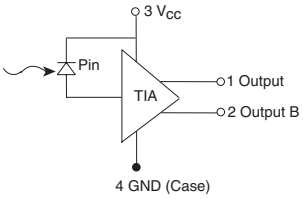


EDR 512C, EDR 515C



Access to photodiode current is provided.

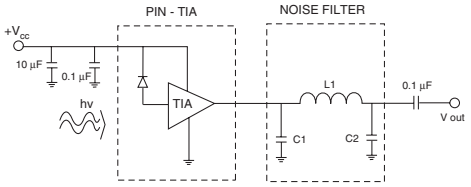
EDR 512D, EDR 515D



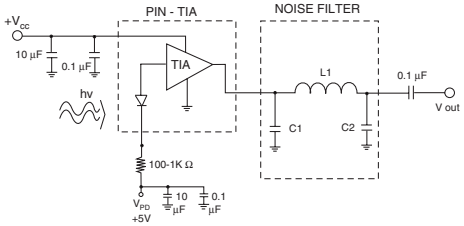
Differential output is provided.

Typical Low Pass Noise Filter Design for 155 Mb/s and 622 Mb/s

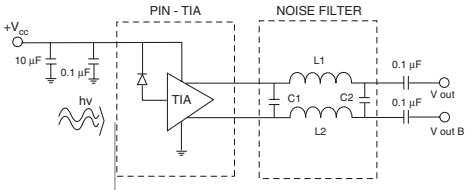
EDR 512B, EDR 515B



EDR 512C, EDR 515C



EDR 512D, EDR 515D



Model	L1	L2	C1	C2
EDR 512B	150 nH	-	27 pF	27 pF
EDR 512C	150 nH	-	27 pF	27 pF
EDR 512D	120 nH	120 nH	18 pF	18 pF
EDR 515B	33 nH	-	10 pF	10 pF
EDR 515C	33 nH	-	10 pF	10 pF
EDR 515D	30 nH	30 nH	5.6 pF	5.6 pF

EDR 512x Specifications

(V_{CC} = +5 V, T_A = 25 °C, R_L = 50 Ω (AC coupled), λ = 1300 nm. All specifications without connector.)

Parameter		EDR 512B	EDR 512C	EDR 512D
Gain[1]	Minimum	15 V/mW	15 V/mW	25 V/mW
	Typical	20 V/mW	20 V/mW	35 V/mW
Bandwidth	Minimum	110 MHz	110 MHz	110 MHz
	Typical	200 MHz	200 MHz	200 MHz
Sensitivity[2]	Typical	-38.0 dBm	-38.0 dBm	-38.5 dBm
	Maximum	-36.0 dBm	-36.0 dBm	-36.5 dBm
Overload	Minimum	0 dBm	0 dBm	0 dBm
	Typical	2 dBm	2 dBm	2 dBm
Output resistance	Typical	70 Ω	70 Ω	70 Ω
Maximum output voltage	Typical	400 mV_{pk-pk}	400 mV_{pk-pk}	800 mV_{pk-pk}
AGC time constant	Typical	4000 µs	4000 µs	4000 µs
AGC threshold	Typical	2 µW	2 µW	2 µW

1. Measured at 100 MHz.
2. BER of 1E-10, 120 MHz noise filter.

EDR 515x Specifications

(V_{CC} = +3.3 V, T_A = 25 °C, R_L = 50 Ω (AC coupled), λ = 1300 nm. All specifications without connector.)

Parameter		EDR 515B	EDR 515C	EDR 515D
Gain[1]	Minimum	1.7 V/mW	1.7 V/mW	3.0 V/mW
	Typical	2.2 V/mW	2.2 V/mW	4.0 V/mW
Bandwidth	Minimum	415 MHz	415 MHz	415 MHz
	Typical	500 MHz	500 MHz	500 MHz
Sensitivity[2]	Typical	-31.5 dBm	-31.5 dBm	-32.5 dBm
	Maximum	-30.0 dBm	-30.0 dBm	-31.0 dBm
Overload	Minimum	-7.0 dBm	-7.0 dBm	-7.0 dBm
	Maximum	-4.0 dBm	-4.0 dBm	-4.0 dBm
Output resistance	Minimum	45 Ω	45 Ω	45 Ω
	Typical	60 Ω	60 Ω	60 Ω
	Maximum	75 Ω	75 Ω	75 Ω
Maximum output voltage	Maximum	500 mV_{pk-pk}	500 mV_{pk-pk}	950 mV_{pk-pk}

1. Measured at 300 MHz.
2. BER of 1E-10, 415 MHz noise filter.

EDR 512x DC Electrical Characteristics and Maximum Ratings

Parameter	Minimum	Typical	Maximum
Supply voltage (V_{CC})	4.5 V	5.0 V	5.5 V
Output offset voltage	2.9 V	3.2 V	3.5 V
Diff. output offset voltage[1]	-	80 mV	-
Supply current (I_{CC})	-	25 mA	50 mA
Dark current[2]	-	-	1 nA
Optical input power	-	-	5.0 mW
Operating temperature	-40 °C	-	85 °C
Storage temperature	-40 °C	-	85 °C
Photodiode voltage (V_{pd})[2]	2 V	-	25 V

1. Applies to EDR 512D only.
2. Applies to EDR 512C only.

EDR 515x DC Electrical Characteristics and Maximum Ratings

Parameter	Minimum	Typical	Maximum
Supply voltage (V_{CC})	3.0 V	3.3/5.0 V	5.25 V
Output offset voltage	-	2.0/3.7 V	-
Diff. output offset voltage[1]	-	7.0 mV	-
Supply current (I_{CC})	12 mA	25/35 mA	50 mA
Dark current[2]	-	-	1.0 nA
Optical input power	-	-	5.0 mW
Operating temperature	-40 °C	-	85 °C
Storage temperature	-40 °C	-	85 °C
Photodiode voltage (V_{pd})[2]	2 V	-	25 V

1. Applies to EDR 515D only.
2. Applies to EDR 515C only.

Ordering Information

For more information on this or other products and their availability, please contact your local JDSU account manager or JDSU directly at 1-800-498-JDSU (5378) in North America and +800-5378-JDSU worldwide or via e-mail at customer.service@jdsu.com.

Sample: EDR 512C FJS LC

EDR 51 □ □ + □ + □ + □

Code	Speed
2	155 Mb/s
5	622 Mb/s

Code	PIN-TIA
B	Single-ended output with case connected to ground
C	Access to photodiode current with case connected to ground
D	With differential output voltage

Code	Package
TL	Transistor ouline with lensed cap
FJS	Single mode (900 µm) fiber jacket
RLC	LC receptacle
RFC2	FC receptacle with 2-hole flange
RSC-DM	SC receptacle, dual-mount (panel & board)
RSC-FM	SC receptacle, front-mount (panel only)

Code	Connector (FJS only)
LC	LC connector
FC/SPC	FC/SPC connector
SC/SPC	SC/SPC connector

Code	Bracket (FJS only)
0	No bracket
MB14	MB-14 bracket

Precautions for Use

ESD protection is imperative. Use of grounding straps, anti-static mats, and other standard ESD protective equipment is required when handling or testing an InGaAs PIN or any other junction photodiode. Fiber pigtails should be handled with less than 10 N pull and with bending radius greater than 1 inch. Soldering temperature of the leads should not exceed 260 °C for more than 10 seconds.