

### Features

- **No Output Capacitor Required**
- **Operating Voltage: 1.8V~4.5V**
- **Supply Current**
  - $I_{DD}=5mA$  at  $V_{DD}=3.3V$
- **Low Shutdown Current**
  - $I_{DD}=1mA$  at  $V_{DD}=3.3V$
- **Meeting VISTA Requirements**
- **Output Power**
  - at 1% THD+N
  - 70mW, at  $V_{DD}=3.3V$ ,  $R_L = 16\Omega$
  - at 10% THD+N
  - 100mW, at  $V_{DD}=3.3V$ ,  $R_L = 16\Omega$
- **Less External Components Required**
- **High PSRR: 78dB at 217Hz**
- **Short-Circuit and Thermal Protection**
- **$\pm 8KV$  ESD Performance**
- **Surface-Mount Packaging**
  - WLCSP2x2-16
- **Lead Free and Green Devices Available (RoHS Compliant)**

### General Description

The APA2178 is a stereo, fixed gain, Cap-Free headphone driver which is available in a WLCSP2x2-16 package.

The APA2178 is a ground-reference output, and doesn't need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, PCB's space, and component height.

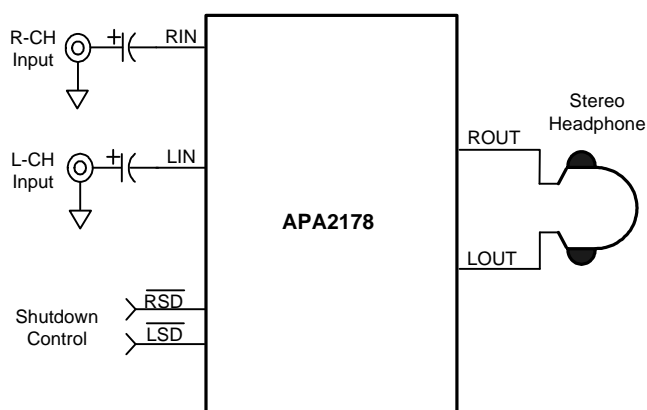
The built-in gain setting can minimize the external component counts and save the PCB space. High PSRR provides increased immunity to noise and RF rectification. In addition to these features, a fast startup time and small package size make the APA2178 an ideal choice for portable multimedia device.

Moreover, the APA2178 is also equipped other features. For example, it is capable of driving 100mW at 3.3V into  $16\Omega$ , at THD+N=10% and provides thermal and short circuit protection.

### Applications

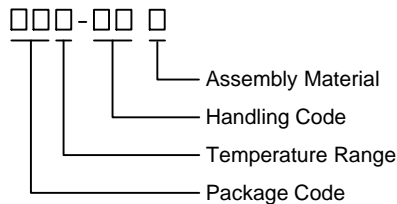

- **Handsets**
- **PDA's**
- **Portable multimedia devices**
- **Notebooks**

### Simplified Application Circuit



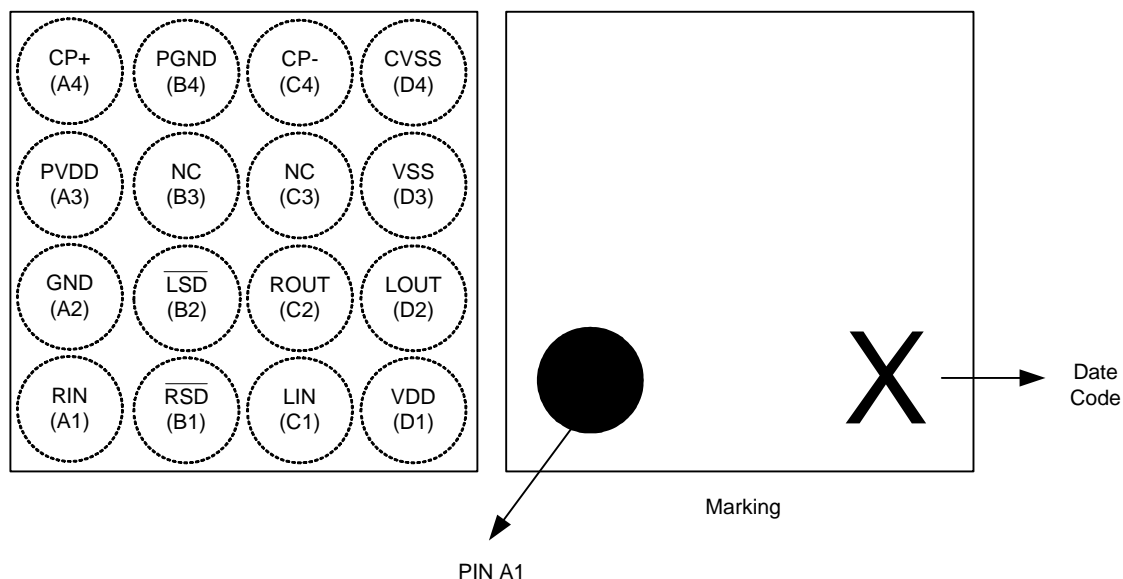
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

<p>APA2178</p>  <p>Assembly Material Handling Code Temperature Range Package Code</p>	<p>Package Code HA : WLCSP2x2-16 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape &amp; Reel Assembly Material G : Halogen and Lead Free Device</p>
<p>APA2178 HA :</p>	 <p>X - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration



## Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
$V_{PVDD\_VDD}$	PVDD to VDD Voltage	-0.3 to 0.3	V
$V_{PGND\_GND}$	PGND to GND Voltage	-0.3 to 0.3	V
$V_{VDD}, V_{DD}$	Supply Voltage (VDD and PVDD to GND and PGND)	-0.3 to 5.5	V
$V_{RSD}, V_{LSD}$	Input Voltage (RSD and LSD to GND)	GND-0.3 to $V_{DD}+0.3$	V
$V_{SS}, CV_{SS}$	VSS and CVSS to GND and PGND Voltage	-5.5 to 0.3	V
$V_{ROUT}, V_{LOUT}$	ROUT and LOUT to GND Voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
$V_{CP+}$	CP+ to PGND Voltage	PGND-0.3 to $PV_{DD}+0.3$	V
$V_{CP-}$	CP- to PGND Voltage	$PV_{SS}-0.3$ to PGND+0.3	V
$T_A$	Operating Ambient Temperature Range	-40 to 85	°C
$T_J$	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_{SDR}$	Maximum Soldering Temperature Range, 10 Seconds	260	°C
$P_D$	Power Dissipation	Internally Limited	W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Junction-to-Ambient Resistance in Free Air <sup>(Note 2)</sup> WLCSP2x2-16	160	°C/W

Note 2: Please refer to "Thermal Pad Consideration". 2 layered 5 in2 printed circuit boards with 2oz trace and copper through several thermal vias. The thermal pad is soldered on the PCB.

## Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
$V_{DD}$	Supply Voltage	1.8 ~ 4.5	V
$V_{IH}$	High Level Threshold Voltage	$0.6V_{DD} \sim V_{DD}$	V
$V_{IL}$	Low Level Threshold Voltage	$0 \sim 0.3V_{DD}$	V
$V_{ICM}$	Common Mode Input Voltage	$\sim V_{DD}-0.5$	V
$T_A$	Ambient Temperature	-40 ~ 85	°C
$T_J$	Junction Temperature	-40 ~ 125	°C
$R_L$	Headphone Resistance	14 ~	$\Omega$

Note 3 : Refer to the typical application circuit.

## Electrical Characteristics

Unless otherwise specified, these specifications apply over  $V_{DD}=PV_{DD}=3.3V$ ,  $V_{PGND}=V_{GND}=0V$ , and  $C_{CPO}=C_{CPF}=1\mu F$ .  
Typical values are at  $T_A=25^\circ C$ .

Symbol	Parameter	Test Conditions	AP2178			Unit
			Min.	Typ.	Max.	
$V_{DD}$	Supply Voltage		1.8	-	4.5	V
$I_{DD}$	Supply Current		-	5	10	mA
$I_{SD}$	Shutdown Current	$\overline{RSD} = \overline{LSD} = 0V$	-	1	2	$\mu A$
$I_i$	Input Current	$\overline{RSD}, \overline{LSD}$	-	0.1	-	$\mu A$
<b>CHARGE PUMP</b>						
$F_{OSC}$	Switching Frequency		440	520	580	kHz
$R_{eq}$	Charge Pump Requirement Resistance		6	7	9	$\Omega$
<b>POWER-ON-RESET</b>						
	Rising VDD Threshold		1.67	1.7	1.73	V
	Falling VDD Threshold		1.57	1.6	1.63	V
<b>AMPLIFIERS</b>						
$A_V$	Internal Voltage Gain	No Load	-1.55	-1.5	-1.45	V/V
$\Delta A_V$	Gain Match		-	1	-	%
$R_i$	Input Resistance		12	14	16	k $\Omega$
SR	Slew Rate		-	2.5	-	V/ $\mu s$
$V_{OS}$	Output Offset Voltage	$V_{DD}=1.8V$ to $4.5V$ , $R_L = 32\Omega$	-5	-	5	mV
$V_n$	Noise Output Voltage		-	15	-	$\mu V_{rms}$
PSRR	Power Supply Rejection Ratio	$V_{DD}=1.8V$ to $4.5V$ , $V_{rr}=200mV_{rms}$ $f_{in}=217Hz$ $f_{in}=1kHz$ $f_{in}=20kHz$	-	78 75 55	-	dB
$C_L$	Maximum Capacitive Load		-	400	-	pF
$T_{start-up}$	Start-up Time		-	120	-	$\mu s$
OUTR, OUTL	ESD Protection		-	$\pm 8$	-	kV
<b><math>V_{DD}=4.5V, T_A=25^\circ C</math></b>						
$P_O$	Output Power (Stereo, in Phase)	THD+N = 1%, $f_{in}=1kHz$ $R_L = 16\Omega$ $R_L = 32\Omega$	120	150 145	-	mW
		THD+N = 10%, $f_{in}=1kHz$ $R_L = 16\Omega$ $R_L = 32\Omega$	180	215 205	-	
THD+N	Total Harmonic Distortion Pulse Noise	$f_{in} = 1kHz$ $P_O = 105mW, R_L = 16\Omega$ $P_O = 100mW, R_L = 32\Omega$ $V_O = 2.2V_{rms}, R_L = 300\Omega$ $V_O = 2.2V_{rms}, R_L = 10k\Omega$	-	0.03 0.02 0.005 0.003	-	%

## Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over  $V_{DD}=PV_{DD}=3.3V$ ,  $V_{PGND}=V_{GND}=0V$ , and  $C_{CPO}=C_{CPF}=1\mu F$ .  
Typical values are at  $T_A=25^\circ C$ .

Symbol	Parameter	Test Conditions	APA2178			Unit
			Min.	Typ.	Max.	
<b><math>V_{DD}=4.5V</math>, <math>T_A=25^\circ C</math> (CONT.)</b>						
Crosstalk	Channel Separation	$f_{in} = 1kHz$ $P_O = 15mW$ , $R_L = 16\Omega$ $P_O = 15mW$ , $R_L = 32\Omega$ $V_O = 0.31V_{rms}$ , $R_L = 300\Omega$ $V_O = 0.31V_{rms}$ , $R_L = 10k\Omega$	-	75 80 95 100	-	dB
S/N	Signal-to-Noise Ratio	With A-weighting Filter $P_O = 100mW$ , $R_L = 32\Omega$ $V_O = 3.1V_{rms}$ , $R_L = 10k\Omega$	-	100 105	-	dB
<b><math>V_{DD}=3.3V</math>, <math>T_A=25^\circ C</math></b>						
$P_O$	Output Power (Stereo, in Phase)	THD+N = 1%, $f_{in}=1kHz$ $R_L = 16\Omega$ $R_L = 32\Omega$	55	70 70	-	mW
		THD+N = 10%, $f_{in}=1kHz$ $R_L = 16\Omega$ $R_L = 32\Omega$	80	100 100	-	
THD+N	Total Harmonic Distortion Pulse Noise	$f_{in} = 1kHz$ $P_O = 50mW$ , $R_L = 16\Omega$ $P_O = 50mW$ , $R_L = 32\Omega$ $V_O = 1.6V_{rms}$ , $R_L = 300\Omega$ $V_O = 1.6V_{rms}$ , $R_L = 10k\Omega$	-	0.03 0.02 0.005 0.003	-	%
Crosstalk	Channel Separation	$f_{in} = 1kHz$ $P_O = 7mW$ , $R_L = 16\Omega$ $P_O = 7mW$ , $R_L = 32\Omega$ $V_O = 0.23V_{rms}$ , $R_L = 300\Omega$ $V_O = 0.23V_{rms}$ , $R_L = 10k\Omega$	-	75 85 95 95	-	dB
S/N	Signal-to-Noise Ratio	With A-weighting Filter $P_O = 50mW$ , $R_L = 32\Omega$ $V_O = 2.3V_{rms}$ , $R_L = 10k\Omega$	-	95 100	-	dB
<b><math>V_{DD}=1.8V</math>, <math>T_A=25^\circ C</math></b>						
$P_O$	Output Power (Stereo, in Phase)	THD+N = 1%, $f_{in}=1kHz$ $R_L = 32\Omega$	10	13	-	mW
		THD+N = 10%, $f_{in}=1kHz$ $R_L = 32\Omega$	15	20	-	
THD+N	Total Harmonic Distortion Pulse Noise	$f_{in} = 1kHz$ $P_O = 9mW$ , $R_L = 32\Omega$ $V_O = 0.85V_{rms}$ , $R_L = 300\Omega$ $V_O = 0.85V_{rms}$ , $R_L = 10k\Omega$	-	0.03 0.007 0.005	-	%

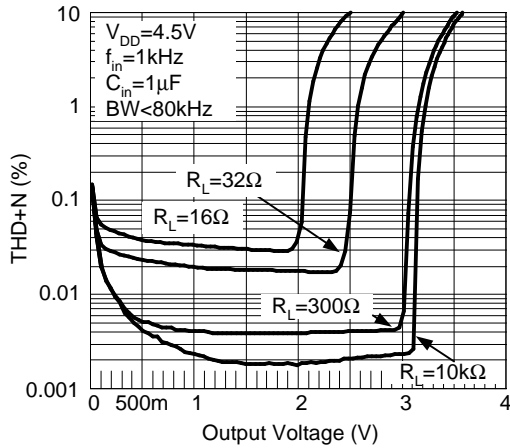
## Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over  $V_{DD}=PV_{DD}=3.3V$ ,  $V_{PGND}=V_{GND}=0V$ , and  $C_{CPO}=C_{CPF}=1\mu F$ .  
 Typical values are at  $T_A=25^\circ C$ .

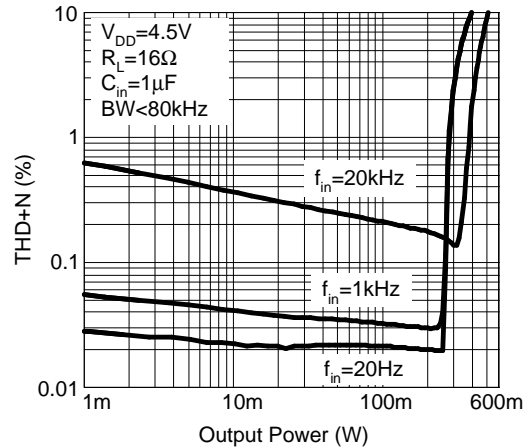
Symbol	Parameter	Test Conditions	APA2178			Unit
			Min.	Typ.	Max.	
<b><math>V_{DD}=1.8V</math>, <math>T_A=25^\circ C</math> (CONT.)</b>						
Crosstalk	Channel separation	$f_{in} = 1kHz$ $P_O = 1.3mW$ , $R_L = 32\Omega$ $V_O = 0.12V_{rms}$ , $R_L = 300\Omega$ $V_O = 0.12V_{rms}$ , $R_L = 10k\Omega$	-	80 85 90	-	dB
S/N	Signal-to-Noise Ratio	With A-weighting Filter $P_O = 9mW$ , $R_L = 32\Omega$ $V_O = 1.2V_{rms}$ , $R_L = 10k\Omega$	-	95 95	-	dB

Typical Operating Characteristics

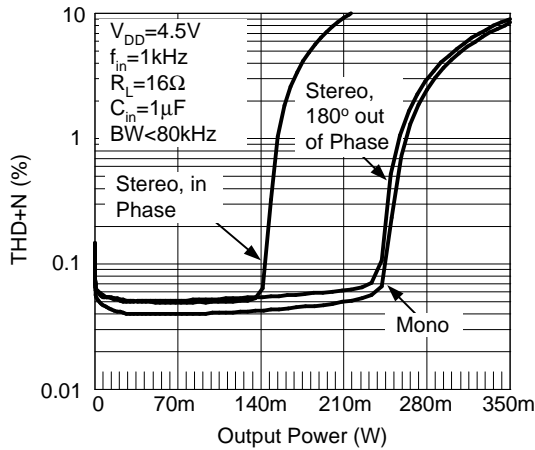
THD+N vs. Output Voltage



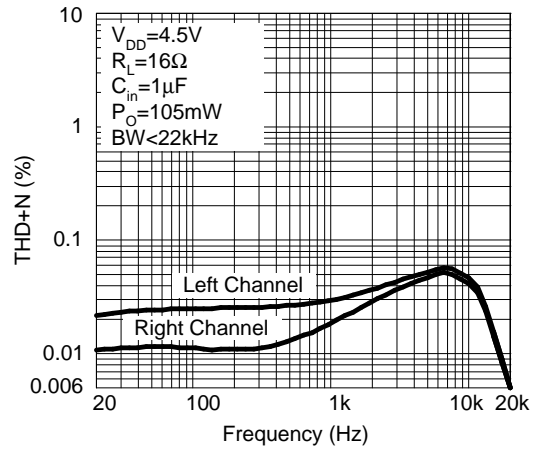
THD+N vs. Output Power



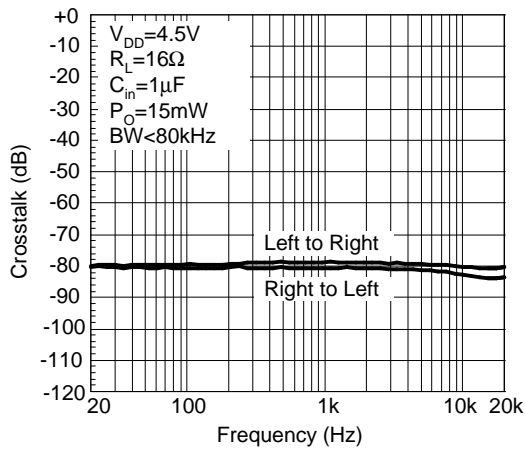
THD+N vs. Output Power



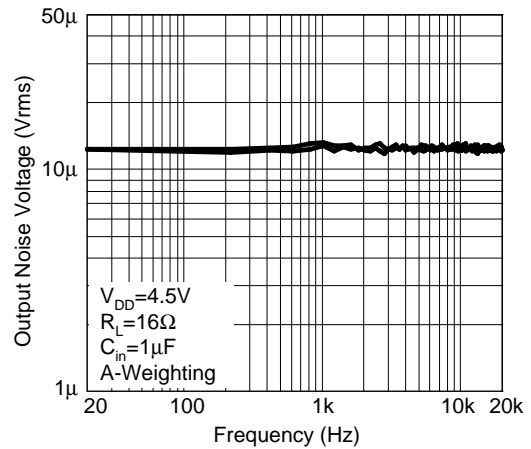
THD+N vs. Frequency



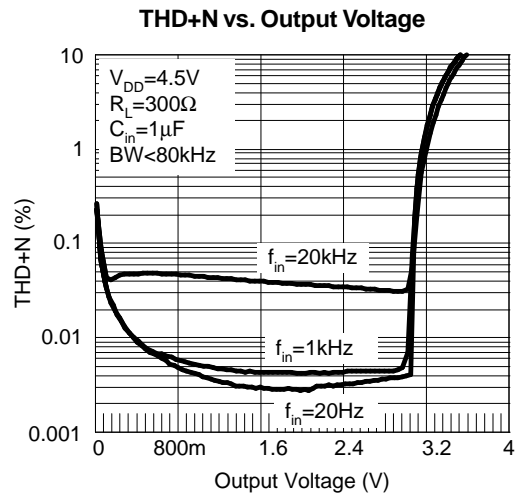
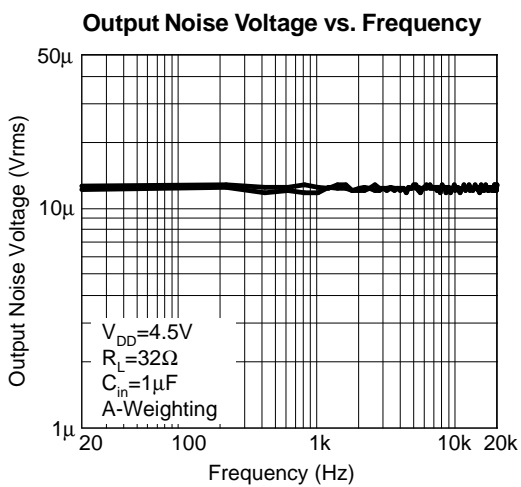
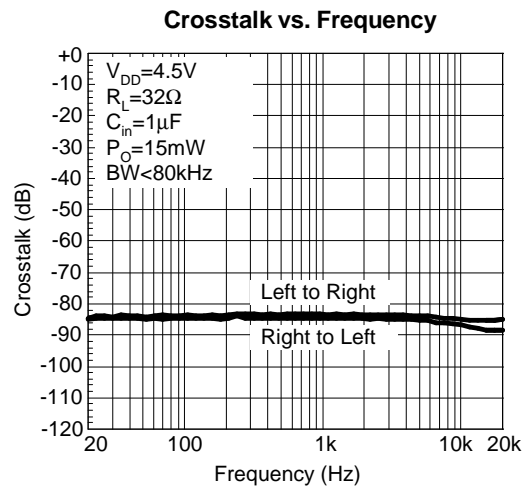
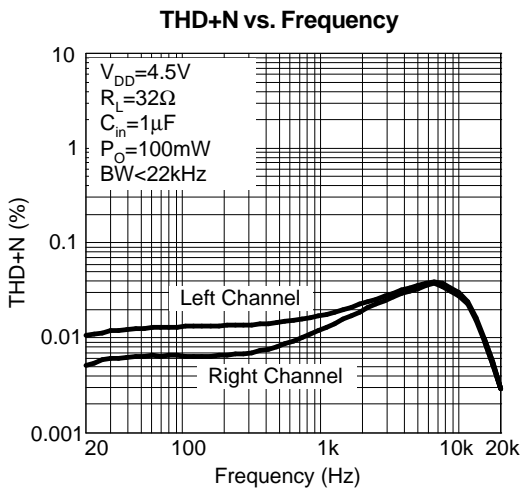
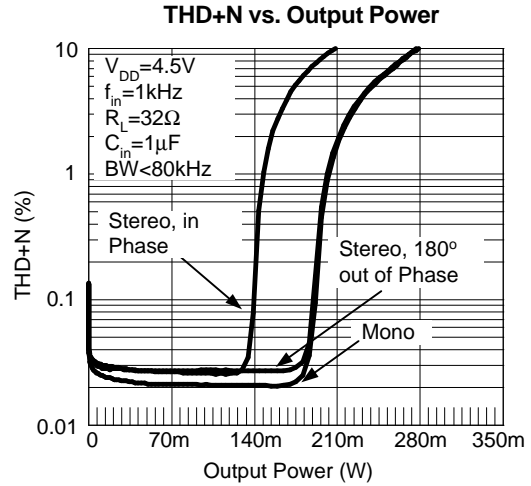
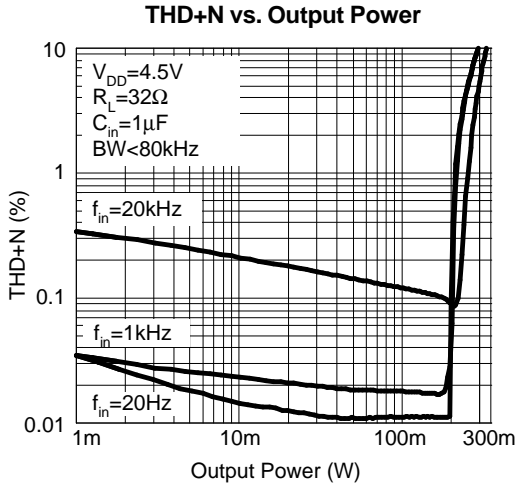
Crosstalk vs. Frequency



Output Noise Voltage vs. Frequency

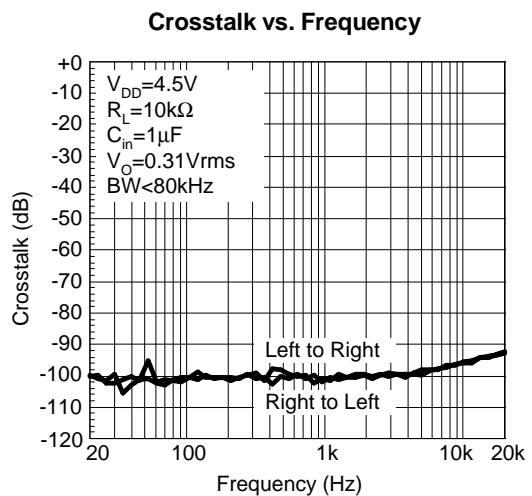
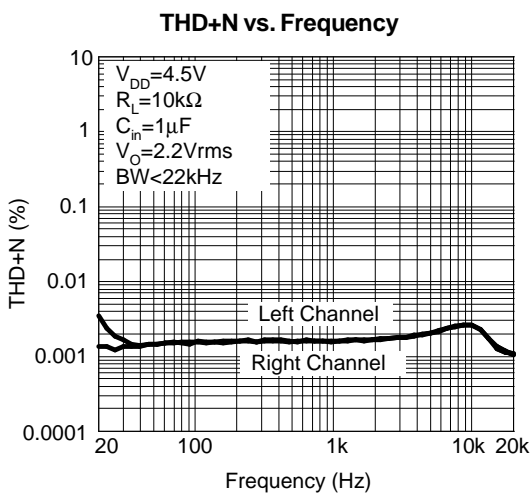
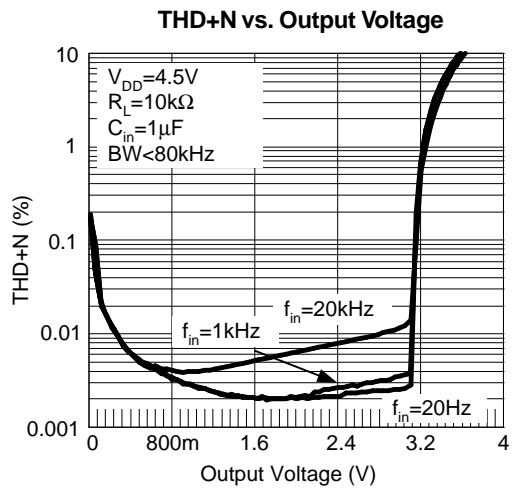
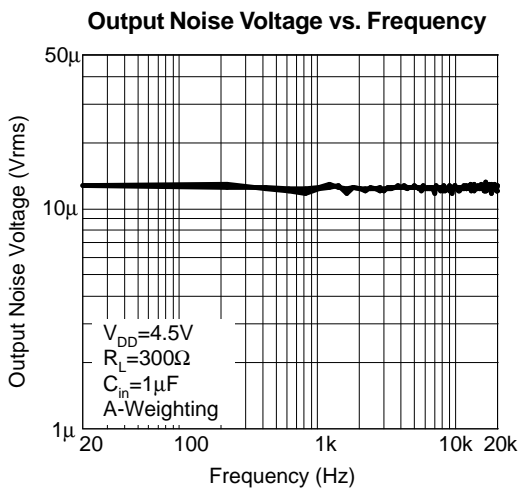
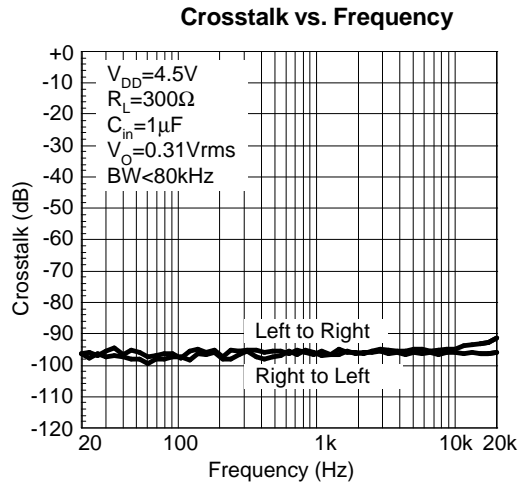
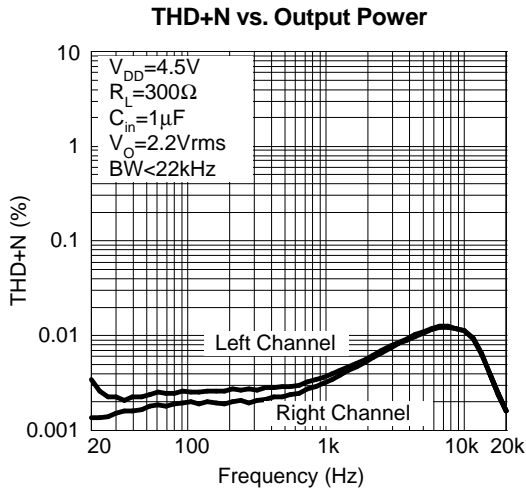


Typical Operating Characteristics (Cont.)

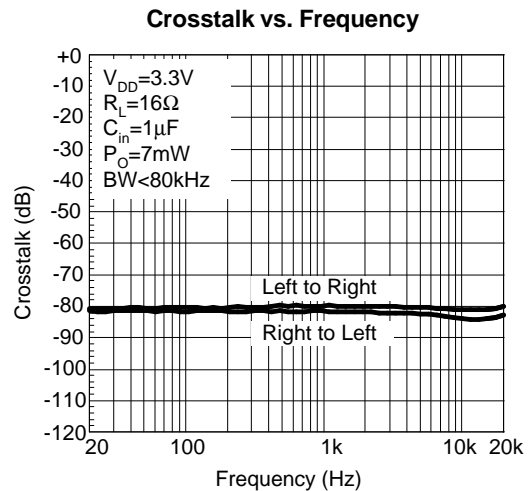
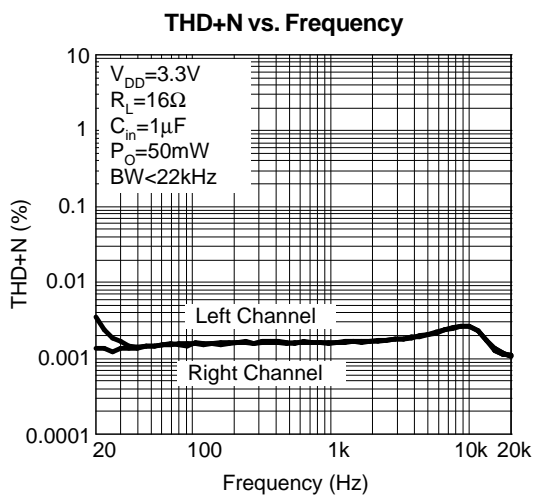
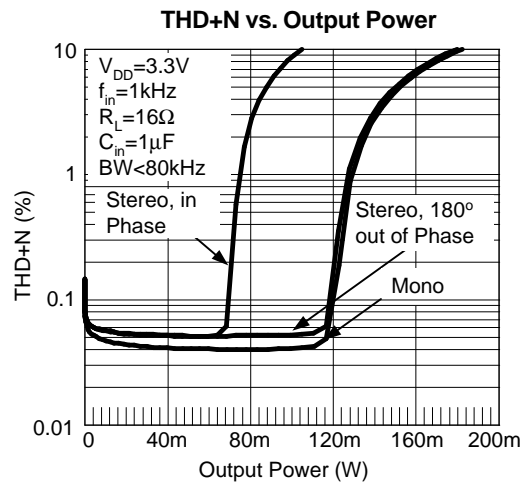
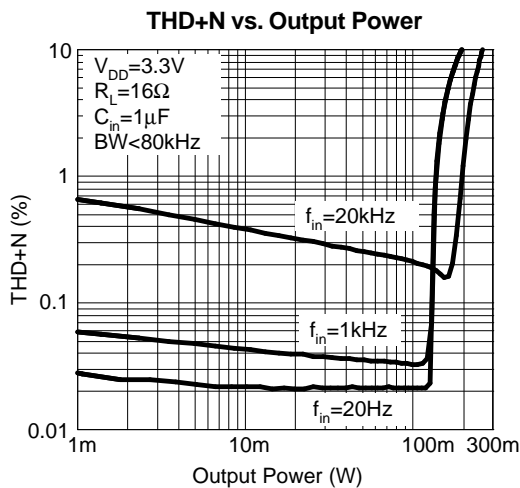
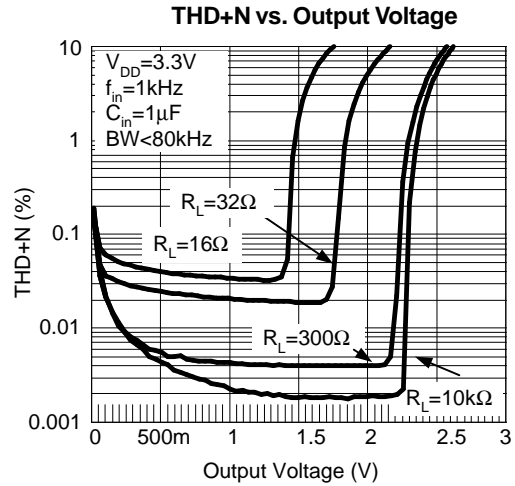
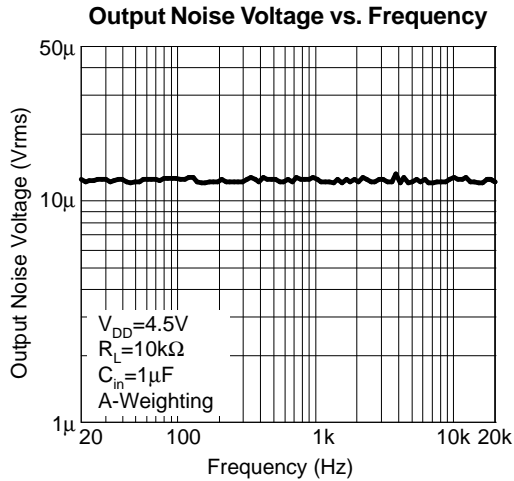




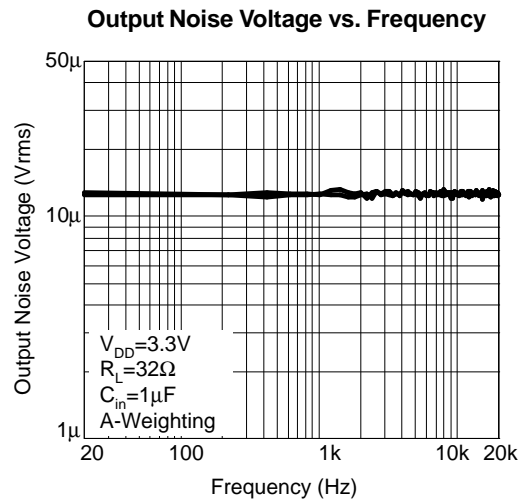
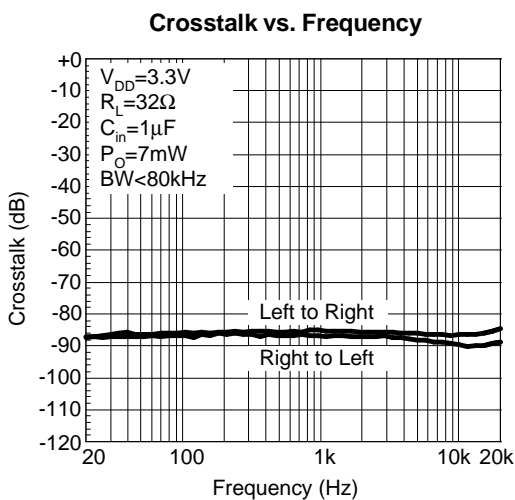
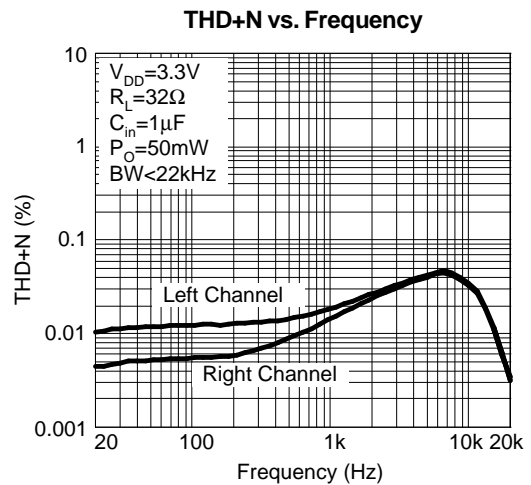
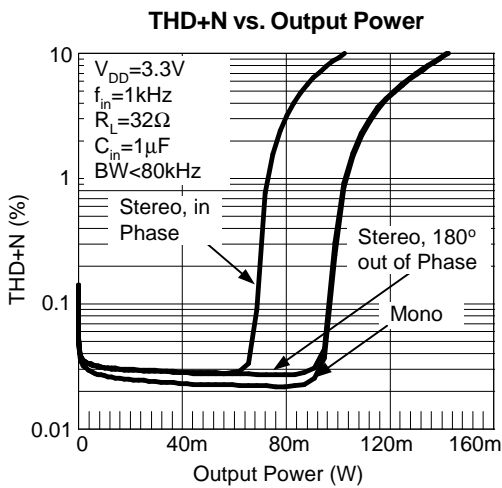
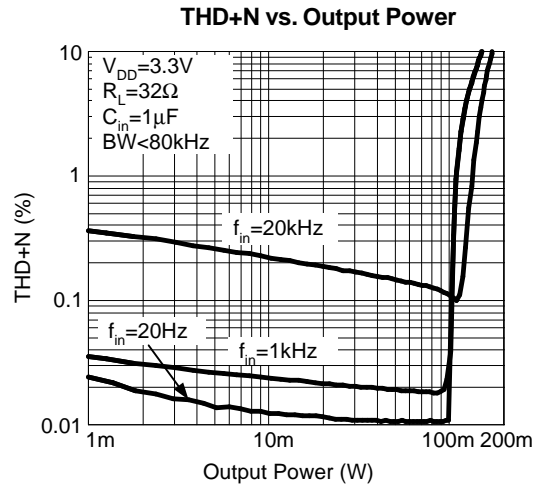
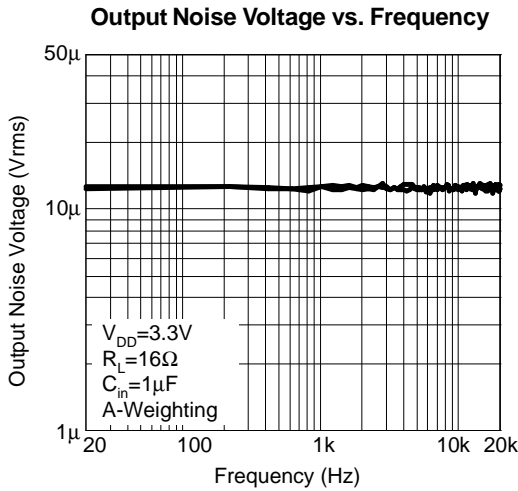
Typical Operating Characteristics (Cont.)



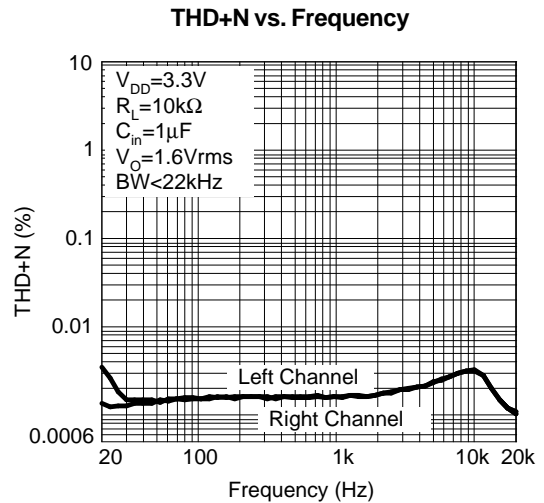
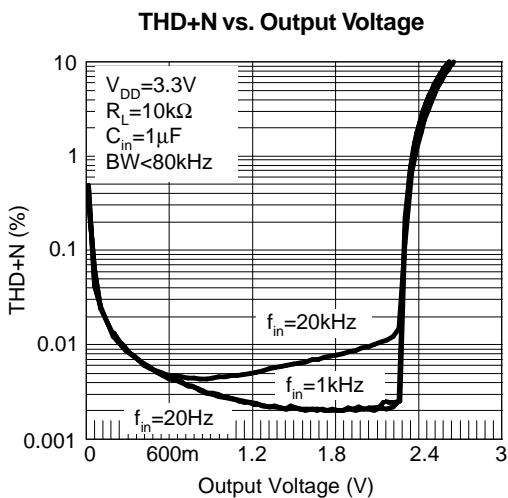
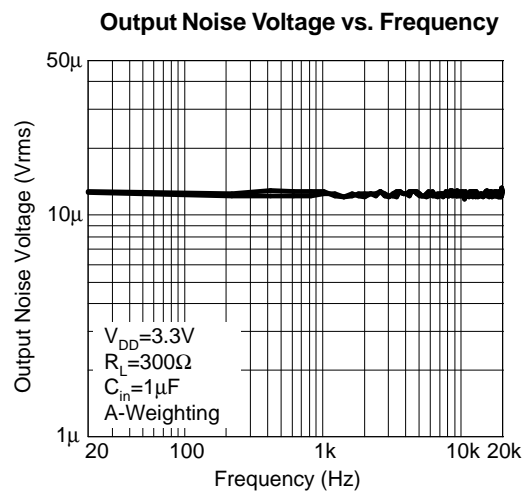
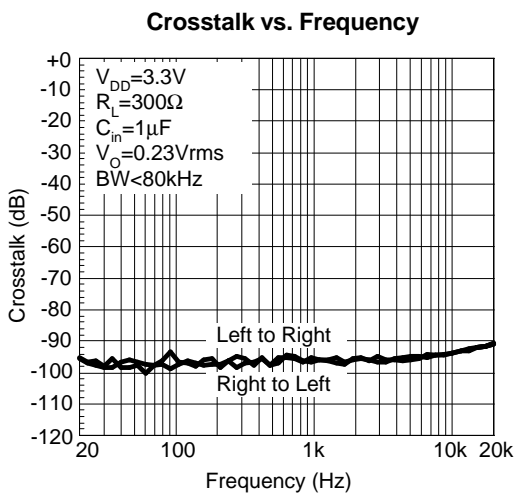
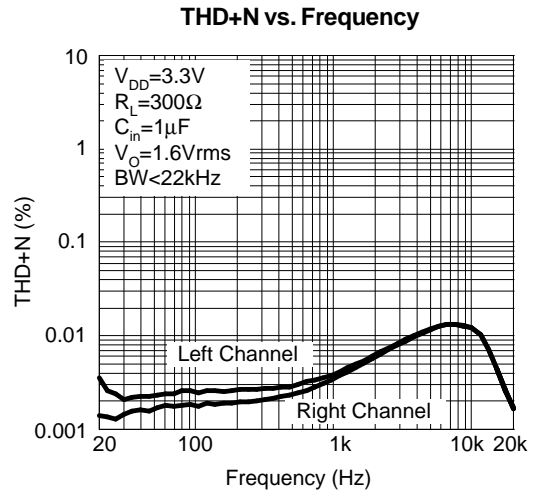
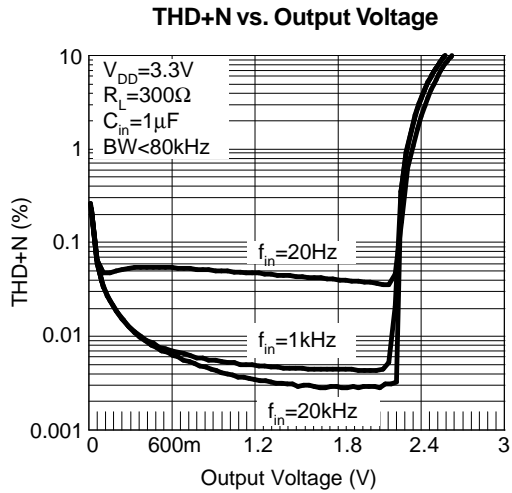
Typical Operating Characteristics (Cont.)



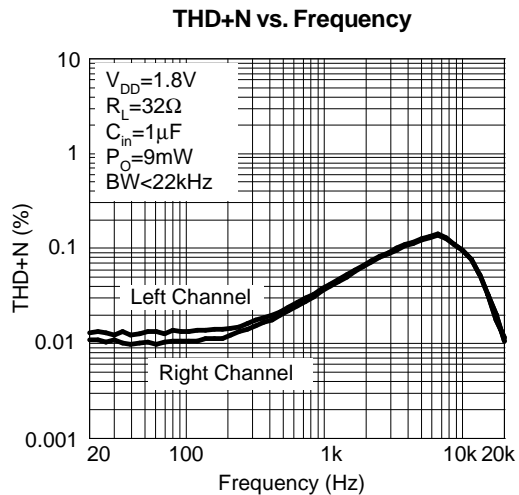
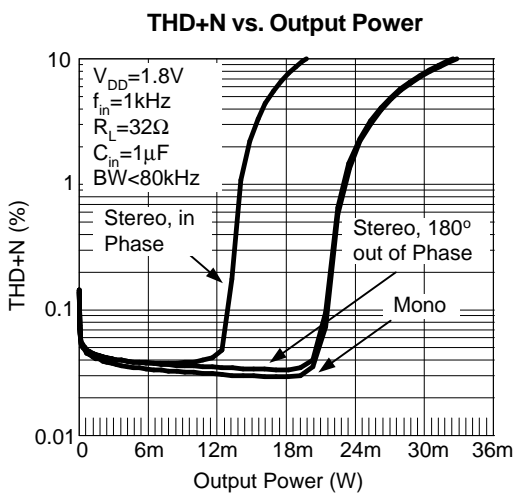
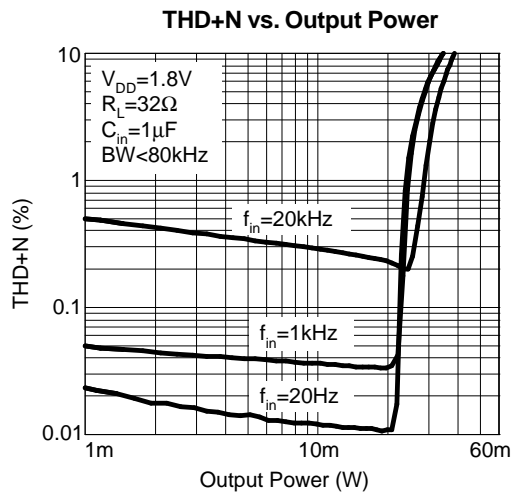
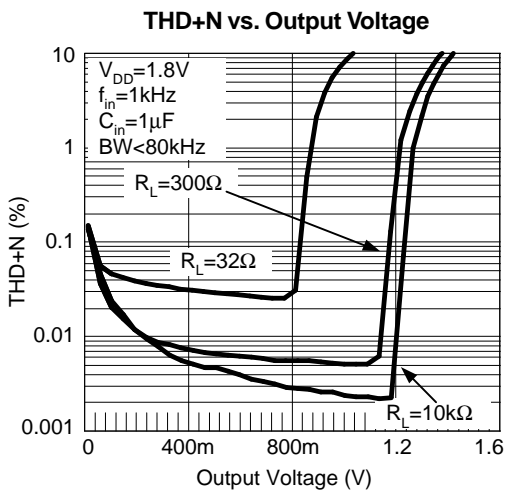
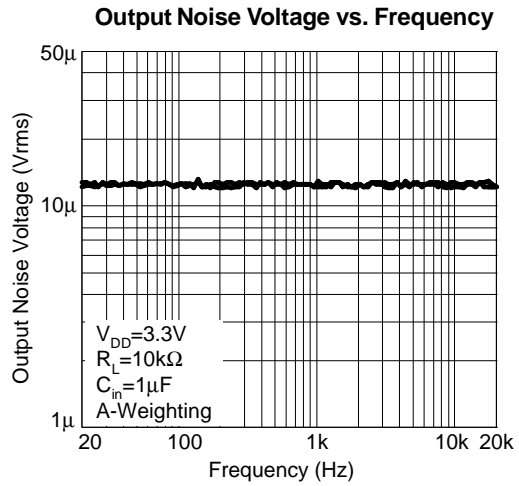
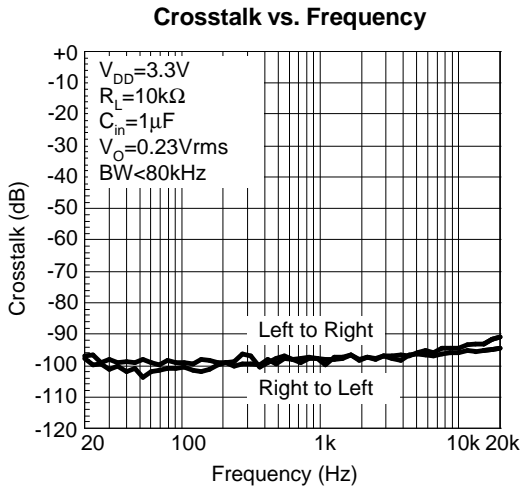
Typical Operating Characteristics (Cont.)



Typical Operating Characteristics (Cont.)

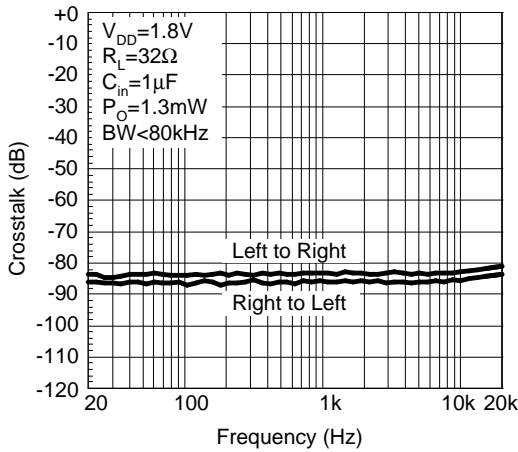


Typical Operating Characteristics (Cont.)

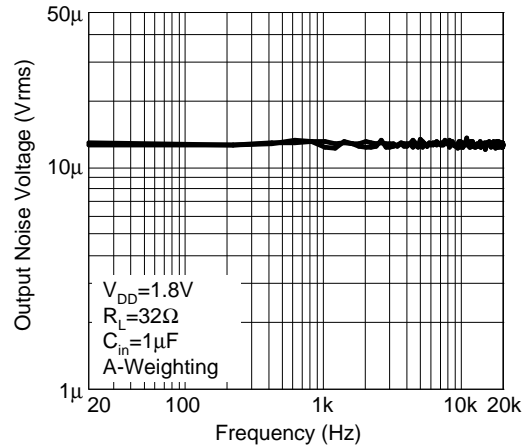


Typical Operating Characteristics (Cont.)

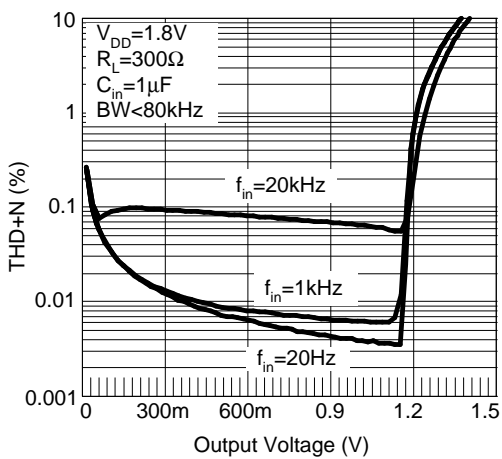
Crosstalk vs. Frequency



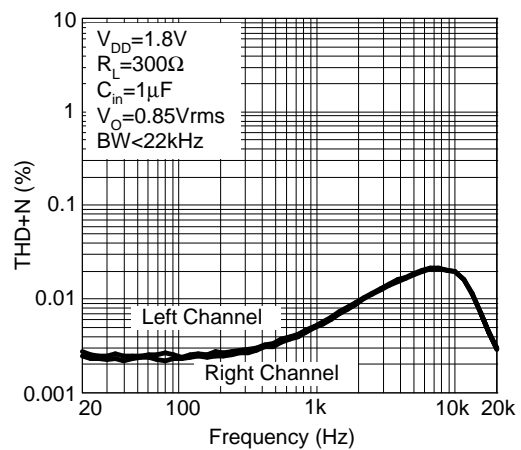
Output Noise Voltage vs. Frequency



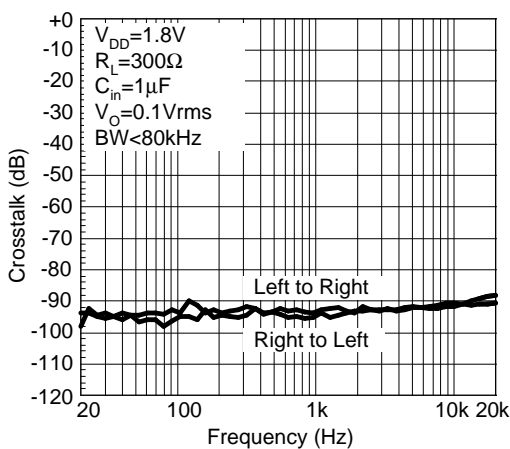
THD+N vs. Output Voltage



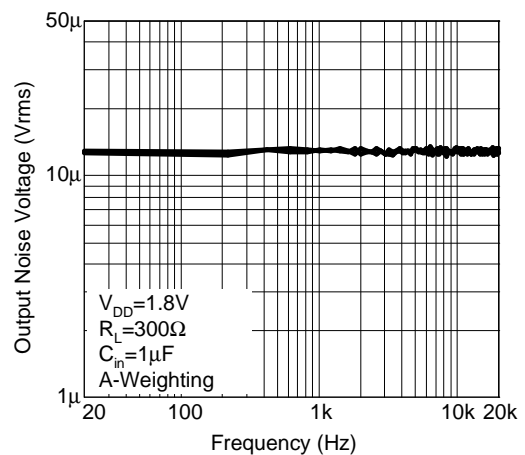
THD+N vs. Frequency



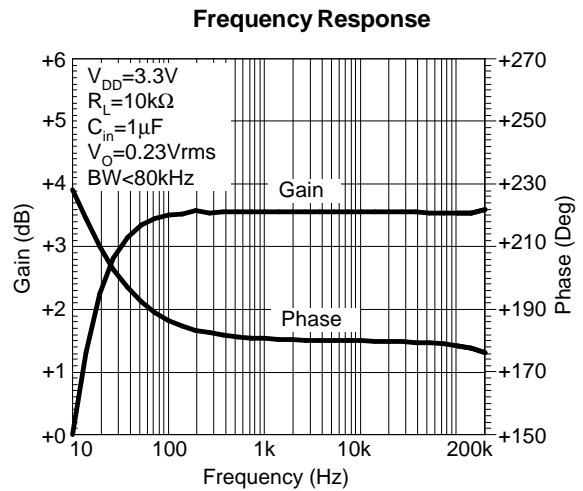
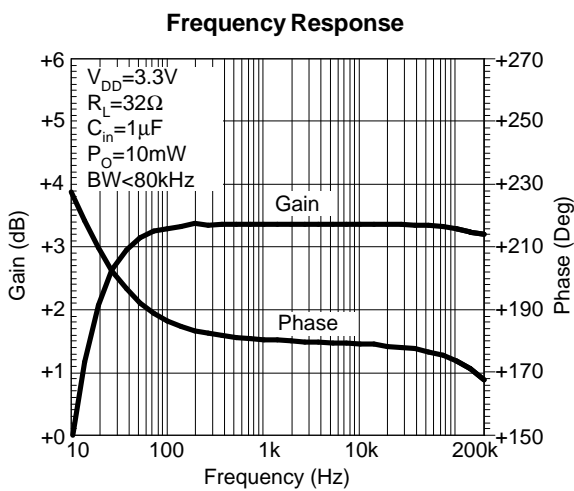
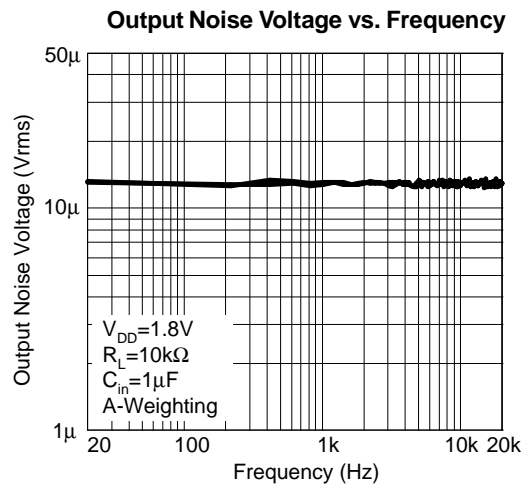
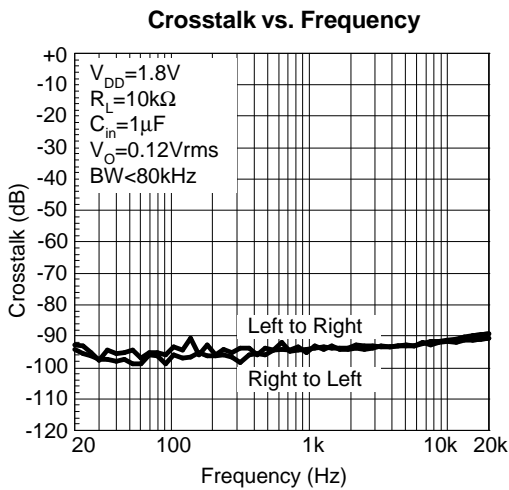
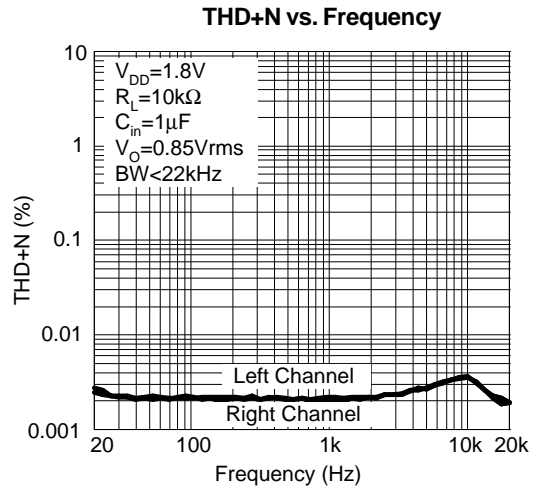
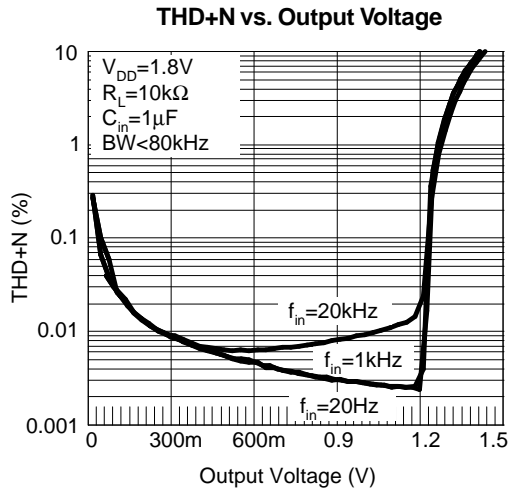
Crosstalk vs. Frequency



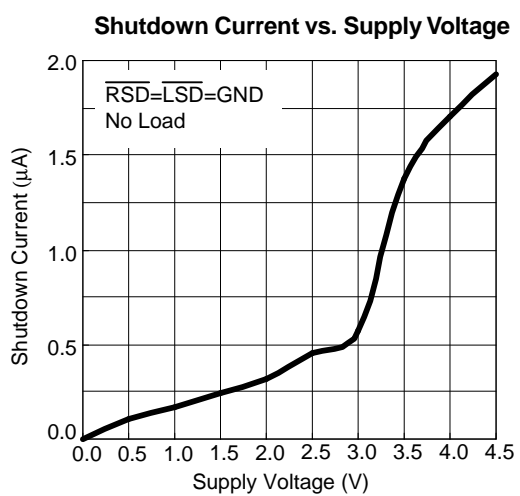
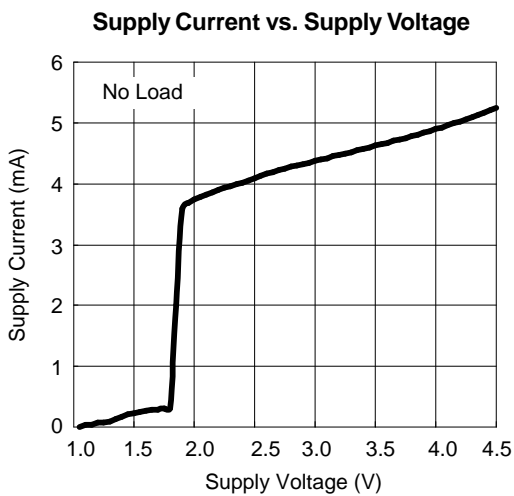
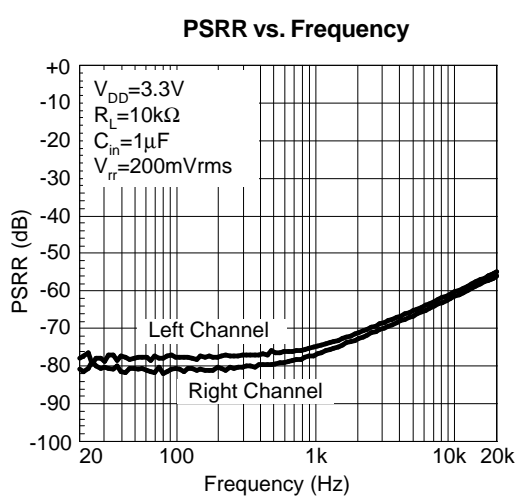
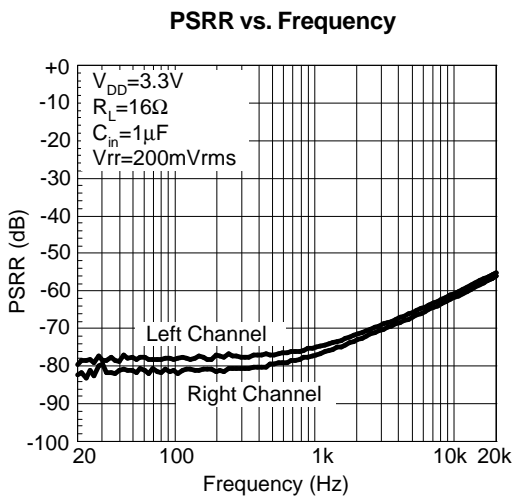
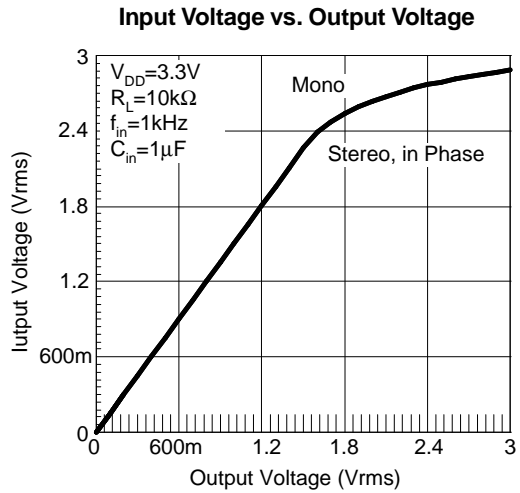
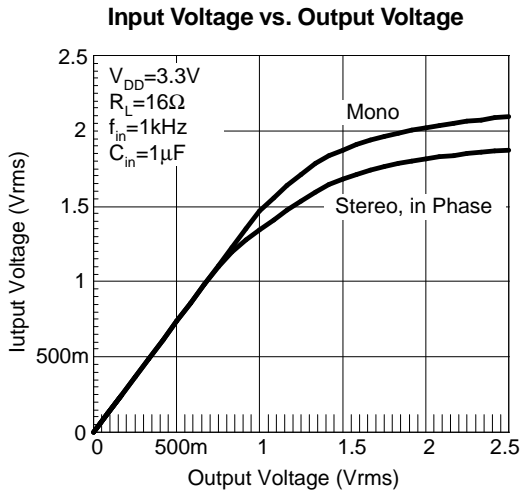
Output Noise Voltage vs. Frequency



Typical Operating Characteristics (Cont.)

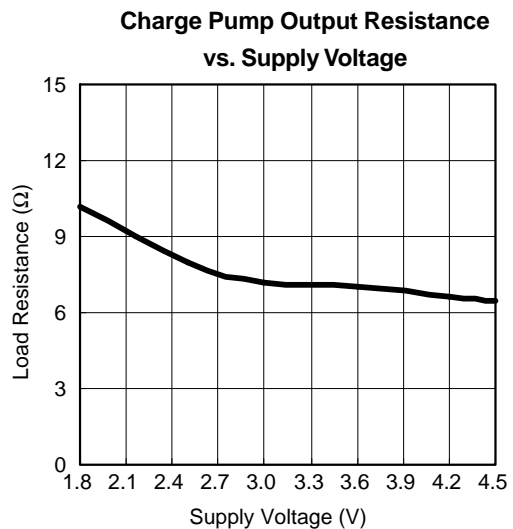
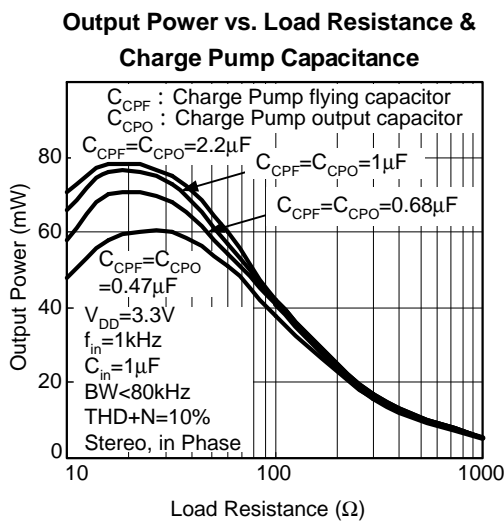
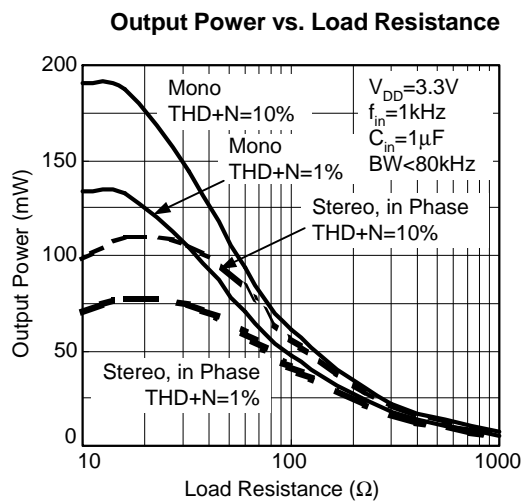
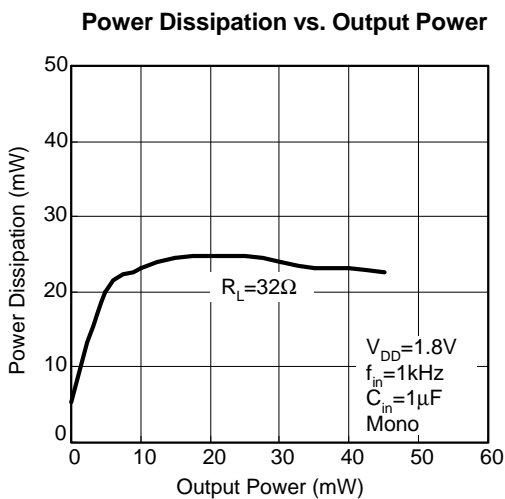
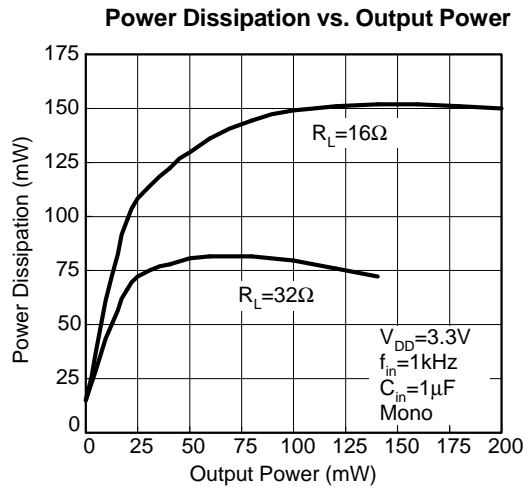
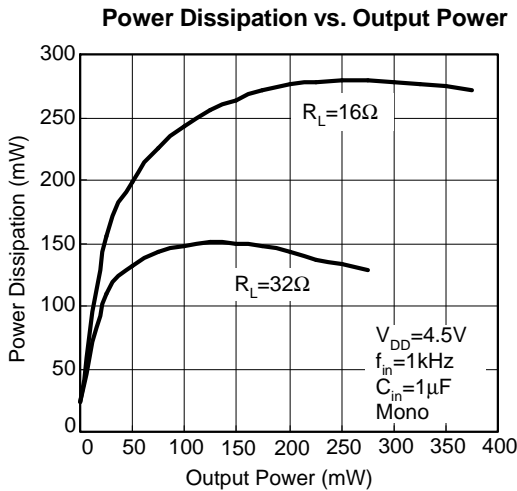


Typical Operating Characteristics (Cont.)



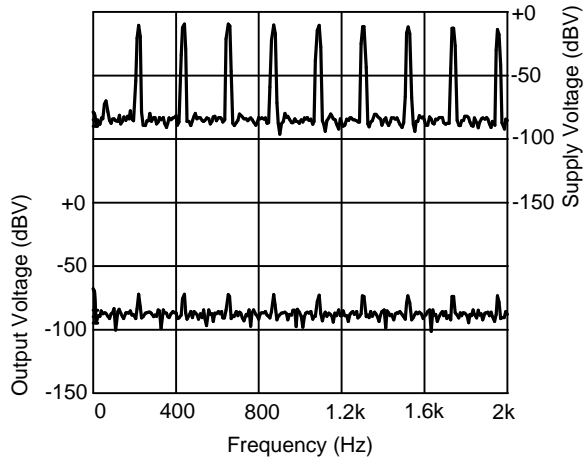


Typical Operating Characteristics (Cont.)

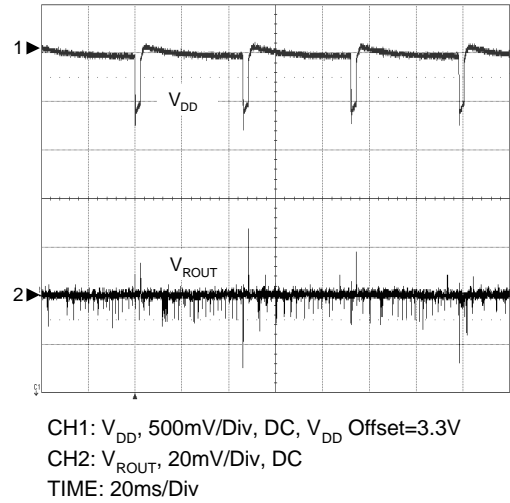


Typical Operating Characteristics (Cont.)

GSM Power Supply Rejection vs. Frequency

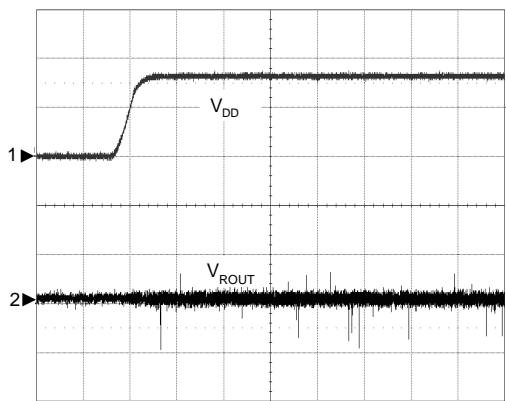


GSM Power Supply Rejection vs. Time



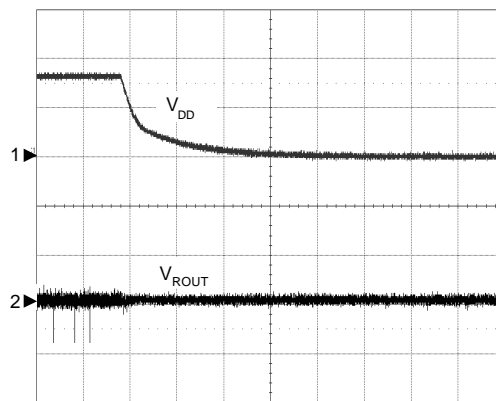
## Operating Waveforms

Output Transient at Turn On



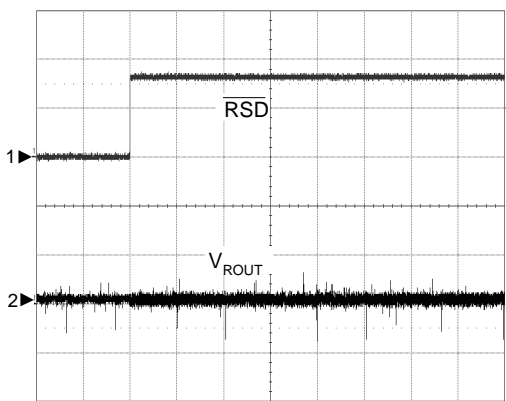
CH1:  $V_{DD}$ , 2V/Div, DC  
 CH2:  $V_{ROUT}$ , 20mV/Div, DC  
 TIME: 20ms/Div

Output Transient at Turn Off



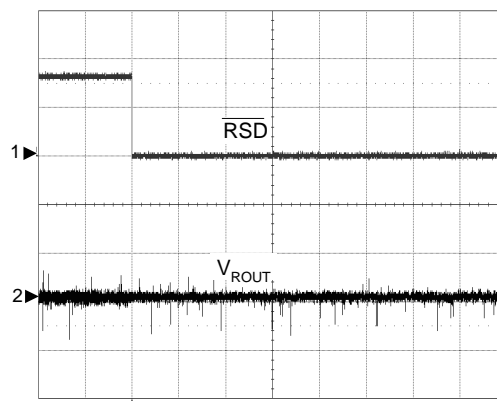
CH1:  $V_{DD}$ , 2V/Div, DC  
 CH2:  $V_{ROUT}$ , 20mV/Div, DC  
 TIME: 200ms/Div

Output Transient at Shutdown Release



CH1:  $\overline{RSD}$ , 2V/Div, DC  
 CH2:  $V_{ROUT}$ , 20mV/Div, DC  
 TIME: 20ms/Div

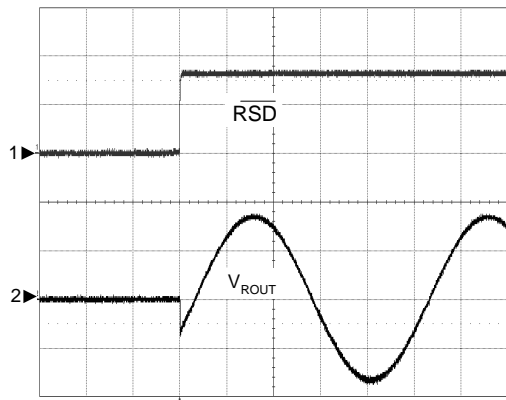
Output Transient at Shutdown Active



CH1:  $\overline{RSD}$ , 2V/Div, DC  
 CH2:  $V_{ROUT}$ , 20mV/Div, DC  
 TIME: 20ms/Div

Operating Waveforms (Cont.)

Shutdown Release

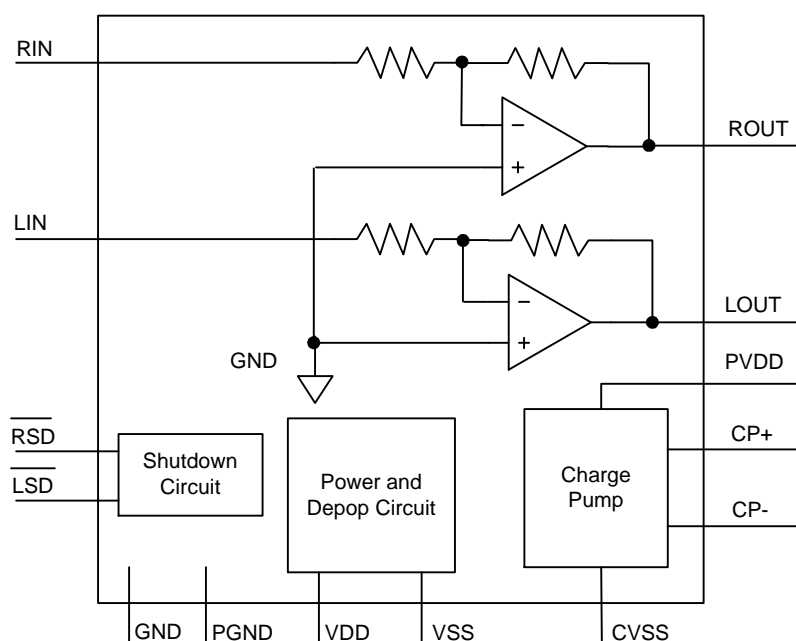


CH1: V<sub>DD</sub>, 2V/Div, DC  
 CH2: V<sub>ROUT</sub>, 1V/Div, DC  
 TIME: 200μs/Div

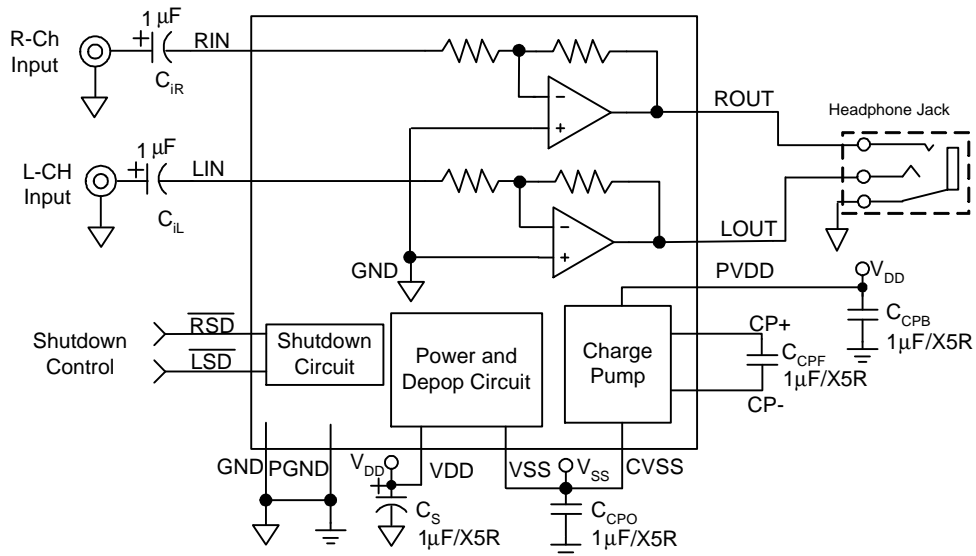
## Pin Description

PIN		I/O/P	FUNCTION
NO.	MANE		
A1	RIN	I	Right channel audio signal input pin.
A2	GND	P	Ground connection for circuitry.
A3	PVDD	P	Charge pump power supply voltage input pin.
A4	CP+	I/O	Charge pump flying capacitor positive connection.
B1	$\overline{\text{RSD}}$	I	Right channel shutdown mode control pin. A low-level voltage applied on this pin shuts off the right channel headphone driver.
B2	$\overline{\text{LSD}}$	I	Left channel shutdown mode control pin. A low-level voltage applied on this pin shuts off the left channel headphone driver.
B3,C3	NC	-	No Connection.
B4	PGND	P	Charge pump ground.
C1	LIN	I	Left channel audio signal input pin.
C2	ROUT	O	Right channel output for headphone.
C4	CP-	I/O	Charge pump flying capacitor negative connection.
D1	VDD	P	Supply voltage input pin.
D2	LOUT	O	Left channel output for headphone.
D3	VSS	P	Connect this pin to CVSS.
D4	CVSS	O	Charge pump output.

## Block Diagram



Typical Application Circuit



**Function Description**

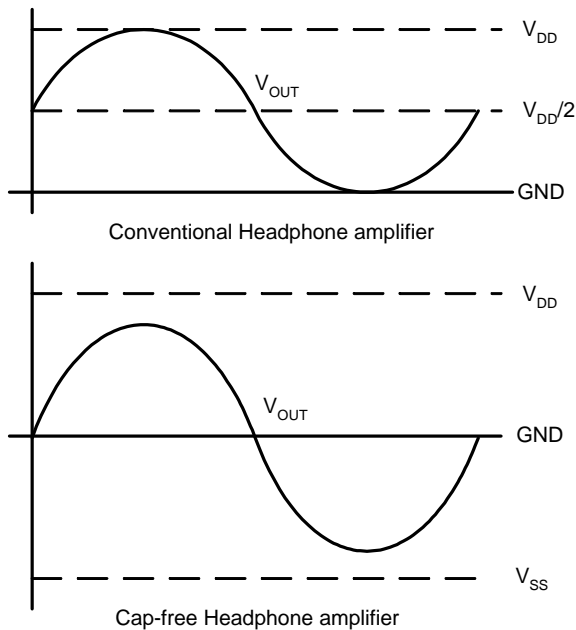


Figure 1. Cap-free Operation

The APA2178 is a stereo, fixed gain, and cap-free headphone driver. The gain is set by internal resistors, input resistors ( $R_i$ ), and feedback resistors ( $R_f$ ) with  $-1.5V/V$  (See Typical Application Circuit).

The APA2178 headphone drivers use a charge pump to invert the positive power supply ( $PV_{DD}$ ) to negative power supply ( $CV_{SS}$ ), see figure 1. The headphone drivers operate at this bipolar power supply ( $V_{DD}$  and  $V_{SS}$ ) and the outputs reference refers to the ground. This feature eliminates the output capacitors which are used in conventional single-ended headphone amplifiers. Compared with the single power supply amplifiers, the power supply voltage is almost double.

**Shutdown Function**

In order to reduce power consumption, the APA2178 contains two shutdown signal input pins ( $\overline{LSD}$  for left channel and  $\overline{RSD}$  for right channel) to allow the respective shutdown which turns off the bias current of the amplifier. This shutdown feature turns the amplifier off when logic low is placed on the  $\overline{RSD}$  or  $\overline{LSD}$  pin for the APA2178. The trigger point between a logic high and a logic low level is typically  $0.6V_{DD}$  and  $0.3V_{DD}$ . It is highly recommended to switch between the ground and the supply

voltage  $PV_{DD}$  to provide maximum device performance. By switching the both  $\overline{RSD}$  and  $\overline{LSD}$  pins to low level, the amplifier enters a low-consumption current circumstance, with charge pump disabled, and very small  $I_{DD}$  for the APA2178. The charge pump is enabled once either  $\overline{RSD}$  or  $\overline{LSD}$  pin is pulled to high. In normal operating, the APA2178  $\overline{RSD}$  and  $\overline{LSD}$  pins should be pulled to high level to keep the IC out of the shutdown mode. The  $\overline{RSD}$  and  $\overline{LSD}$  pins should be tied to a definite voltage to avoid unwanted mode changing.

## Application Information

### Charge Pump Flying Capacitor ( $C_{CPF}$ )

The flying capacitor ( $C_{CPF}$ ) affects the load transient of the charge pump. If the capacitor's value is too small, and then this increases charge pump's output resistance and degrades the performance of headphone amplifier.

Increasing the flying capacitor's value improves the load transient of charge pump. It is recommend to use the low ESR ceramic capacitors (X5R or X7R type is recommended) above  $1\mu\text{F}$ .

### Charge Pump Output Capacitor ( $C_{CPO}$ )

The charge pump needs an output capacitor( $C_{CPO}$ ) to filter the negative output current pulse flowing into CVSS pin as well as reduces the output voltage ripple(CVSS). The capacitor also sucks in surge current flowing from the  $V_{SS}$  pin, the negative power input pin for the amplifiers. The output ripple is determined by the capacitance, ESR, and current ripple of the output capacitor. Increasing the value of output capacitor and decreasing the ESR can reduce the voltage ripple. Using a low-ESR ceramic capacitor greater than  $1\mu\text{F}$  is recommended. For reducing the parasitic inductance and improving the noise decoupling, place the capacitor near the CVSS and PGND pins as close as possible.

### Charge Pump Bypass Capacitor ( $C_{CPB}$ )

The bypass capacitor( $C_{CPB}$ ) connected with  $PV_{DD}$  pin supplies the charge pump with surge current as well as reduces the voltage ripple on  $PV_{DD}$  pin. Using a low-ESR ceramic capacitor  $1\mu\text{F}$ (typical) is recommended. For reducing the parasitic inductance and improving the noise decoupling, place the capacitor near the  $PV_{DD}$  and PGND pins as close as possible.

### Input Capacitor ( $C_i$ )

In the typical application, an input capacitor ( $C_i$ ) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case,  $C_i$  and the input impedance  $R_i$  from a high-pass filter with the cutoff frequency are determined in the following equation:

$$f_{C(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of  $C_i$  must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where  $R_i$  is  $14\text{k}\Omega$  and the specification that calls for a flat bass response down to  $10\text{Hz}$ . The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_C} \quad (2)$$

When input resistance variation is considered, the  $C_i$  is  $1\mu\text{F}$ . Therefore, a value in the range of  $1\mu\text{F}$  to  $2.2\mu\text{F}$  would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network ( $R_i + R_f, C_i$ ) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the negative side of the capacitor should face the amplifiers' inputs in most applications because the DC level of the amplifiers' inputs are held at  $0\text{V}$ . Please note that it is important to confirm the capacitor polarity in the application.

### Power Supply Decoupling ( $C_s$ )

The APA2178 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitor that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically  $0.1\mu\text{F}$ , is placed as close as possible to the device VDD lead for the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of  $10\mu\text{F}$  or greater placed near the audio power amplifier is recommended.

### Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package in normal operating condition. The first consideration to calculate maximum ambient tem-



## Application Information (Cont.)

### Thermal Consideration (Cont.)

peratures is the numbers from the Power Dissipation vs. Output Power graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given  $\theta_{JA}$ , the maximum allowable junction temperature ( $T_{JMax}$ ), the total internal dissipation ( $P_D$ ), and the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2178 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graphs. The APA2178 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

### Layout Consideration

1. All components should be placed close to the APA2178. For example, the input capacitor ( $C_{iR}$ ,  $C_{iL}$ ) should be close to APA2178 input pins to avoid causing noise coupling to APA2178 high impedance inputs; the decoupling capacitor ( $C_S$ ) should be placed by the APA2178 power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 50mil.
5. The input trace and output trace should be away from  $C_{CPF}$  and  $C_{CPB}$  possible.

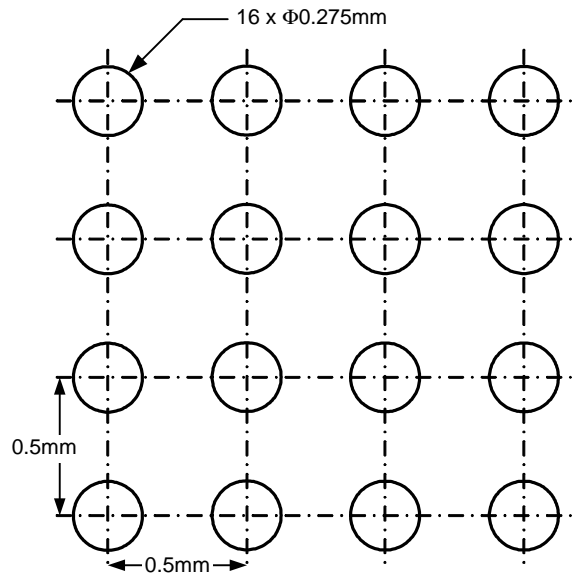


Figure 2. WLCSP2x2-16 land pattern recommendation

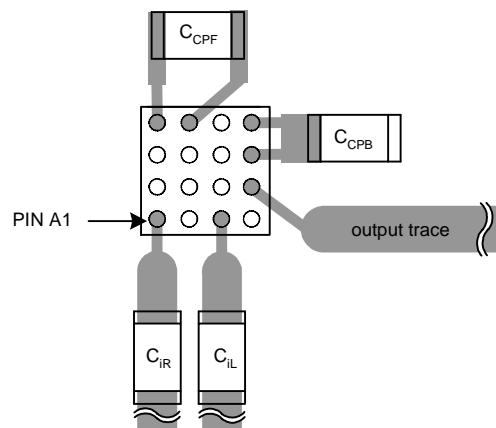
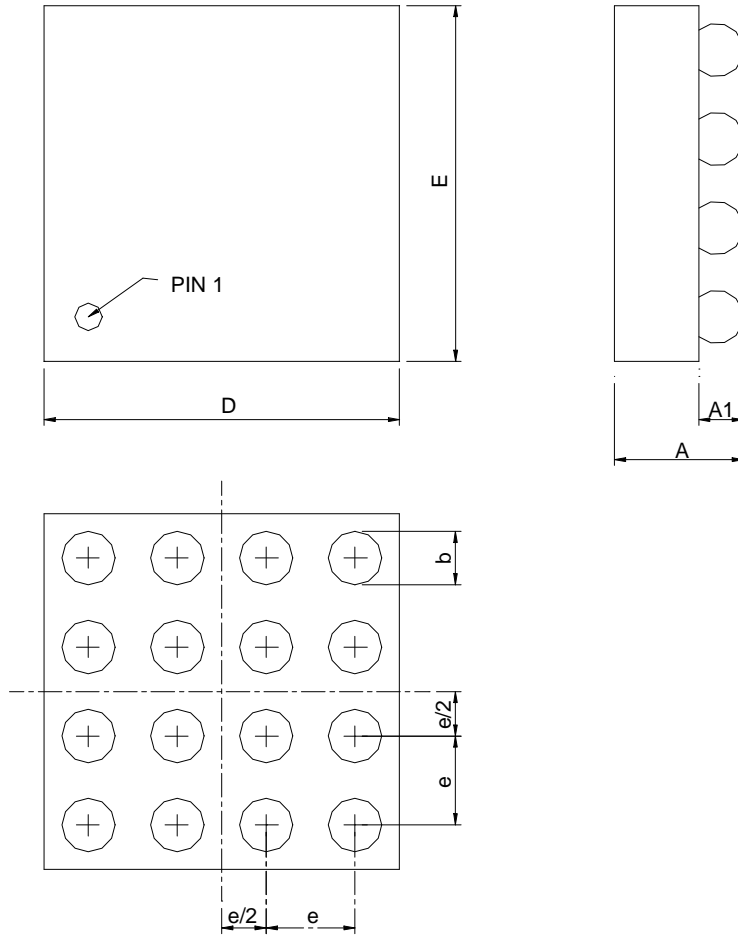


Figure 3. APA2178 Layout Suggestion

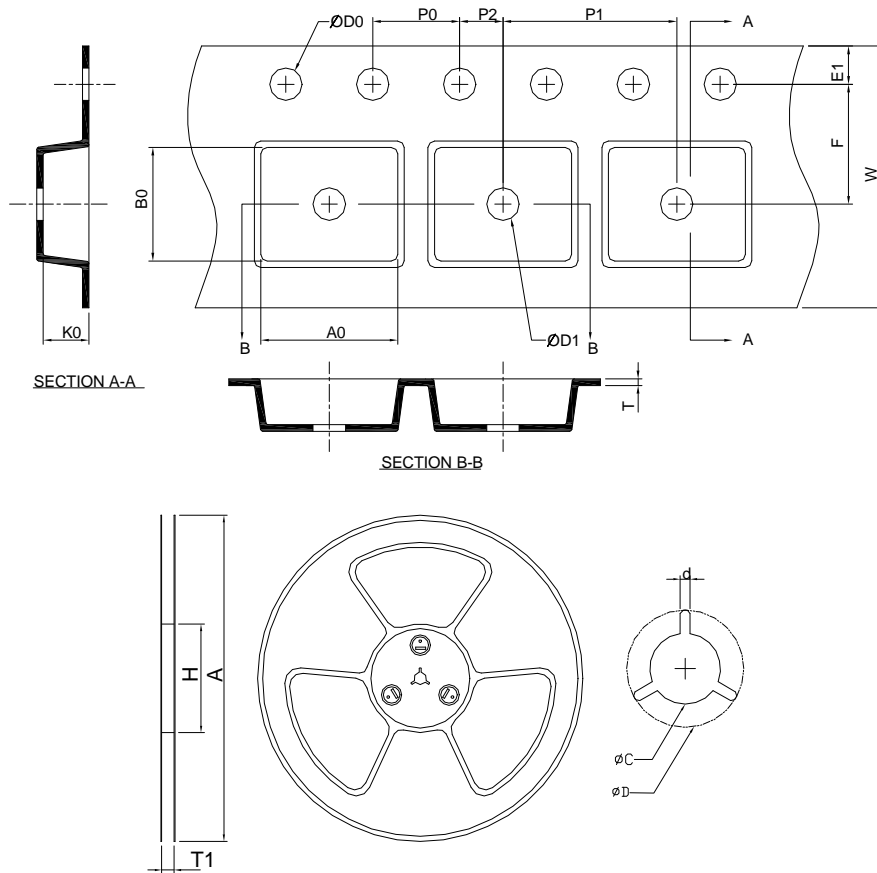
Package Information

WLCSP2x2-16



SYMBOL	WLCSP2x2-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		0.625		0.025
A1	0.15	0.35	0.006	0.014
b	0.25	0.35	0.010	0.014
D	1.97	2.03	0.077	0.080
E	1.97	2.03	0.077	0.080
e	0.50 BSC		0.020 BSC	

### Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP2x2-16	178.0 ±0.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.20 ±0.20	2.20 ±0.20	0.90 ±0.20

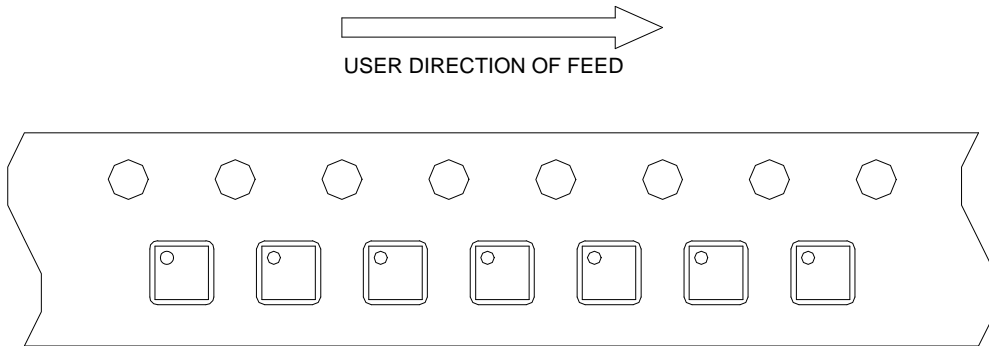
(mm)

### Devices Per Unit

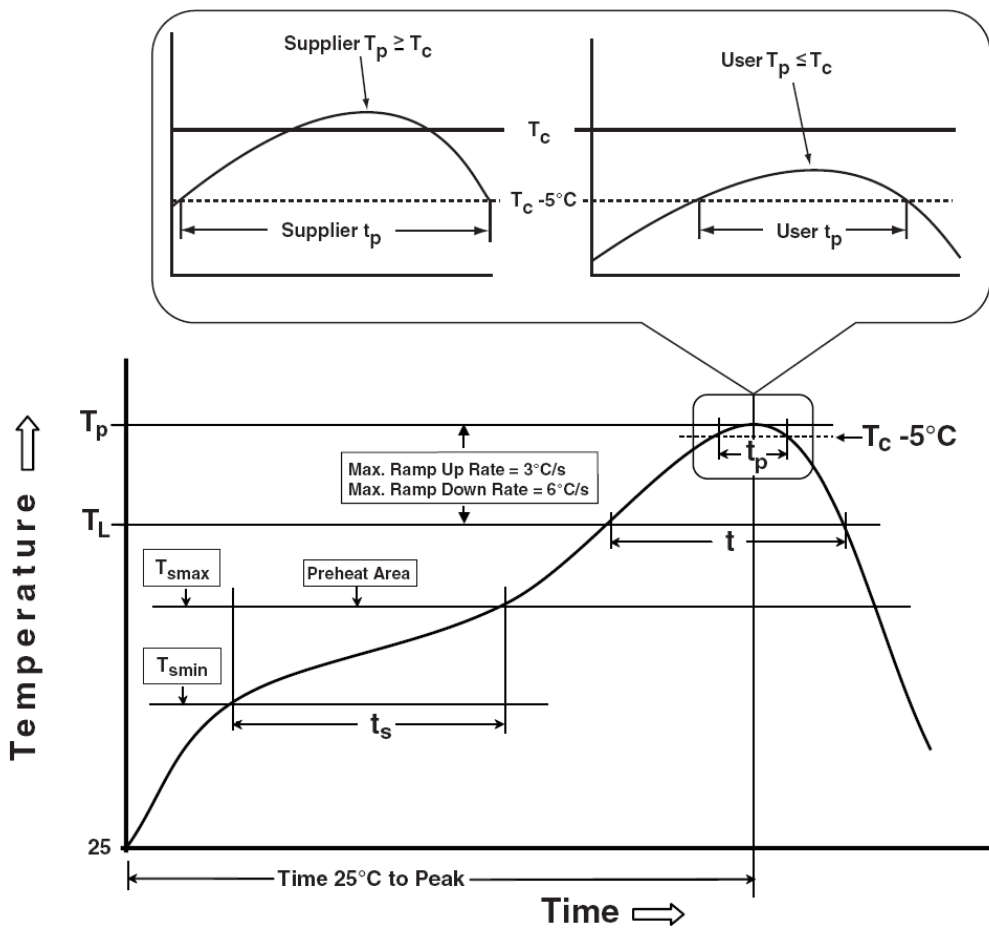
Package Type	Unit	Quantity
WLCSP2x2-16	Tape & Reel	3000

## Taping Direction Information

WLCSP2x2-16



## Classification Profile



### Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

### Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> 100mA

## **Customer Service**

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