SERIES ULN-7000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

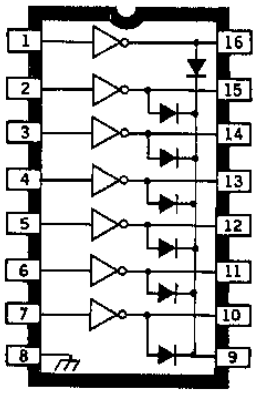
These high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

Series ULN-7001A devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.

Series ULN-7002A is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-7003A has a 2.7 kΩ series base resistor for each Darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs—particularly those beyond the capabilities of standard logic buffers.

Series ULN-7004A has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-7003A, while the required input voltage is less than that required by Series ULN-7002A.

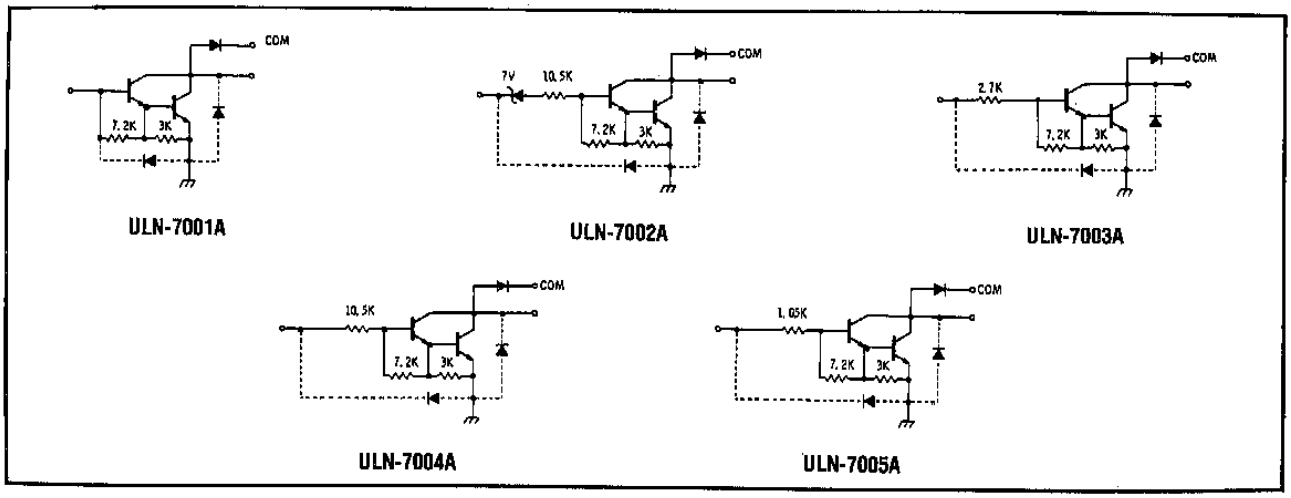


Series ULN-7005A is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 250 mA when driven from a "totem pole" logic output.

Series ULN-7000A is the original high-voltage, high-current Darlington Array. The output transistors are capable of sinking 300 mA and will sustain at least 150 V in the OFF state. Outputs may be paralleled for higher load-current capability.

All Series ULN-7000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These devices can also be supplied in a hermetic dual in-line package for use in military and aerospace applications.

PARTIAL SCHEMATICS



ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} . . . . . 150 V
Input Voltage,
V_{IN} (ULN-7002/7003/7004A) . . . . . 30 V
(ULN-7005A) . . . . . 15 V
Continuous Collector Current, I_C . . . . . 300 mA
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D (total package) . . . . . 2.0 W*
Operating Ambient Temperature Range, T_A . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Derate at rate of 16.67 mW/°C above 25°C.

Device Number Designation

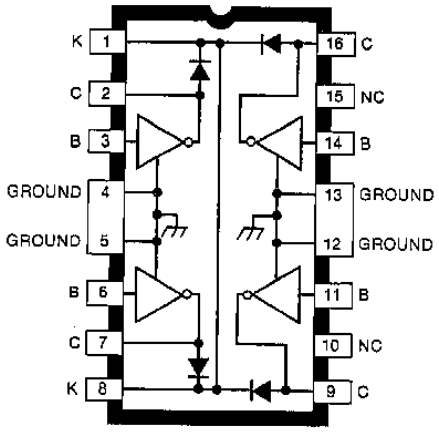
Logic	Type Number
General Purpose PMOS, CMOS	ULN-7001A
14-25 V PMOS	ULN-7002A
5 V TTL, CMOS	ULN-7003A
6-15 V CMOS, PMOS	ULN-7004A
High-Output TTL	ULN-7005A

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	V_{CE} = 150 V, T_A = 25°C	—	—	50	µA
			V_{CE} = 150 V, T_A = 70°C	—	—	100	µA
		ULN-7002A	V_{CE} = 150 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	µA
		ULN-7004A	V_{CE} = 150 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	I_C = 100 mA, I_B = 250 µA	—	1.2	1.3	V
			I_C = 250 mA, I_B = 350µA	—	1.4	1.6	V
Input Current	$I_{IN(ON)}$	ULN-7002A	V_{IN} = 17 V	—	0.82	1.25	mA
		ULN-7003A	V_{IN} = 3.85 V	—	0.93	1.35	mA
		ULN-7004A	V_{IN} = 5.0 V	—	0.35	0.5	mA
			V_{IN} = 12 V	—	1.0	1.45	mA
		ULN-7005A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	ULN-7002A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	13	V
		ULN-7003A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
		ULN-7004A	V_{CE} = 2.0 V, I_C = 100 mA	—	—	5.0	V
			V_{CE} = 2.0 V, I_C = 150 mA	—	—	6.0	V
			V_{CE} = 2.0 V, I_C = 200 mA	—	—	7.0	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	8.0	V
		ULN-7005A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULN-7001A	V_{CE} = 2.0 V, I_C = 250 mA	1000	—	—	—
Input Capacitance	C_{IN}	All		—	15	25	pF
Turn-On Delay	t_{PLH}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	All	V_R = 150 V, T_A = 25°C	—	—	50	µA
			V_R = 150 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 250 mA	—	1.7	2.0	V
Sustaining Voltage	$V_{CE(SUS)}$	All	L = 2 mH; R = 450 Ω	90	—	—	V

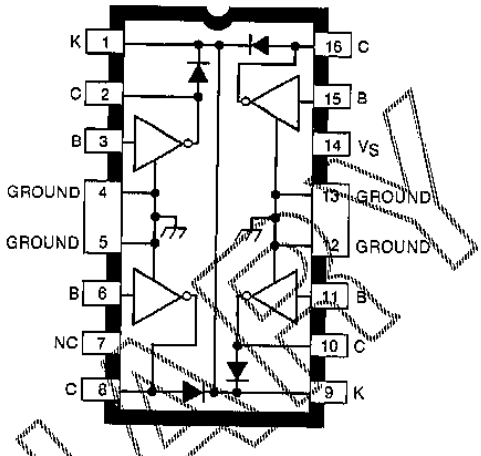
ULN-7064B, ULN-7068B AND ULN-7074B QUAD HIGH-VOLTAGE, 1 A DARLINGTON ARRAYS

ULN-7064B



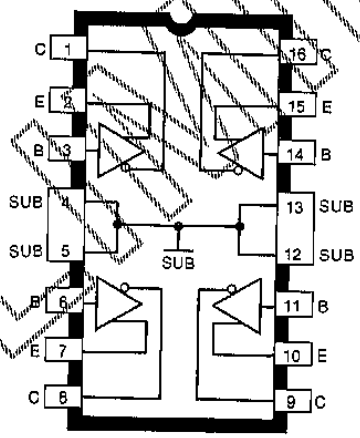
Dwg. No. A-13,669

ULN-7068B



Dwg. No. A-13,670

ULN-7074B



Dwg. No. A-13,671

The ULN-7064B, ULN-7068B and ULN-7074B quad Darlington arrays are high-voltage versions of the industry standard ULN-2064B through ULN-2077B Darlington arrays. The ULN-7064B is the basic driver. Four open-collector Darlingtons feature 150 V minimum breakdowns, 90 V sustaining voltages and integral diodes for inductive load transient suppression.

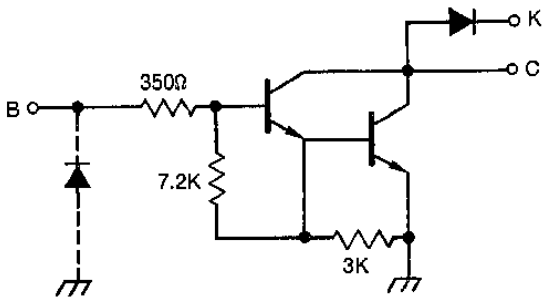
The ULN-7068B includes additional predriver stages for minimum input loading. The ULN-7074B features open emitter outputs for emitter follower or output current sensing applications.

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . . 150 V
Sustaining Voltage, $V_{CE(sus)}$ . . . . . 90 V
Continuous Output Current, I_C . . . . . 1.0 A

PARTIAL SCHEMATICS

ULN-7064B



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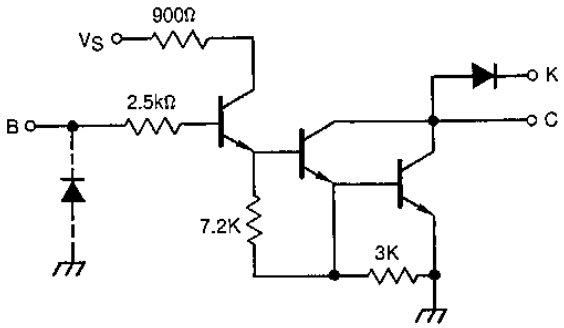
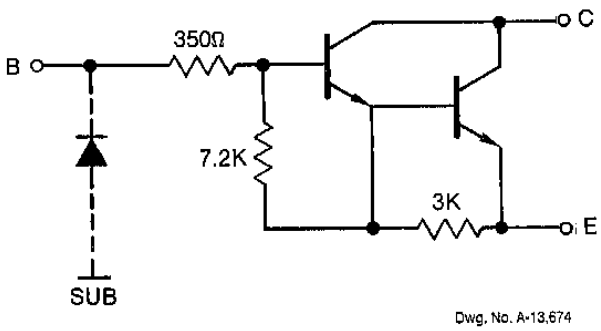
ULN-7068B



Dwg. No. A-13,673

ULN-7074B

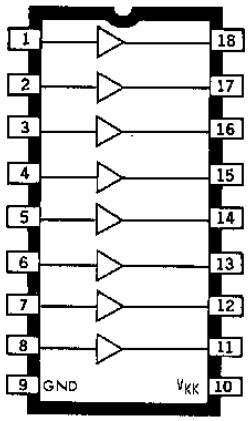


Dwg. No. A-13,674

SERIES UDN-7180A
GAS DISCHARGE DISPLAY SEGMENT DRIVERS

FEATURES

- Reliable Monolithic Construction
- High Output Breakdown Voltage
- Low Power
- TTL/MOS Compatible Inputs



Dwg. No. A-9640A

Description

Series UDN-7180A segment drivers are monolithic high-voltage bipolar integrated circuits for interfacing between MOS or other low-voltage circuits and the cathode of gas-discharge display panels.

These drivers reduce substantially the number of discrete components required with panels (Beckman, Burroughs, Dale, Matsushita, NEC, Pantek, etc) in calculator, clock and instrumentation applications.

The UDN-7183A, UDN-7184A, and UDN-7186A drivers contain appropriate level shifting, signal amplification, current limiting, and output OFF-state voltage bias. The UDN-7180A driver requires external current limiting and is intended for higher-current applications or where individual outputs are operated at different current levels (i.e. with alpha-numeric displays). All inputs have pull-down resistors for direct connection to open-drain PMOS logic.

These devices provide output currents suitable for display segments in a wide variety of display sizes and number of display digits. Either a fixed split supply operation or a feedback-controlled scheme is allowed.

Applications

The Series UDN-7180A drivers can be used in a wide variety of low-level to high-voltage applications utilizing gas discharge displays such as those found in calculators, clocks, point-of-sale terminals, and instruments. Their high reliability combined with minimum size, ease of installation, and the cost advantages of a complete monolithic interface make them the ideal choice in many applications. A typical application showing the use of these devices, and their counterpart anode drivers, is shown.

ABSOLUTE MAXIMUM RATINGS at +25°C

Supply Voltage, V_{KK} ..... −115 V
Input Voltage, V_{IN} ..... +20 V
Output Current, I_{OUT}: UDN-7180A ..... 20 mA
UDN-7183A ..... 3.25 mA
UDN-7184A ..... 2.0 mA
UDN-7186A ..... 1.0 mA
Power Dissipation, P_D ..... 1.13 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at the rate of 9.1 mW/°C above 25°C

Due to the high input impedance of these devices, they are susceptible to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{KK} = 110 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A			UDN-7184A			UDN-7186A			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 2.4 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 2.4 V, V_{KK} = −70 V	1	—	−66	—	—	−65*	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 2.4 V, I_{ON} = 14 mA		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 2.4 V, V_{KK} = −110 V, Test output held at −60 V	3A	* UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, V_{KK} = −110 V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	4	—	100	200	—	100	200	—	100	200	μA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	−125	−175	—	−125	−175	—	−125	−175	μA

NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.
4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

TEST CIRCUITS

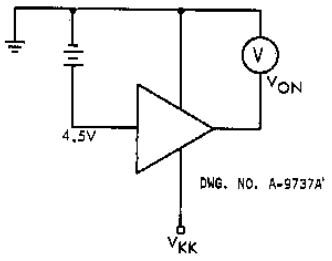


FIGURE 1

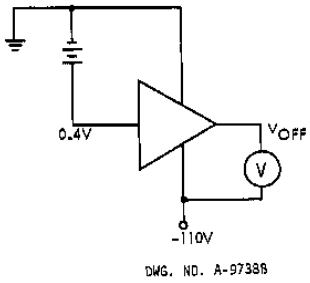


FIGURE 2

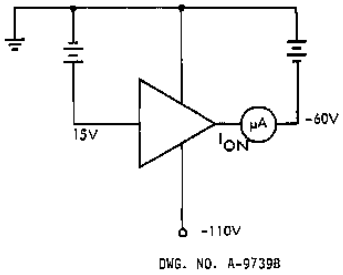


FIGURE 3A

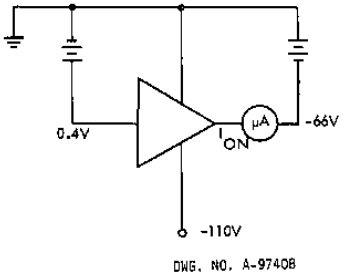


FIGURE 3B

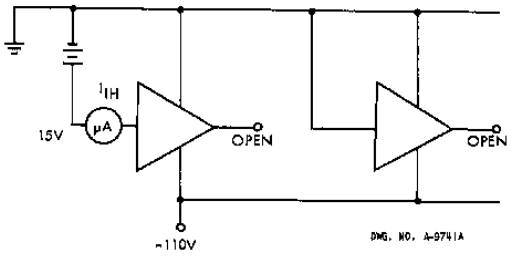


FIGURE 4

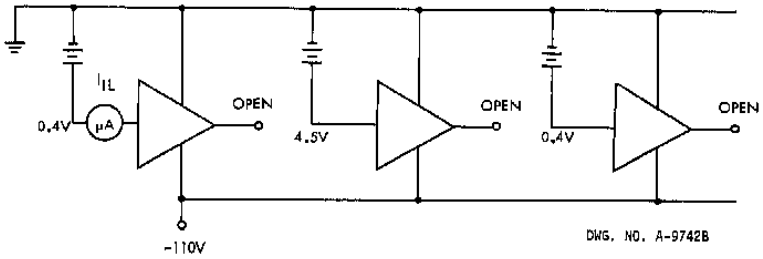


FIGURE 5

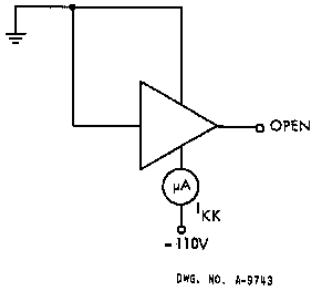
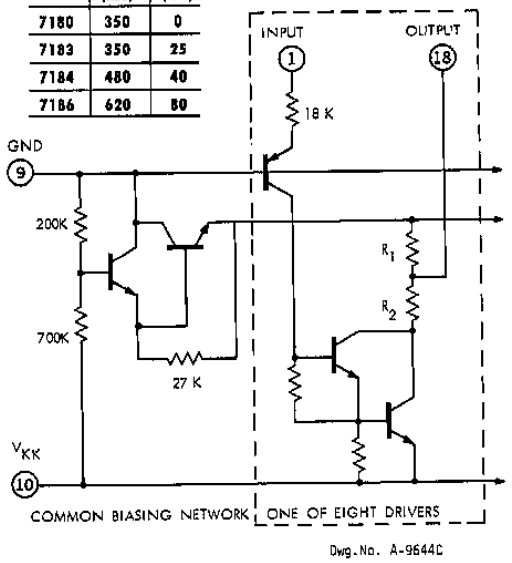


FIGURE 6

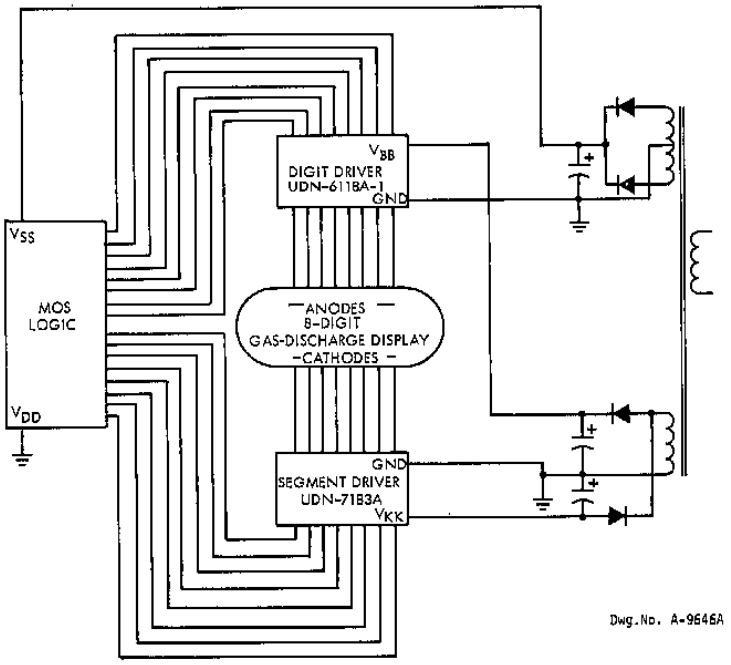
PARTIAL SCHEMATIC

	R_1 (kΩ)	R_2 (kΩ)
7180	350	0
7183	350	25
7184	480	40
7186	620	80



Dwg.No. A-9644C

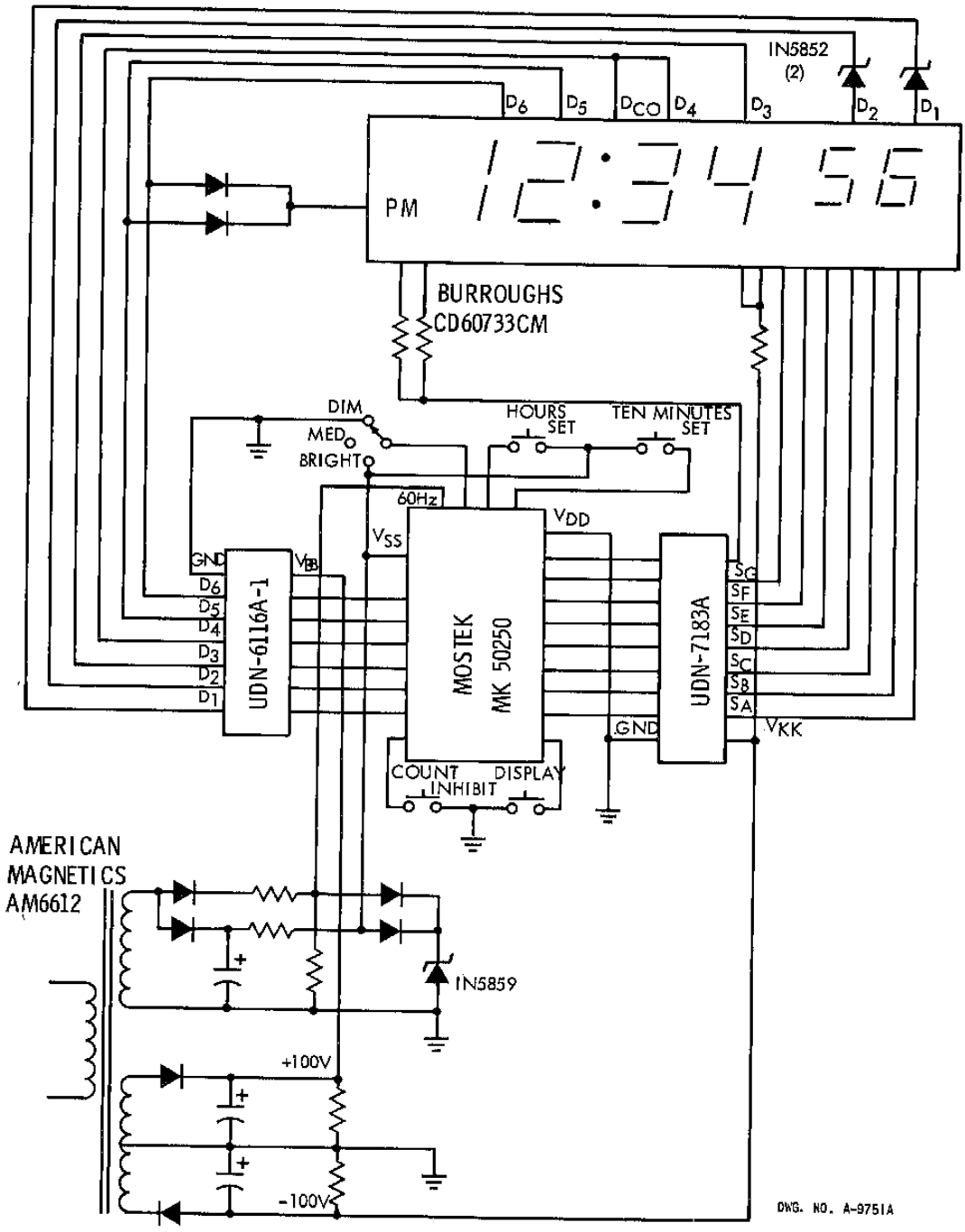
TYPICAL APPLICATION

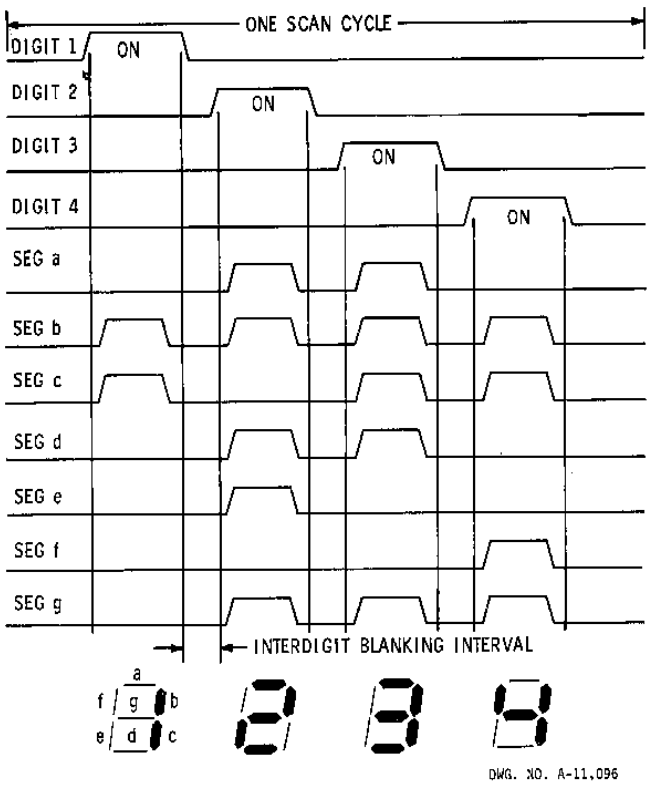


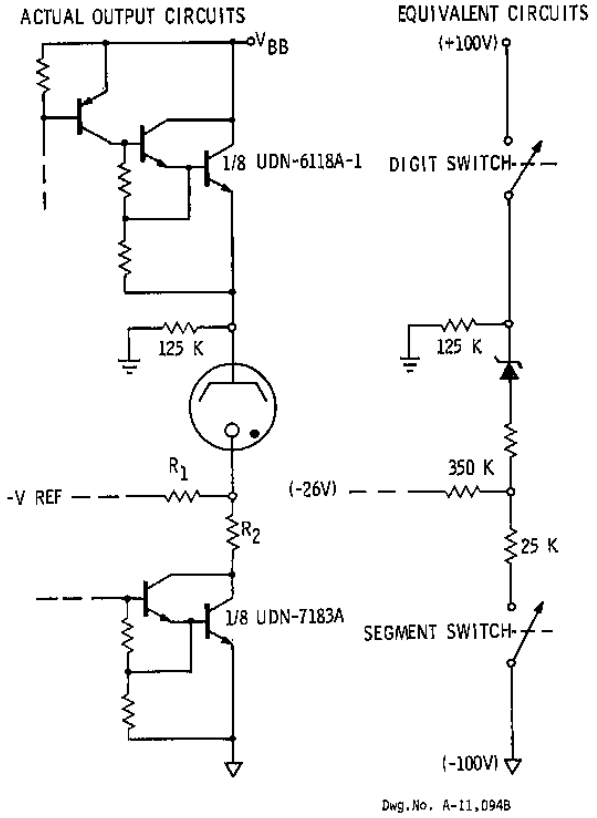
Dwg.No. A-9646A

2

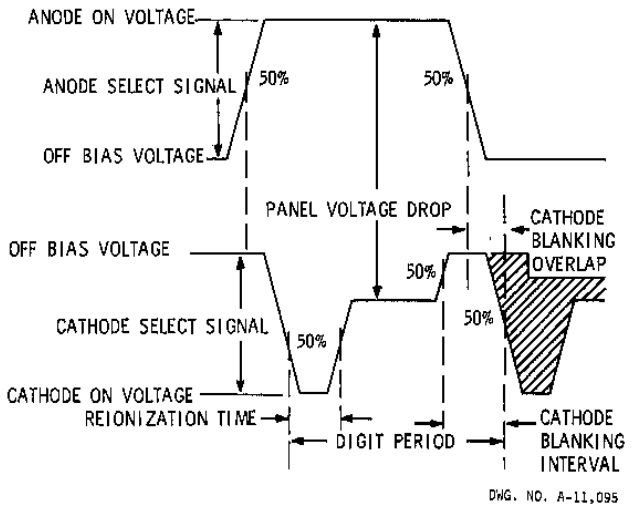
TYPICAL SIX-DIGIT CLOCK







ANODE AND CATHODE WAVEFORMS



A MONOLITHIC IC SERIES FOR GAS-DISCHARGE DISPLAY INTERFACE

Introduction

The switching of the high voltages necessary for display panels such as the Burroughs Panaplex® has long presented difficulties to the semiconductor industry – particularly to IC manufacturers. It is difficult to fabricate devices capable of sustaining 200 volts or greater with standard IC processes of today. Solutions to the high voltage gas discharge display interface also must be inexpensive as well as functional; this cost/simplicity factor prohibits most unusual or exotic circuit designs and/or IC processes.

The earliest (and a great many recent) gas discharge interface schemes used discrete components, but that has been an increasingly cumbersome and expensive solution. Competition at the system level has largely come from LEDs, and a great many standard ICs are available for the smaller LEDs. In most instances, the small displays have gone to LEDs. However, the larger display applications are still an opportunity for gas discharge since character size and cost are not directly related. The cost impact upon the potential for gas discharge displays in many systems is a function of interface complexity and cost, and it was to this end that a joint Sprague/Burroughs effort was launched.

Early Sprague/Burroughs meetings were held to define the relevant factors involved in such a program and provide the necessary insight for both parties into the capabilities of diode isolated ICs, the voltage and current requirements of the Panaplex displays, the need for minimization of power (battery systems), packaging of the circuits, component count and cost, etc. Add to this the potential for use with feedback controlled supplied, poorly regulated d-c supplies, the wide variety of numbers of display digits, the range of digit sizes (in use or contemplated), etc., and our task was not to be an easy one.

Our direction was determined by two factors: a history of fabricating 130-140 volt PN diode isolated display circuits, and a more recent effort to utilize compatible thin-film resistor technology. These factors, coupled with considerable expertise in designing and processing high voltage ICs, dictated an approach utilizing a split (± 100 V) supply. The split supply would provide the 200 volts needed to ionize the display and the resistor capability would greatly aid the incorporation of functions previously done by discrete components – including both input and output (segment) current limiting, pulldown (open drain PMOS), pullup and pulldown reference for IC outputs, and a high impedance voltage divider for the output OFF bias. All level shifting is accomplished via use of PNP or NPN transistors, and the capacitors previously required were negated.

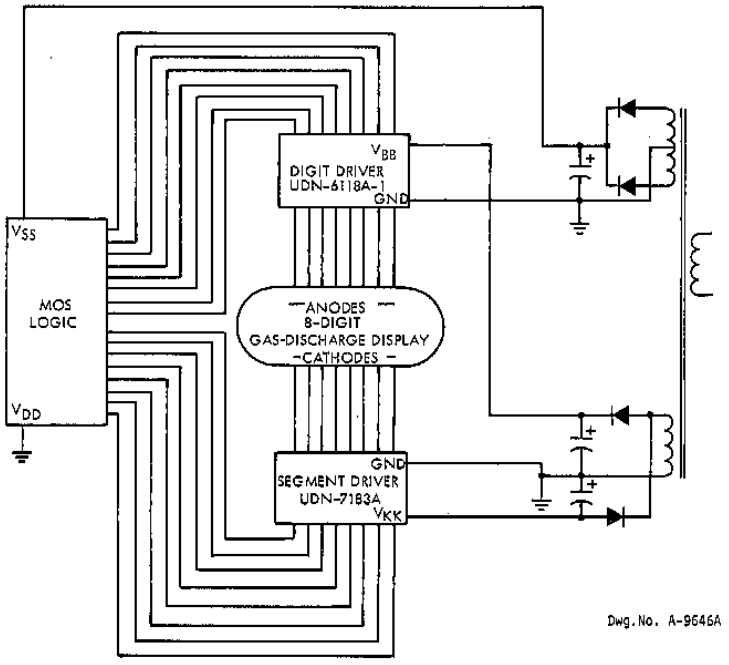


Figure 1

Basic Scheme

Replacing discrete components through incorporating their function into this IC series results in the block diagram of Figure 1 with its basic requirement for a single digit and single segment driver; a scheme capable of driving as many as eight digits and the eight segments. Additional digits or segments beyond the eight provided in an 18-lead DIP may be driven by combinations of packages beyond the minimum two necessary. Example: three ICs—two digit and one segment—will fulfill the needs of a 12 to 16 digit calculator.

Included in this series of high voltage interface are two digit driver packages: UDN-6116 (6-digit), and UDN-6118 (8-digit). Segment drivers include the UDN-7180, UDN-7183, UDN-7184, and UDN-7186, and the four offer current ranges compatible with display sizes from 0.250″ to 1″ panels, and others will be made available as needs are defined.

Digit Interface

The digit driver is the more complex of the two and its schematic is shown in Figure 2. Input address polarity is positive (active high in TTL parlance) and the circuit is designed to interface from TTL (4.5 volts from open collector—or using pull-up to V_{CC}), CMOS, PMOS, etc. Input current-limiting and one-half of the pull-down for open drain PMOS is the function of R_5; R_6 adds the second half of the pull-down to the ground bus. The protective value of R_4 and R_5 must be noted; a junction failure in Q_1 has the two resistors as a current limiter to the MOS (or TTL) output and will minimize the likelihood of destroying the low level logic outputs.

Input transistor Q_4 is a high voltage inverter and sinks the base current of PNP Q_3. A positive input (4.5 to 20 V) will turn on Q_4 and this base current (65 μA typ.) for PNO Q_3 will turn on the output Darlington (Q_1 and Q_2) and source digit current.

ELECTRICAL CHARACTERISTICS: $T_A = +25°C$, $V_{KK} = 110$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	UDN-7180/83A Typ.	UDN-7180/83A Max.	UDN-7184A Min.	UDN-7184A Typ.	UDN-7184A Max.	UDN-7186A Min.	UDN-7186A Typ.	UDN-7186A Max.	Units
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 2.4 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 2.4 V, $V_{KK} = -70$ V	1	—	−66	—	—	−65	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 2.4 V, $I_{ON} = 14$ mA		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 2.4 V, $V_{KK} = -110$ V, Test output held at −60 V	3A	UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, $V_{KK} = -110$ V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	4	—	100	200	—	100	200	—	100	200	μA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	−125	−175	—	−125	−175	—	−125	−175	μA

NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.
4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

PARTIAL SCHEMATIC

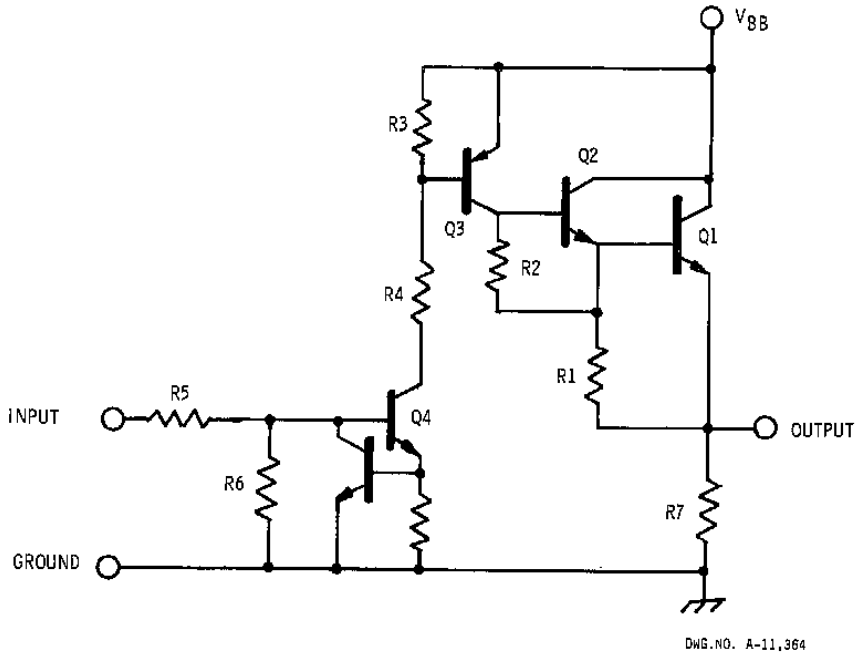


Figure 2

Consistent ionization and extinguishing of the display panel is the result of the 60-75 volt swings available from both digit and segment ICs. The conditions that previously created problems for the direct MOS drive with minimal swings at the output have been very adequately handled with the increased output swings of the 6100/7100 series. Problems from leading zero blanking, low temperature, low ambient light, etc. which previously gave difficulty are well taken care of with this series of ICs.

Segment Interface

The segment driver circuit is shown in Figure 3 and the value of R_2 (segment limiting) is determined via masking for the appropriate display current. Its counterpart pull-up resistor R_1 is also changed to some known ratio of R_2. The ground terminal (#9) is referenced near, or connected directly to ground, and the V_{KK} line is typically a -90 to -100 volts.

The input PNP (Q_1) serves as a level translator and provides d-c level shifting to the output Darlington (Q_2 and Q_3). Emitter resistor (R_3) both limits the input current and furnished pull-down for open drain PMOS. An added intent is the measure of protection furnished the MOS by the very high impedance of R_3.

The basic switching function is the combination of PNP Q_1, Darlington Q_2 and Q_3, and the associated resistors R_1, R_2, and R_3. Address polarity is again active high. The input may be raised a maximum of 20 volts above ground and will function with input levels obtained from CMOS and open collector TTL (4.5 V).

PARTIAL SCHEMATIC

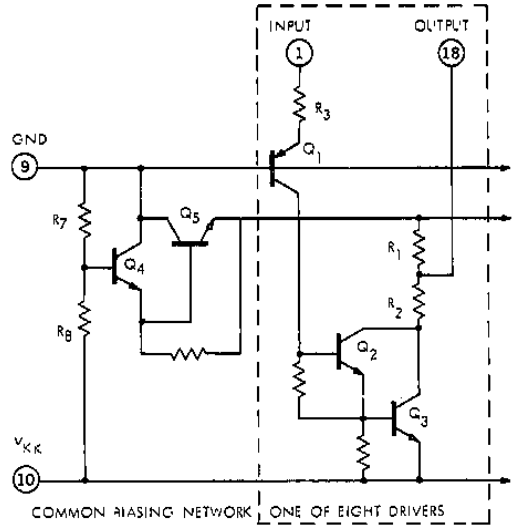


Figure 3

TYPICAL APPLICATION

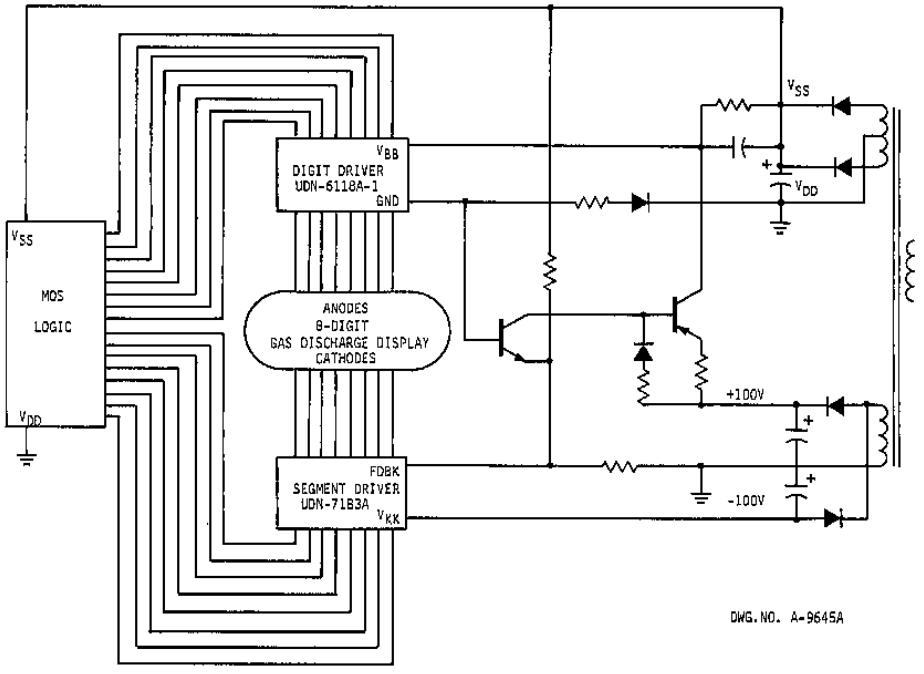


Figure 4

The OFF output biasing network is common to all the individual drivers with the level of bias determined by the ratio of R_7 to the total of R_7 and R_8. As in the digit driver, the value of output bias is ≈⅔ the voltage across V_{KK} and ground—thus insuring sufficient 'on to off' swings to properly fire, and effectively extinguish unaddressed segments during a scan. Emitter follower Q_4 and Q_5 sources current to the pull-up bus connected to the various outputs as they are turned on during the display scan.

Minimum Component Interface

The impact of this new product family may be seen in the typical digital clock of Figure 5. This a-c powered clock uses a Mostek 50250 clock IC, a UDN-6116A-1 digit driver, and a UDN-7183 segment driver. Total component count is approximately 30 pieces, and the board layout is straightforward and uses single-sided board.

Many calculator interface schemes use considerable numbers of components (70 to 100 typically) to drive gas discharge panels. As one example: a twelve digit/eight segment machine uses 85-90 discretes while the new IC version uses only three packages, and results in less space along with considerable simplification. Other applications will benefit similarly with this series of circuits.

Summary

Display technology and usage has emerged at a mind boggling rate in the past several years—largely due to the fantastic growth rate of calculators. The planar gas panels have been an integral portion of this burgeoning market, but like all the other displays

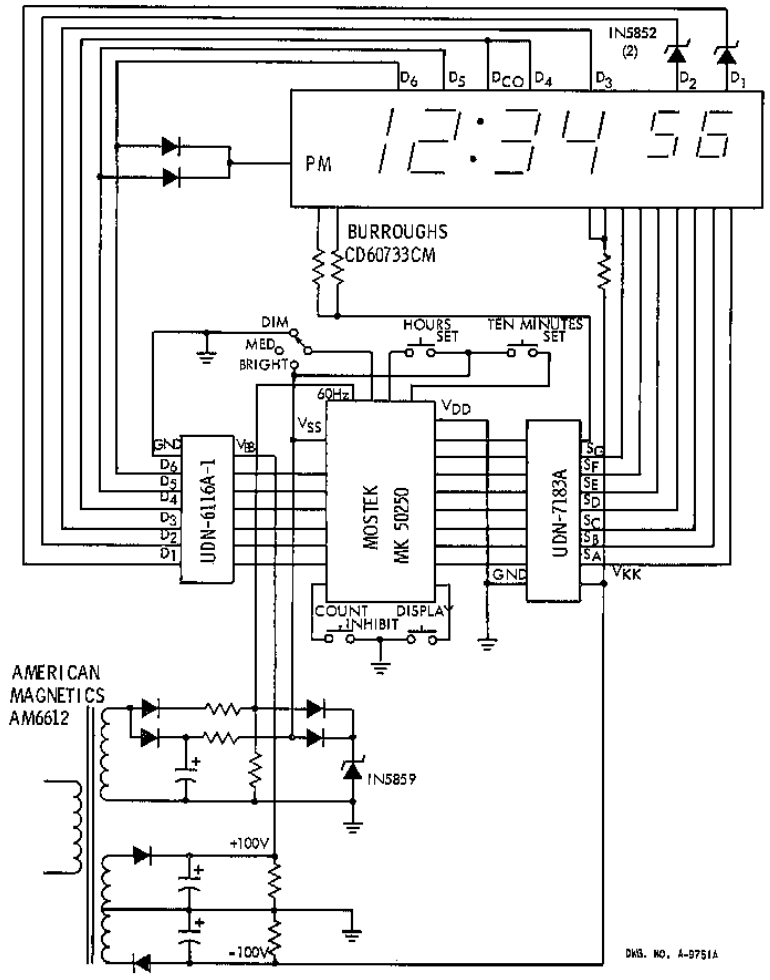


Figure 5

available does not meet the requirements for an ideal display.

Gas discharge panels are a fine combination of aesthetics, reliability, low cost, large character size, multiplexing capability, etc., but have been impacted to some degree by the lack of an available and inexpensive, totally monolithic interface. The move toward IC interface for displays has stifled some potential — largely in favor of LEDs; although many applications requiring large characters and/or in high ambient light turn toward gas panels. The planar gas discharge display is a long way from obscurity, and the availability of this family of ICs should open up new areas as well as satisfying existing systems.

The intent from the inception of this program has been to produce and provide a standard, inexpensive and easy to use interface for gas discharge displays. A great many potential applications exist for these circuits in consumer and commercial products. From the calculator and digital clock areas this product also will find use in automotive dashboards, point-of-sale systems, electronic cash registers and scales, and instrumentation. The market for displays is still very elastic, and many applications for gas discharge panels are continuing to appear. The Sprague contribution to this market is this series of state-of-the-art interface ICs.

TRENDS IN IC INTERFACE FOR ELECTRONIC DISPLAYS

Introduction

Display technology was truly set into high gear by the explosion of the electronic calculator business. Expansion at a phenomenal pace continues, encompassing a multitude of products, particularly high-volume consumer products (calculators, clocks, games, and watches). Recently, further stimulated by the "microprocessor revolution," with its far-reaching effects, and the resulting changeover to solid state design from electromechanical, mechanical, fluidic, or electrical systems, the vistas for displays have expanded well beyond the horizon. Products have been and are being developed, using microprocessors and displays, that never previously existed.

To augment this microprocessor revolution, semiconductor manufacturers are developing many new interface circuits useful with displays, although some of these will not be exclusively for display systems. To accomplish this, the present boundaries of device design, process, packaging, and electrical parameters will require continual extension and expansion.

Display Buffers

A continuing evolution of standard interface ICs is needed to buffer low-level logic from high-voltage and/or high-current loads. Some of this buffer development will serve display systems. Since there already is a broad assortment of buffers (particularly for low- to medium-current LED applications), the ongoing development in simple or low-order interface will mainly concentrate upon further reduction in discrete component count, package improvement (particularly for high-current/high-power devices), improvements in device current, voltage, switching speed, and greater reliability.

Figures 1, 2, and 3 show some Sprague interface ICs that represent buffer circuits; other vendors supply similar, or identical, high-current or high-voltage buffers to allow operation of displays from low-level logic. Two basic changes have occurred relatively recently:

1. Greater use of 18-pin DIPs for eight driver channels (Source Driver, Figure 2).
2. Creation of sourcing functions (Figures 2 and 3; useful for LED, gas-discharge, vacuum fluorescent, incandescent, and electromagnetic displays, depending upon device ratings). While further buffer designs are needed (particularly in high-current (> 2 A) and high-voltage (> 100 V) circuits), the main emphasis will be toward the incorporation of logic and control circuitry with output buffers.

Complex Interface

Paralleling (though lagging) the microprocessor LSI revolution is the area of greatest future for IC display circuits: The need for complex, smart or high-order interface. This will be MSI to LSI logic (with perhaps some linear functions) combined with suitable output buffers.

UDN-6116A-1 GAS-DISCHARGE DRIVER

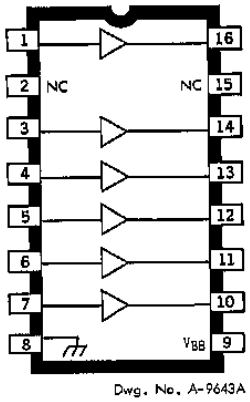


Figure 1A

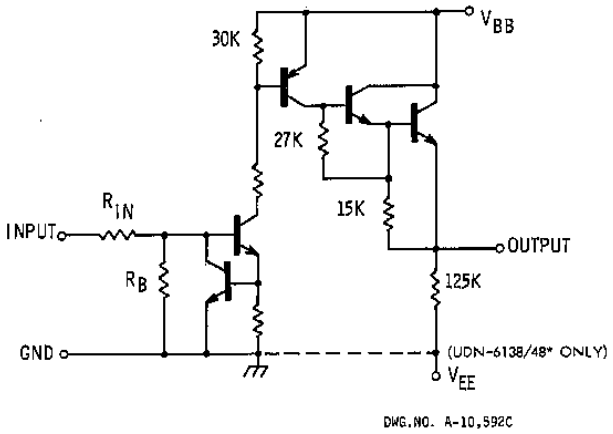


Figure 1B

SERIES UDN-2980 SOURCE DRIVER

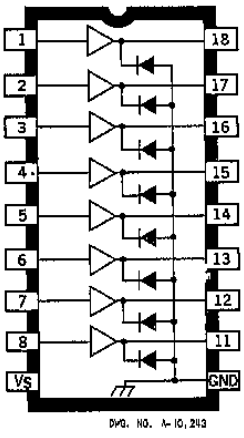


Figure 2A

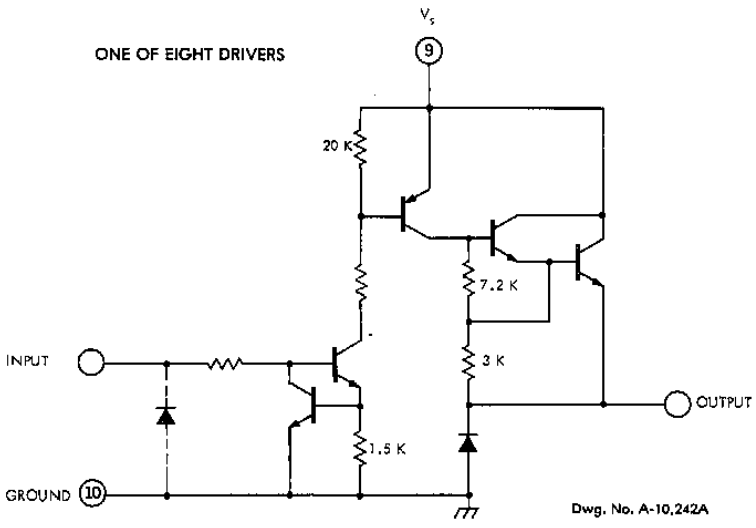


Figure 2B

Display interface ICs (similar to the MOS I/O control chips), both custom and standard product, are becoming available in this category. High-volume applications may justify custom ICs, but the more general trend will be toward standard, off-the-shelf designs — chiefly due to the high costs of developing custom ICs.

The higher voltage displays (gas-discharge, vacuum fluorescent, a-c plasma, and d-c electroluminescent) may share some circuits (if appropriately planned and designed), particularly in the area of matrix displays. It is difficult to imagine, however, much commonality between high-current LEDs, high-voltage gas-discharge or a-c plasma, and low-power LCDs,

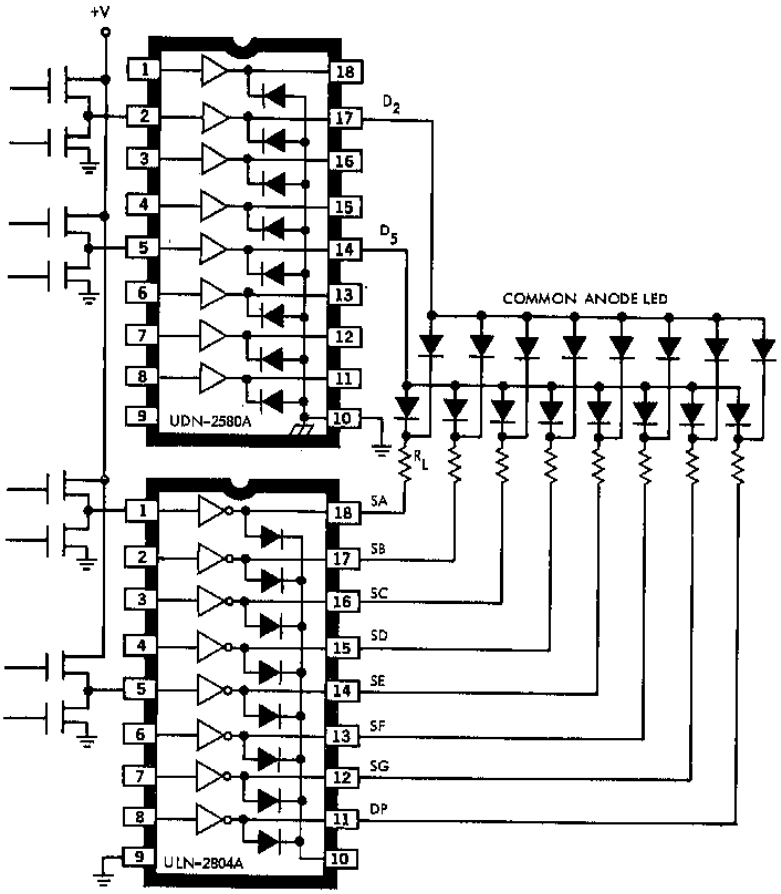


Figure 3
8-DIGIT/8-SEGMENT HIGH-CURRENT LED INTERFACE

although they should share considerably the development of cellular CAD circuit designs. Basic shift registers, latches and decoders do have considerable commonality.

In Figure 4 is a pinout and logic diagram of a BiMOS Sprague IC combining logic and output drive. Although not expressly intended for display applications, this BiMOS (CMOS logic and bipolar outputs) IC has a great deal of utility to engineers working with lower voltages and high currents (LEDs, incandescent and electromagnetic displays). Type UCN-5801A is a parallel-in/parallel-out unit composed of eight 'D' latches and eight 350 mA/50 V bipolar Darlington outputs.

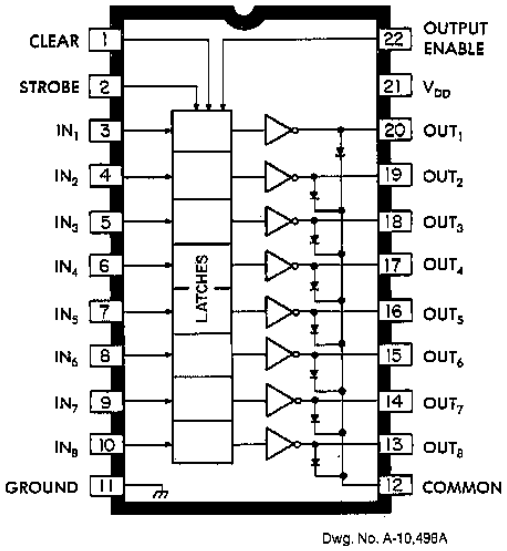


Figure 4A

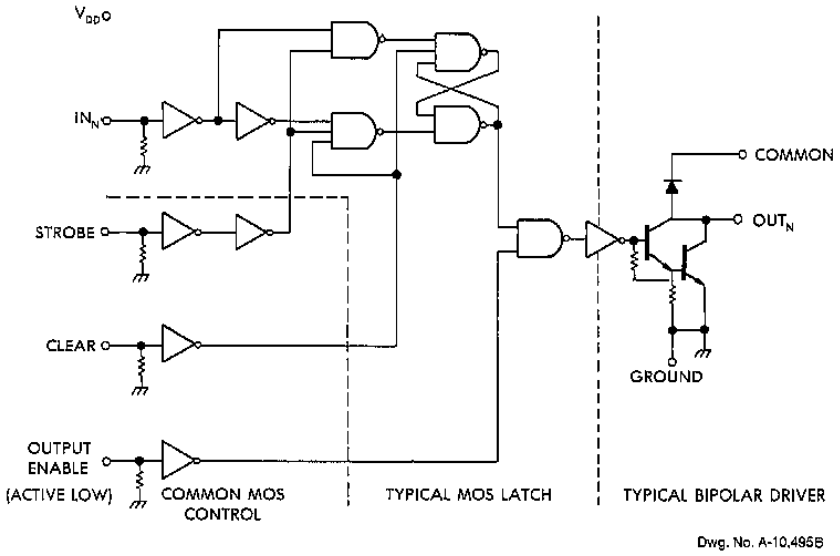


Figure 4B
UCN-5801A BIMOS LATCH/DRIVER

More recently, Sprague has designed a serial-in/parallel-out BiMOS interface IC expressly for use with vacuum fluorescent displays. Figure 5 shows the UCN-5810A 10-bit serial-in/parallel-out interface for use with VF displays; the use of serial data allows 10 output lines, data in and data out in a standard 18-lead DIP. It makes possible both fewer IC packages and simpler PC board wiring, although it is slower than a parallel data approach. It uses only a single pin of the I/O ports.

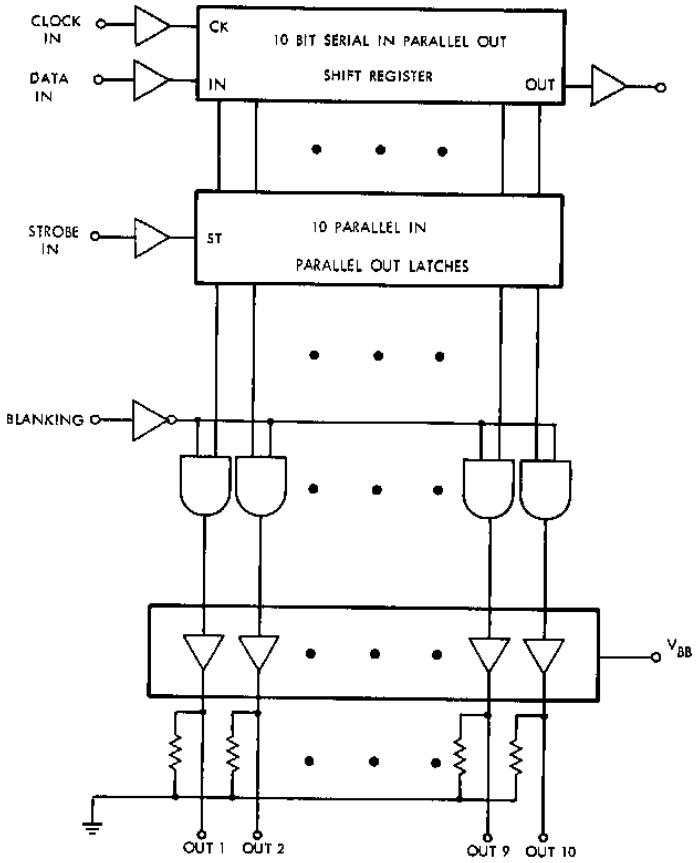


Figure 5B
UCN-5810A VF DRIVER BLOCK DIAGRAM

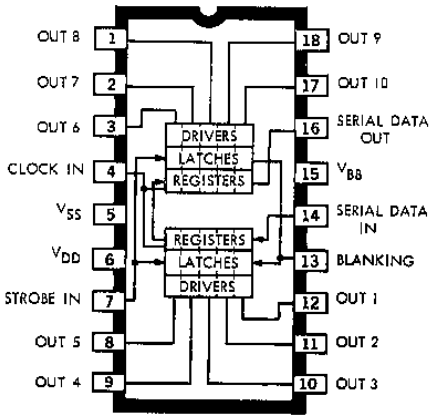


Figure 5A
UCN-5810A PINOUT

A slightly more recent design for vacuum fluorescent displays is the Sprague UCN-5815A. This is a 22-lead, 8-bit parallel-in/parallel-out BiMOS unit. The unit may have data inputs and a strobe bus (see Figure 6). The chip enable/blanking pin provides control of VF buffers. A power-on-clear is internally incorporated.

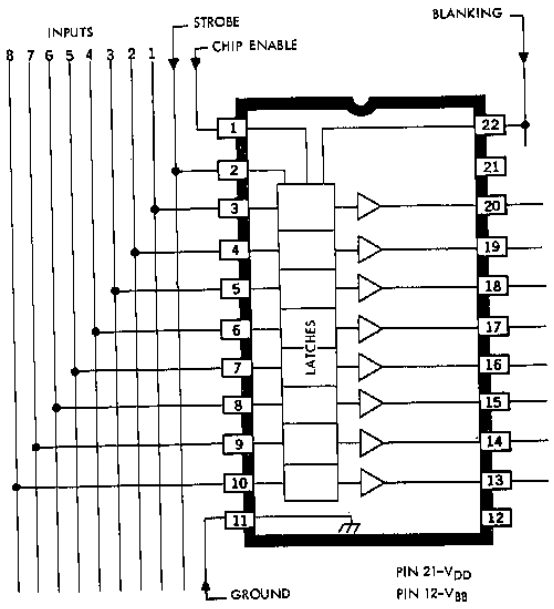


Figure 6
UCN-5815A PARALLEL 8-BIT VF INTERFACE

Device Technologies

With the exception of LCD displays (which at least until recently have been largely, if not entirely, driven by MOS) the display and interface technologies in high-volume use are mainly associated with bipolar semiconductors. Early display interface ICs (particularly devices such as the 7447 and 7448) were aimed at LED technology and represent MSI with modest output capability. The increasing use of higher voltage displays, multiplexed high-current applications, and the need for greater circuit complexity and low pin count will dictate other technologies, such as I^2L, BiMOS, CMOS/DMOS, and possibly DMOS.

Standard Bipolar

Standard bipolar technology, long associated with TTL or linears (early op amps), appears very limited in scope for the future. Circuit density and supply power requirements will dictate other processes for functions beyond the simple MSI level. The advantages of standard bipolar ICs appear to be in the areas of simple high-current, high-power or high-voltage interface. In particular, applications requiring the combination of high voltages ($\geq$ 100 V) or multiple high-current outputs ($\geq$ 2 A) will restrict the logic/control circuitry to a low level. Cost, chip size and package power dissipation will restrict this circuitry largely to versatile, simple buffers.

I^2L

Anticipated to increase significantly is the use of I^2L for systems of low to modest voltages (LEDs through VF). The present limits of I^2L appear to be limited to applications below the 50- to 60-volt level. I^2L, with its combination of circuit density, low power and reasonable switching speeds should make a fine match for LEDs or other low-voltage display applications. For higher voltages (> 25 or 30 V), prospects the penalty of reduced circuit density may diminish its cost effectiveness. Some increase in standoff voltage may be afforded by the uses of cascaded output transistors or process improvements, thus reducing the need to sacrifice logic density. Without a standard I^2L logic family, the main market penetration would appear to be custom designs although there is a definite opportunity for standard interface for lower voltage applications, particularly LEDs and vacuum fluorescent.

BiMOS

BiMOS, a combination of CMOS and bipolar for interface ICs, seems to fit a technology niche of higher breakdown voltages than I^2L, especially where logic power and supply voltage range (5 to 15 V) is important. BiMOS or BiFET ICs, which are presently on the market, are largely related to operational amplifiers, although other uses, such as the Sprague application of BiMOS to interface, are emerging.

Currently, it is feasible to design and manufacture BiMOS interface with breakdown voltages in the 80 to 100 V range. With additional time and greater concentration on increasing BV, it appears that higher voltages ($\geq$ 150 V) for output buffers could be obtained. By obtaining breakdowns in the 120 V to 160 V range, BiMOS then becomes a viable IC technology for interface for the higher voltage displays: d-c gas-discharge with $\pm$100 to $\pm$130 V; a-c plasma with 160 to 170 V, and glow transfer or d-c electroluminescent (DCEL) opportunities with a range of 120-150 volts.

Switching speeds and output configurations (active pull-down or resistive) are critical to matrix displays (particularly a-c plasma) with large numbers of drive lines. Adding active pull-down or pull-up will tend to increase chip size (and cost), thus adding to the potential overall difficulty of BiMOS with its greater process complexity and slightly longer manufacturing cycle. This does appear to be a very key technology for the near future. Its product niche will include for applications requiring 60 to 100 V (or more) breakdowns, low-power logic, wide supply range, modest speeds, and MSI to small LSI.

CMOS/DMOS

Chiefly being carried on by Texas Instruments, CMOS/DMOS display interface appears to be intended for much of the same display market as BiMOS. Product information now available indicates 60 to 100 V breakdown (DMOS outputs), CMOS logic, low to modest output currents ($\leq$25 mA), and logic speeds to 4 MHz. Designs now being promoted are targeted toward a-c plasma and vacuum fluorescent panels.

Two apparent disadvantages now appear to exist:

1. Logic operates from 12 V $\pm$10% (may be done to provide maximum speed).
2. Output drive current is insufficient for high-current displays (without 100 mA, or more, the larger matrix panels will use discretes or another technology).

These shortcomings may be modified with time, although it is doubtful if 500 mA to 1 A DMOS outputs are practical.

Dielectric Isolation

Affording the highest breakdown voltage capability of present technologies is dielectric isolation. Since there is no collector-to-substrate PN junction, nor a collector-to-isolation wall PN junction, considerable improvement in collector-to-base and collector-to-emitter voltage is possible. Additionally, transistor sizes are considerably smaller than their PN-isolated counterparts. The dielectrically isolated devices offered by Dionics span a spectrum of approximately 100 volts to 280 volts (a-c plasma driver). DI affords the maximum breakdown voltage capability currently available.

Opposing this great advantage in breakdown voltage, however, is the increased process complexity of dielectrically isolated ICs. Definite improvements are needed in the area of process simplification, cost reduction, and alternate sources. Large-volume use of DI circuits will be restrained until these problems (particularly alternate sources) can be overcome. DI interface, with its potential for 300 V transistors, has a great promise if the barriers can be overcome.

Packaging

Semiconductor design and process have greatly outstripped packaging currently in use, particularly the area of power-handling capability. Greater concentration and resources are required to solve some of the following display interface related problems:

1. DIP power dissipation.
2. Greater number of leads (and smaller package sizes).
3. Improved plastic DIP resistance to moisture and corrosive environments.
4. Lower package manufacturing costs.
5. Smaller module or display subassemblies.

Power dissipation difficulties (strobed high currents) are most associated with LEDs. Use of very low duty-cycle and bright LEDs (particularly alphanumeric and matrix) dictates a need for multiplexing with peak currents as high as 3 A. Nothing currently on the market exceeds 1.75 A per output, and DIP ratings preclude d-c operation at such currents. However, many of the high-current applications are within the capability of standard bipolar ICs now offered.

For LSI ICs containing many I/O lines, the 24-, 28-, and 40-lead DIPs are standard. Since package size and cost increase together, it may be desirable to constrain many newer ICs to 18-, 20-, or 22-lead DIPs (with 0.300″ spacing, 22 also in use with 0.450″ width). Printed wiring board real estate is increasingly dictating smaller size. Solutions such as the quad in-line (Rockwell) or less than 0.100″ centers are possible. There are problems associated with a non-standard configuration (lack of sockets and higher prices) and the smaller physical size will not aid the quest for higher power (LEDs).

Improvements in plastic DIP moisture resistance and reliability are already underway; uses of tri-metal schemes (such as RCA's), silicon nitride or quartz passivation will continue to improve resistance to moisture and corrosive fumes. For display applications, these reliability improvements are of greatest concern in high-voltage devices.

Lower package costs are necessary to further increase the use of ICs in areas such as flat panel matrix displays. Currently, much of the cost of such a system is related to drive electronics, and much of the cost of the interface is the assembly cost of the DIPs (or hybrids). Increased use of automated assembly, film-carrier techniques and solder bumps will enhance the choice of ICs over discretes, and flat panel over CRT.

Also of concern is the possible mating of IC chips, solder-bump chips, or film-strip chips into the display assembly. Candidates for such a treatment would include d-c and a-c plasma, LEDs (already being done to a degree), DCEL, ACEL, LCD, and VF. Panel technologies using thick or thin-film techniques could benefit from such an approach. The biggest barrier to such an integrated assembly is the market data needed to justify tooling and lead time. It will only require one manufacturer willing to be a pioneer to further swing display technology into integrated systems. Prospects for purchasing a display complete with all drive electronics, such as a flat panel a-c plasma matrix (chips mounted via hybrid techniques on the rear of the glass envelope), are improving with time.

Summary

A bright future exists for IC interface in display systems; the combination of logic (from MSI to small LSI) with suitable output buffers will further assist display designs. The following IC Technology-Display Interface matrix lists the key characteristics and primary display applications of various semiconductor technologies. Since many of these characteristics are changing, the table lists the device characteristics either now available or for the near future.

The most dynamic technologies for the immediate future appear to be BiMOS, I^2L, CMOS/DMOS, and, perhaps soon, DMOS. Sprague, Dionics, RCA, Texas Instruments, National Semiconductor, and others are using these device technologies to carve market niches where suitable. The dynamics of the IC market make for an uncertain future for any supplier of display circuitry unable or unwilling to continue the technological advancement necessary to meet the changing demands of the display market.

IC TECHNOLOGY — DISPLAY INTERFACE

Technology	Breakdown V	Output 1	Speed	LOGIC			Primary Display Suitability
				Complexity (max)	Supply Range	Supply Power	
Linear Process Bipolar	10 to −170 V	<10 mA to 2 A	<1 MHz	MSI	5 V	High	LEDs, GD, VF, ACP, DCEL, EM
I^2L	20 to −60 V	<10 mA to 2 A	3-6 MHz	LSI	5 V	Low-Modest	LED, VF, EM
BiMOS	50 to −150 V	<10 MA to 500 mA	2-5 MHz	LSI	5 to 15 V	Low	LED, GD, VF, ACP, DCEL, EM
CMOS/DMOS	60 to −100 V	−25 mA	2-4 MHz	LSI	12 V	Low	GD, VF, ACP, LCD
DI	−200 to −300 V	<10 mA to 100 mA (est)	1 MHz (est)	MSI	5 V	High	GD, VF, ACP, DCEL

Code: GD = D-C Gas-Discharge & Glow Transfer
ACP = A-C Plasma
VF = Vacuum Fluorescent
DCEL = D-C Electroluminescent
EM = Electromagnetic

RELIABILITY OF SERIES UDN-6100A HIGH-VOLTAGE DISPLAY DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series UDN-6100A integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.
2) Accelerated testing is performed at temperatures above +125°C and is used to generate failure-rate data.
3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Table I contains Series UDN-6100A data produced by life tests that were conducted at +150°C. The data includes the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C. If these tests had been qualification tests, they would have ended at 200 hours at +150°C or 40 hours at +175°C.

The data at the bottom of Table I is compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% fail-point. The median life at a junction temperature of +150°C is 100,000 hours, in this case.

The log-normal distribution is commonly and widely used, because most semiconductor device data fits such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^{\circ} e^{-\varepsilon/kT}$$

where V_r° = a constant
ε = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5700M, and Series UDN-2980A devices at multiple temperatures. Failure analysis of devices rejected during the testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

TABLE I
TEST RESULTS AT T_J = +150°C

TEST NUMBER	BIAS VOLTS	QTY.	HOURS ON TEST: 90	150	300	600	1200	1800	2000	5000	6000
			NUMBER OF FAILURES								
1	80	24	0	0	2	—	—	—	—	—	—
2	80	24	0	0	0	0	0	0	1	0	—
3	80	12	0	0	0	0	0	—	—	—	—
4	80	12	0	0	0	0	2	1	1	0	0
5	110	24	0	0	0	0	0	0	1	—	—
6	80	12	0	0	0	—	—	—	—	—	—
TOTAL ON TEST			108	108	108	72	72	58	57	31	8
TOTAL FAILURES			0	0	2	0	2	1	3	0	0
TOTAL GOOD			108	108	106	72	70	57	54	31	8
P_s			1.00	1.00	0.981	1.00	0.972	0.983	0.947	1.00	1.00
Cumulative P_s			1.00	1.00	0.981	0.981	0.954	0.938	0.888	0.888	0.888
$P_f = 1 - P_s$			0	0	0.019	0.019	0.046	0.062	0.112	0.112	0.112
% Failures			0	0	1.9	1.9	4.6	6.2	11.2	11.2	11.2

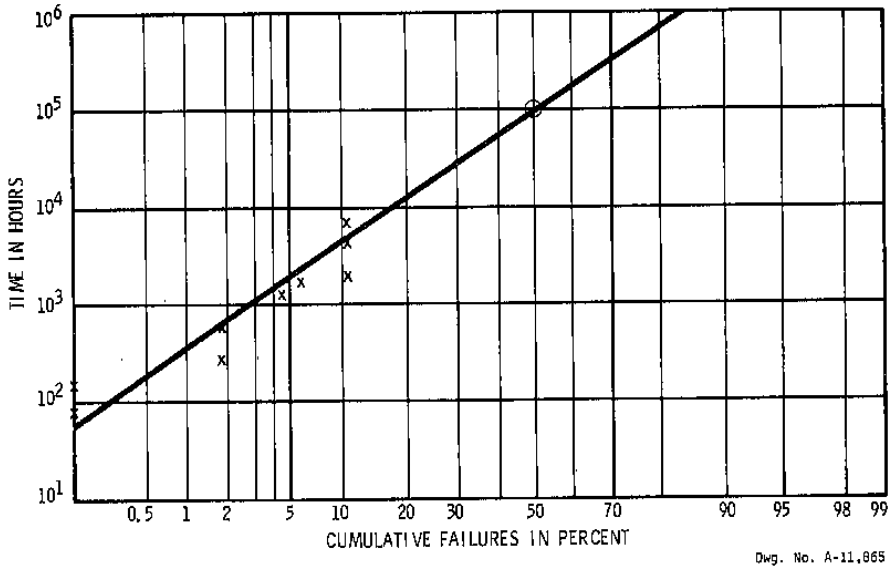


Figure 1
CUMULATIVE PERCENT OF FAILURES

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of $\varepsilon = 1.0$ eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life with lower junction temperatures may now be determined using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\Theta_{JA} + T_A$$

or

$$T_J = P_D\Theta_{JC} + T_C$$

The median lifetime, or 50% fail-point, as determined in Figure 2, is approximately 100 years at +125°C or 1,000 years at +90°C junction temperature.

The approximate failure rate ($\overline{FR}$) may be determined from $\overline{FR}$ = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$\overline{FR} = 1/(4 \times 10^6 \text{ hours})$$
$$= 0.025\%/1000 \text{ hours}$$

Other failure rate values have been calculated in Table II.

TABLE II
SERIES UDN-6100A FAILURE RATES

T_J (°C)	Median Life (h)	Failure Rate (%/1000 h)
125	6×10^5	0.167
100	4×10^6	0.025
75	4×10^7	0.0025
50	5×10^8	0.0002

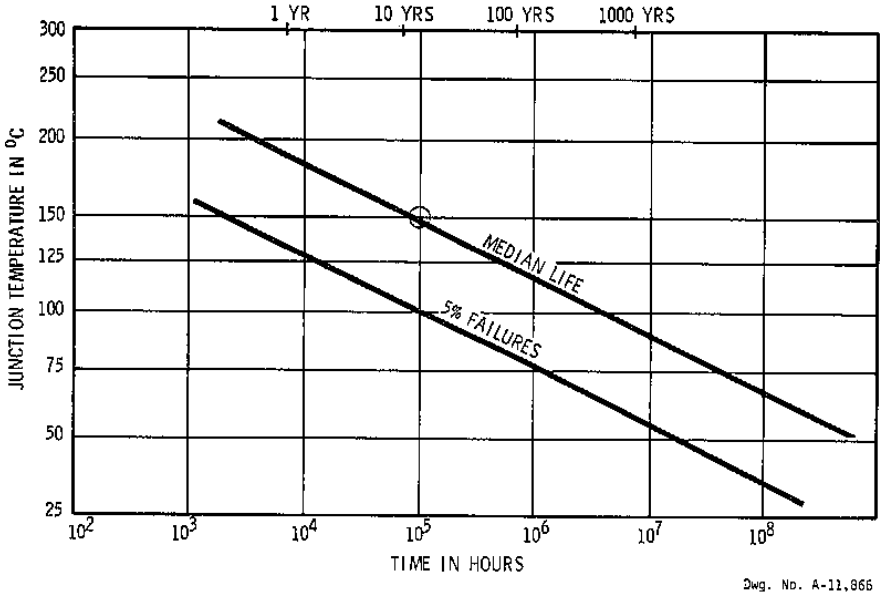


Figure 2
MEDIAN LIFE

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calculated from internal power dissipation and external ambient temperature, reaches the 5% fail-point in 10 years. Lowering the junction temperature to +70°C increases the time to 100 years.

A complete sequence of environmental tests on Series UDN-6100A, including temperature cycle, pressure cooker, and biased humidity tests are also continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

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1) Manchester, K.E., and Bird, D.W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580–587 (Sprague Technical Paper TP 80-2).

2) Peck, D.S., and Trapp, O.D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6–7.

4) Goldwaite, L.R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208–213.