TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J114TU

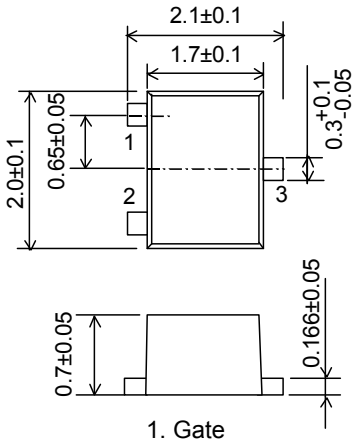
○ High-Speed Switching Applications

○ Power Management Switch Applications

- 1.5 V drive
- Low on-resistance

R_{on} = 526 mΩ (max) (@ V_{GS} = -1.5 V)
R_{on} = 321 mΩ (max) (@ V_{GS} = -1.8 V)
R_{on} = 199 mΩ (max) (@ V_{GS} = -2.5 V)
R_{on} = 149 mΩ (max) (@ V_{GS} = -4.0 V)

Unit: mm



UFM	
JEDEC	—
JEITA	—
TOSHIBA	2-2U1A

Weight: 6.6 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	-20	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-1.8	A
	Pulse	I_{DP}	-3.6	
Drain power dissipation		P_D (Note 1)	800	mW
		P_D (Note 2)	500	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	−55 ~ 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on ceramic board
(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm2)

Note 2: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

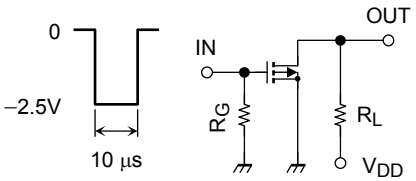
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−20	—	—	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = +8 V	−12	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	—	—	−10	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 8 V, V_{DS} = 0	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −1 mA	−0.3	—	−1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -0.6 A (Note 3)	1.9	3.9	—	S
Drain-Source ON-resistance		$R_{DS\ (ON)}$	I_D = -0.6 A, V_{GS} = -4.0 V (Note 3)	—	100	149	mΩ
			I_D = -0.6 A, V_{GS} = -2.5 V (Note 3)	—	133	199	
			I_D = -0.6 A, V_{GS} = -1.8 V (Note 3)	—	183	321	
			I_D = -0.1 A, V_{GS} = -1.5 V (Note 3)	—	220	526	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 f = 1 MHz	—	331	—	pF
Output capacitance		C_{oss}		—	48	—	pF
Reverse transfer capacitance		C_{rss}		—	39	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.6 A	—	19	—	ns

	Turn-off time	t_{off}	V_{GS} = 0 ~ –2.5 V, R_G = 4.7 Ω	—	18	—	
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge		Q_g	V_{DS} = –16 V, I_{DS} = -1.2 A, V_{GS} = – 4 V	—	7.7	—	nC
Gate-Source charge		Q_{gs}		—	4.9	—	
Gate-Drain charge		Q_{gd}		—	2.8	—	
Drain-Source forward voltage		V_{DSF}	I_D = 1.8 A, V_{GS} = 0 (Note 3)	—	0.8	1.2	V

Note 3: Pulse test

Switching Time Test Circuit

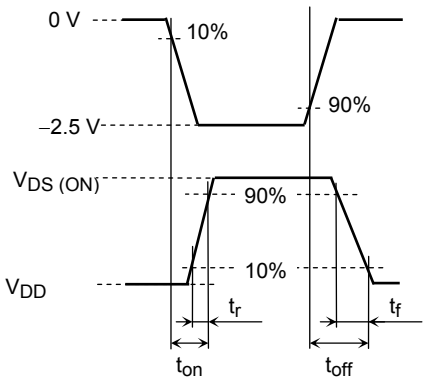
(a) Test Circuit



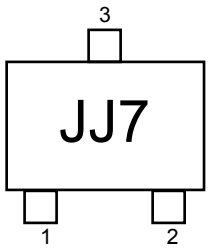
V_{DD} = -10 V
R_G = 4.7 Ω
D.U. ≦ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25 °C

(b) V_{IN}

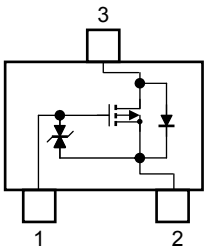
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



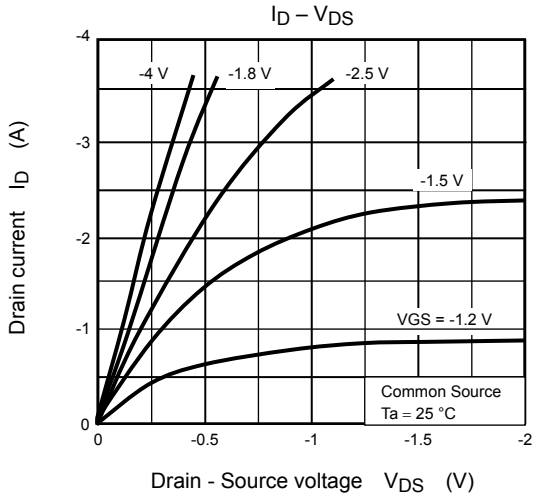
Precaution

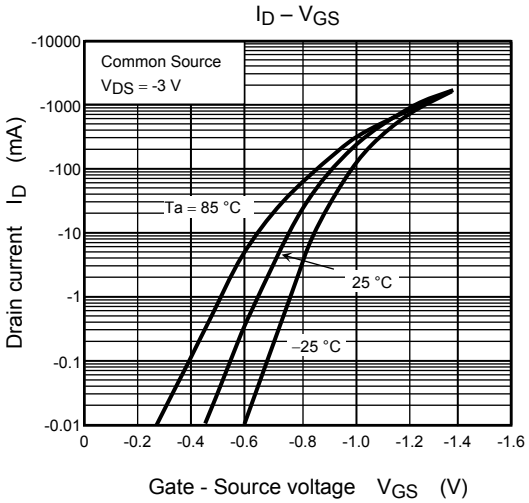
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = -1mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

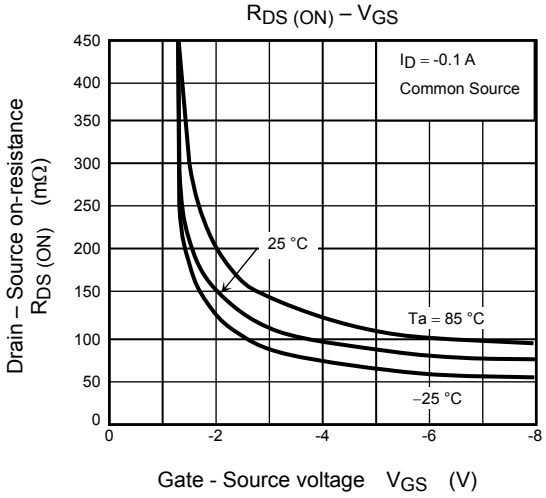
Be sure to take this into consideration when using the device.

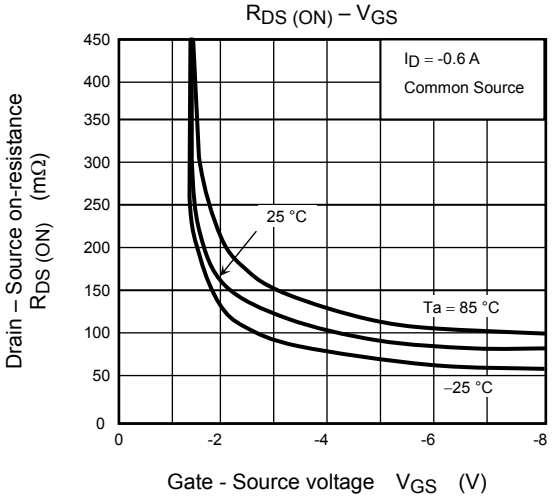
Handling Precaution

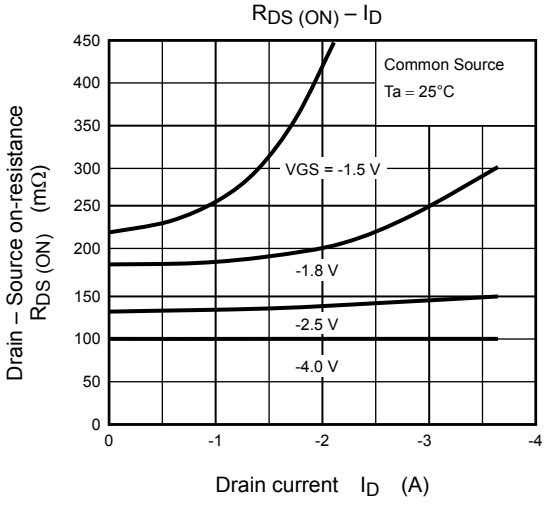
When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

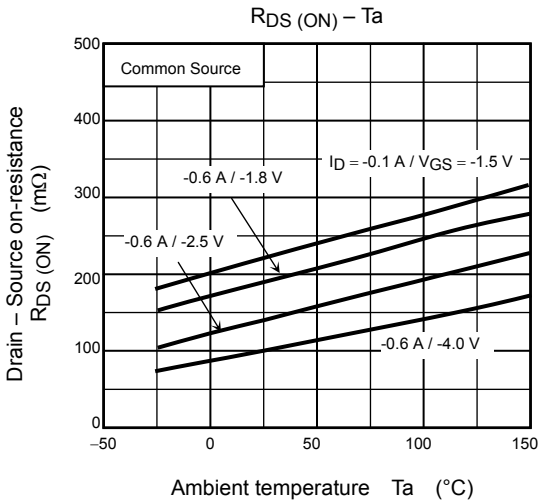

I_D – V_{DS}
-4 V
-1.8 V
-2.5 V
-1.5 V
VGS = -1.2 V
Common Source
Ta = 25 °C
Drain current I_D (A)
Drain - Source voltage V_{DS} (V)


I_D – V_{GS}
Common Source
V_{DS} = -3 V
Ta = 85 °C
25 °C
−25 °C
Drain current I_D (mA)
Gate - Source voltage V_{GS} (V)

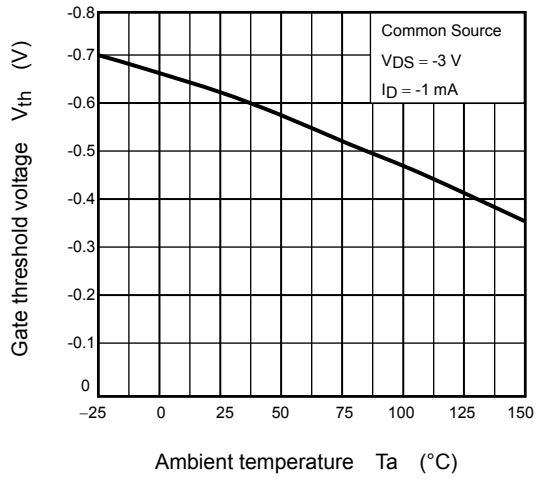

$R_{DS\ (ON)}$ – V_{GS}
I_D = -0.1 A
Common Source
25 °C
Ta = 85 °C
−25 °C
Drain – Source on-resistance $R_{DS\ (ON)}$ (mΩ)
Gate - Source voltage V_{GS} (V)


$R_{DS\ (ON)}$ – V_{GS}
I_D = -0.6 A
Common Source
25 °C
Ta = 85 °C
−25 °C
Drain – Source on-resistance $R_{DS\ (ON)}$ (mΩ)
Gate - Source voltage V_{GS} (V)

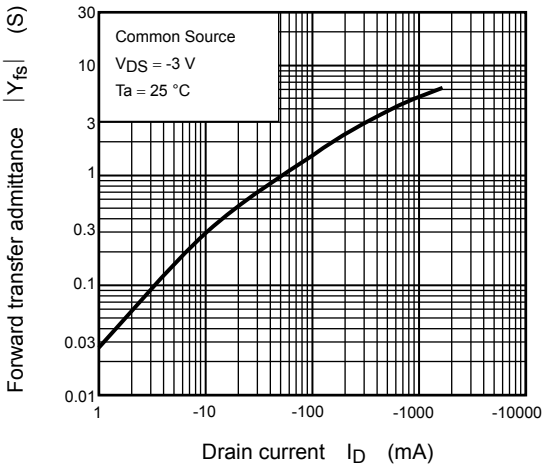

$R_{DS\ (ON)}$ – I_D
Common Source
Ta = 25°C
VGS = -1.5 V
-1.8 V
-2.5 V
-4.0 V
Drain – Source on-resistance $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)


$R_{DS\ (ON)}$ – Ta
Common Source
I_D = -0.1 A / V_{GS} = -1.5 V
-0.6 A / -1.8 V
-0.6 A / -2.5 V
-0.6 A / -4.0 V
Drain – Source on-resistance $R_{DS\ (ON)}$ (mΩ)
Ambient temperature Ta (°C)

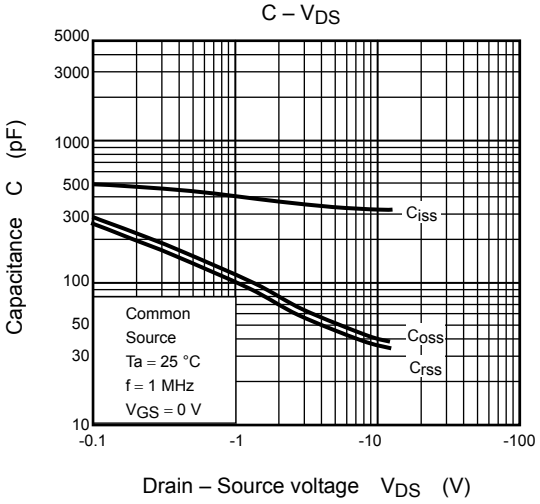
V_{th} – Ta



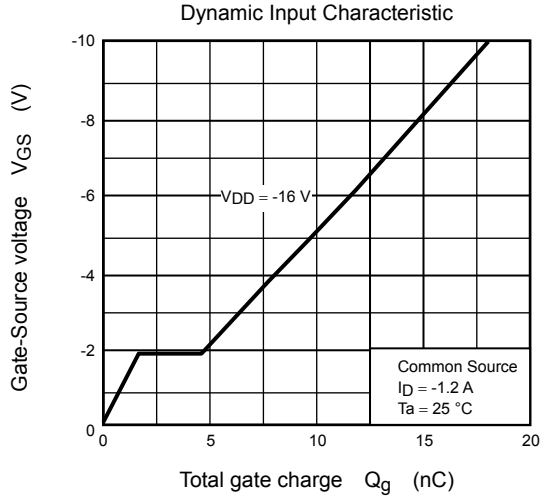
$|Y_{fs}|$ – I_D



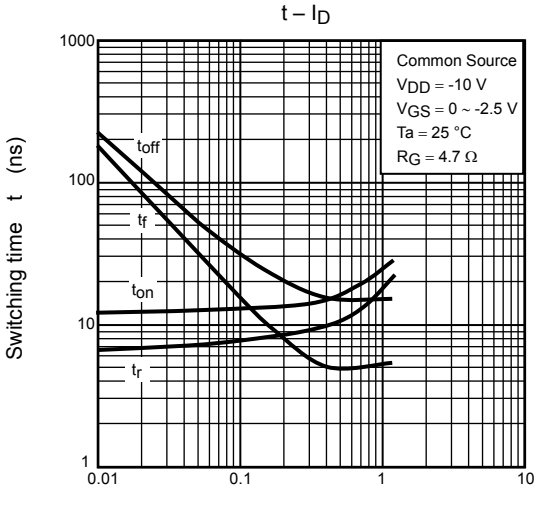
C – V_{DS}



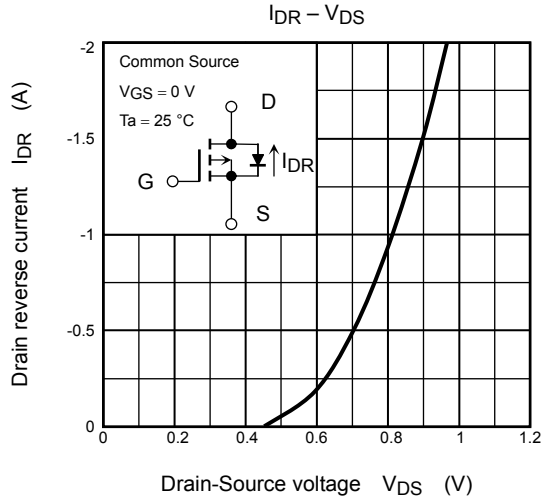
Dynamic Input Characteristic

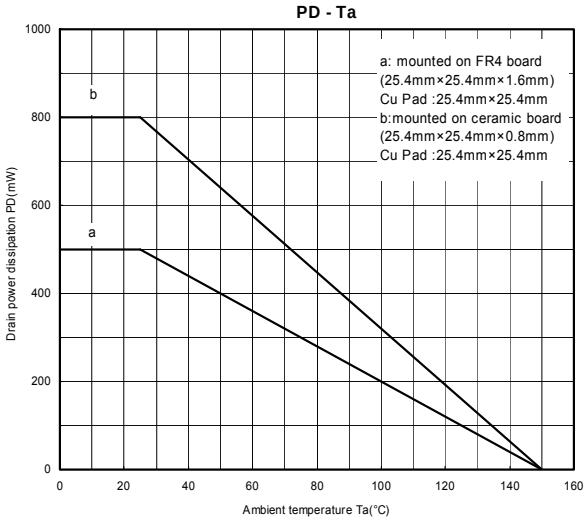


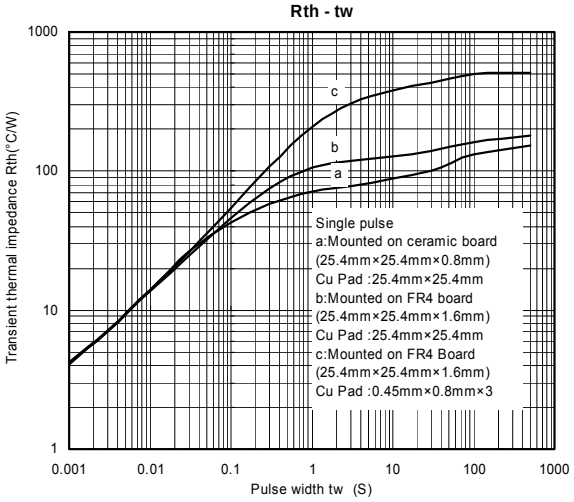
t – I_D



I_{DR} – V_{DS}




PD - Ta
Drain power dissipation PD(mW)
Ambient temperature Ta(°C)
a: mounted on FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
b:mounted on ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
a
b
1000
800
600
400
200
0
0
20
40
60
80
100
120
140
160


Rth - tw
Transient thermal impedance Rth(°C/W)
Pulse width tw (S)
Single pulse
a:Mounted on ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
b:Mounted on FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
c:Mounted on FR4 Board
(25.4mm×25.4mm×1.6mm)
Cu Pad :0.45mm×0.8mm×3
a
b
c
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000

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