High Current Transistors NPN Silicon

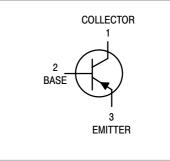
Features

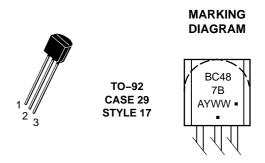
• Pb–Free Packages are Available*

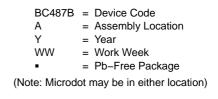


ON Semiconductor®

http://onsemi.com







ORDERING INFORMATION

Device	Package	Shipping [†]
BC487	TO-92	5000 Units / Box
BC487G	TO–92 (Pb–Free)	5000 Units / Box
BC487B	TO-92	5000 Units / Box
BC487BG	TO–92 (Pb–Free)	5000 Units / Box
BC487BRL1	TO-92	2000/Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS

MAXIMUM RATINGS					
Rating	Symbol	Value	Unit		
Collector – Emitter Voltage	V _{CEO}	60	Vdc		
Collector – Base Voltage	V _{CBO}	60	Vdc		
Emitter – Base Voltage	V _{EBO}	5.0	Vdc		
Collector Current – Continuous	Ι _C	0.5	Adc		
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P _D	625 5.0	mW mW/°C		
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	1.5 12	W mW/°C		
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150	°C		

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

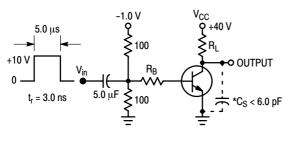
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	R_{\thetaJA}	200	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83.3	°C/W

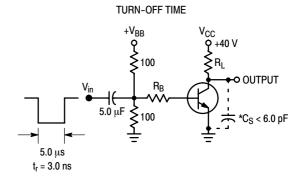
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (Note 1) ($I_C = 10 \text{ mAdc}, I_B = 0$)	V _{(BR)CEO}	60	-	-	Vdc
Collector – Base Breakdown Voltage ($I_C = 100 \ \mu Adc, I_E = 0$)	V _{(BR)CBO}	60	-	-	Vdc
Emitter – Base Breakdown Voltage ($I_E = 10 \ \mu Adc, I_C = 0$)	V _{(BR)EBO}	5.0	-	-	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$)	I _{CBO}	-	_	100	nAdc
ON CHARACTERISTICS*					
$\label{eq:loss} \begin{array}{l} \text{DC Current Gain} \\ (I_C = 10 \text{ mAdc}, \text{ V}_{CE} = 2.0 \text{ Vdc}) \\ (I_C = 100 \text{ mAdc}, \text{ V}_{CE} = 2.0 \text{ Vdc}) \\ & \text{BC487B} \\ (I_C = 1.0 \text{ Adc}, \text{ V}_{CE} = 5.0 \text{ Vdc})^* \end{array}$	h _{FE}	40 60 160 15	- - 260 -	- 400 400 -	_
Collector – Emitter Saturation Voltage ($I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$) ($I_C = 1.0 \text{ Adc}, I_B = 100 \text{ mAdc}$)	V _{CE(sat)}		0.2 0.3	0.5 -	Vdc
Base – Emitter Saturation Voltage ($I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$) ($I_C = 1.0 \text{ Adc}, I_B = 100 \text{ mAdc}$) ⁽¹⁾	V _{BE(sat)}		0.85 0.9	1.2 -	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (I _C = 50 mAdc, V_{CE} = 2.0 Vdc, f = 100 MHz)	f _T	-	200	-	MHz
Output Capacitance $(V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz})$	C _{ob}	-	7.0	-	pF
Input Capacitance ($V_{EB} = 0.5 \text{ Vdc}, I_C = 0, f = 1.0 \text{ MHz}$)	C _{ib}	-	50	-	pF

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle 2.0%.







*Total Shunt Capacitance of Test Jig and Connectors For PNP Test Circuits, Reverse All Voltage Polarities

Figure 1. Switching Time Test Circuits

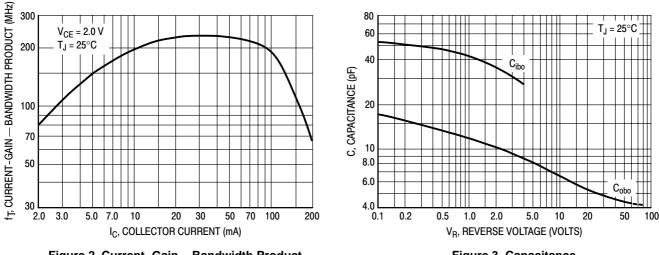
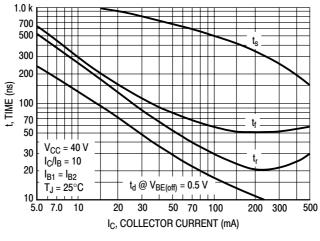




Figure 3. Capacitance





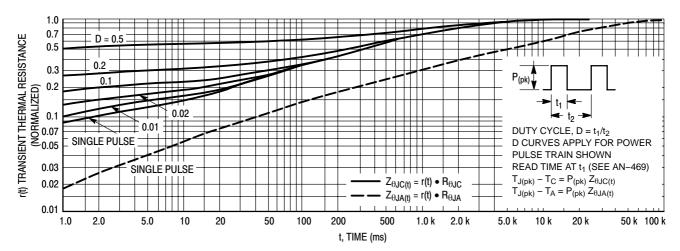


Figure 5. Thermal Response

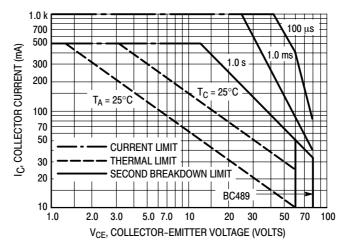
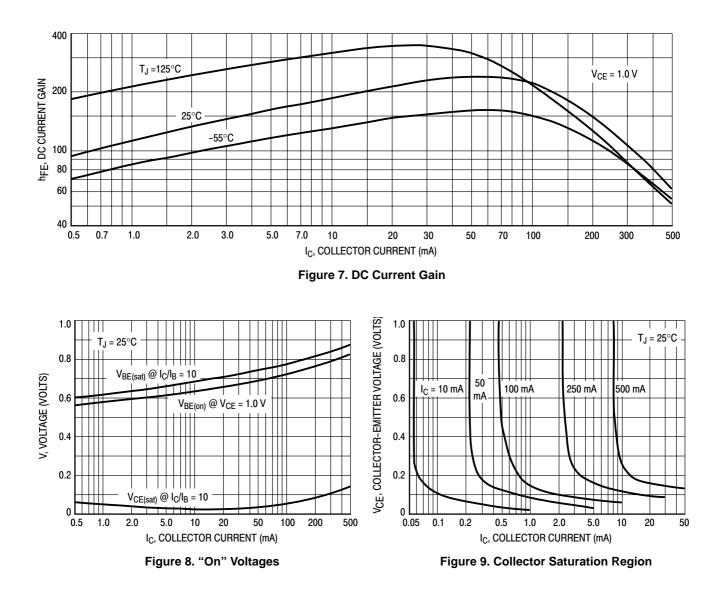
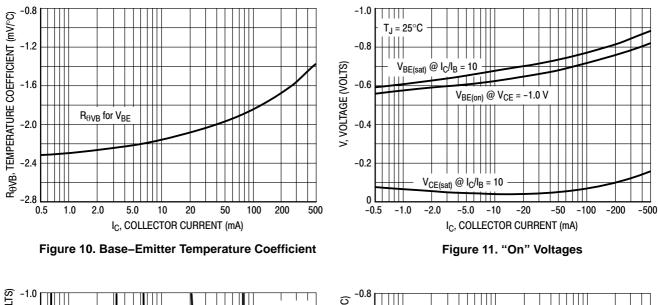


Figure 6. Active Region – Safe Operating Area





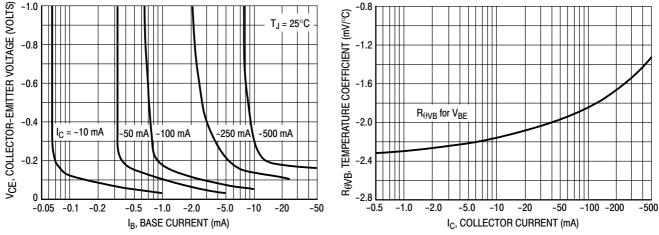
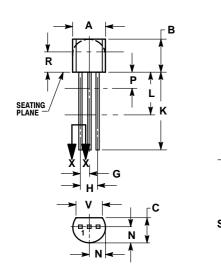


Figure 12. Collector Saturation Region

Figure 13. Base–Emitter Temperature Coefficient

PACKAGE DIMENSIONS

TO-92 (TO-226) CASE 29-11 ISSUE AL





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
 CONTOUR OF PACKAGE BEYOND DIMENSION R
- IS UNCONTROLLED. 4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.175	0.205	4.45	5.20
В	0.170	0.210	4.32	5.33
С	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
Н	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
Κ	0.500		12.70	
L	0.250		6.35	
Ν	0.080	0.105	2.04	2.66
Ρ		0.100		2.54
R	0.115		2.93	
٧	0.135		3.43	

STYLE 17:

PIN 1. COLLECTOR 2. BASE 3. EMITTER

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use payes that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunit//Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082–1312 USA Phone: 480–829–7710 or 800–344–3860 Toll Free USA/Canada Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850 ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.