SC16C2552B

5 V, 3.3 V and 2.5 V dual UART, 5 Mbit/s (max.), with 16-byte FIFOs

Rev. 03 — 12 February 2009 Product data sheet

1. General description

The SC16C2552B is a two channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data, and vice versa. The UART can handle serial data rates up to 5 Mbit/s.

The SC16C2552B is pin compatible with the PC16552 and ST16C2552. The SC16C2552B provides enhanced UART functions with 16-byte FIFOs, modem control interface, DMA mode data transfer and concurrent writes to control registers of both channels. The DMA mode data transfer is controlled by the FIFO trigger levels and the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ signals. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loopback capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC16C2552B operates at 5 V, 3.3 V and 2.5 V and the industrial temperature range, and is available in a plastic PLCC44 package.

2. Features

- Industrial temperature range (–40 °C to +85 °C)
- 5 V, 3.3 V and 2.5 V operation
- Pin-to-pin compatible to PC16C552, ST16C2552
- Up to 5 Mbit/s data rate at 5 V and 3.3 V, and 3 Mbit/s at 2.5 V
- 5 V tolerant on input only pins[1]
- 16-byte transmit FIFO
- 16-byte receive FIFO with error flags
- Independent transmit and receive UART control
- Four selectable receive FIFO interrupt trigger levels; fixed transmit FIFO interrupt trigger level
- Modem control functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, $\overline{\text{CD}}$)
- DMA operation and DMA monitoring via package I/O pins, $\overline{\text{TXRDY}}$/$\overline{\text{RXRDY}}$
- UART internal register sections A and B may be written to concurrently
- Multi-function output allows more package functions with fewer I/O pins
- Programmable character lengths (5, 6, 7, 8), with even, odd, or no parity

1. For data bus pins D7 to D0, see Table 23 “Limiting values”.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC16C2552BIA44	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

4. Block diagram

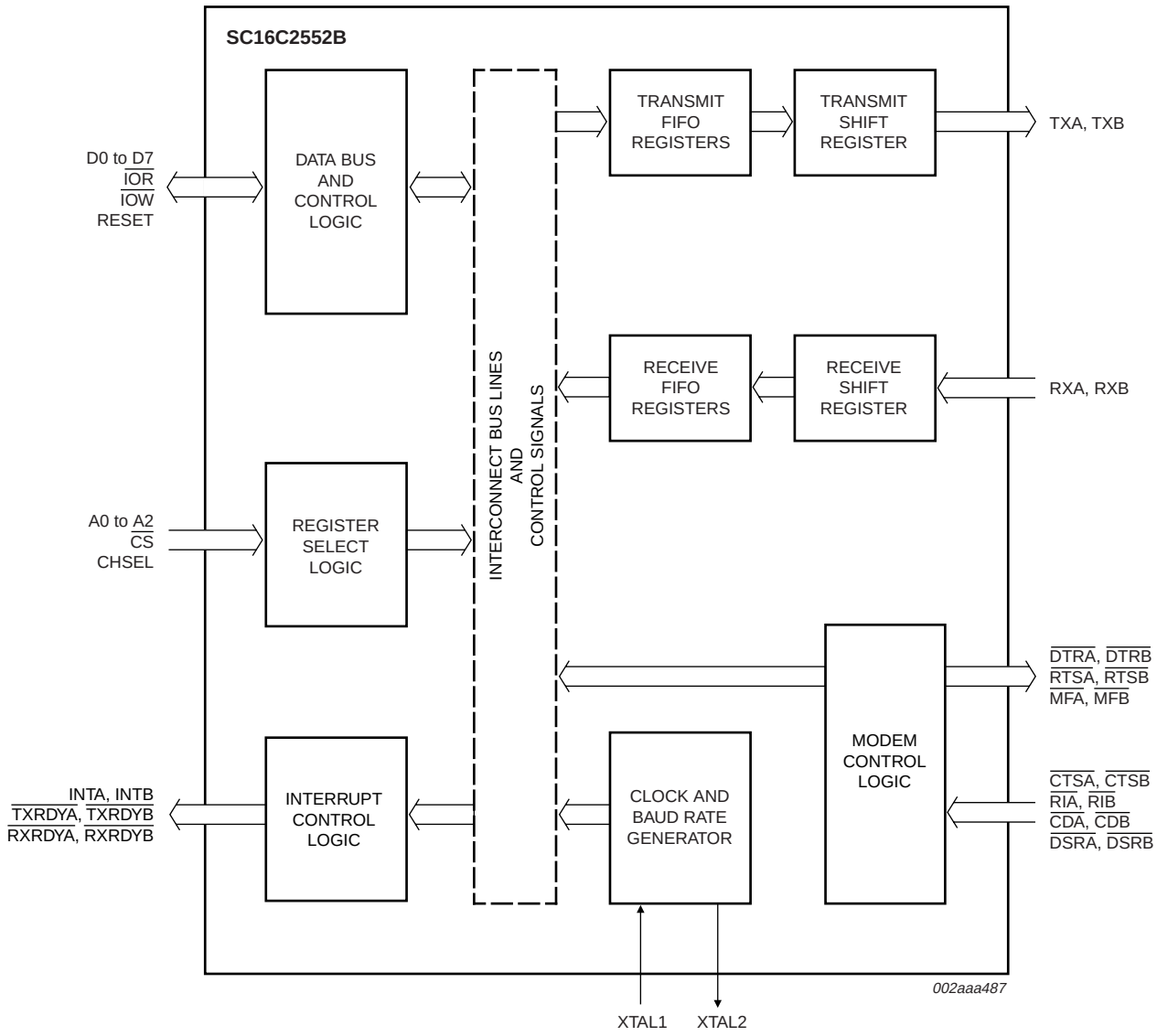


Fig 1. Block diagram of SC16C2552B

5. Pinning information

5.1 Pinning

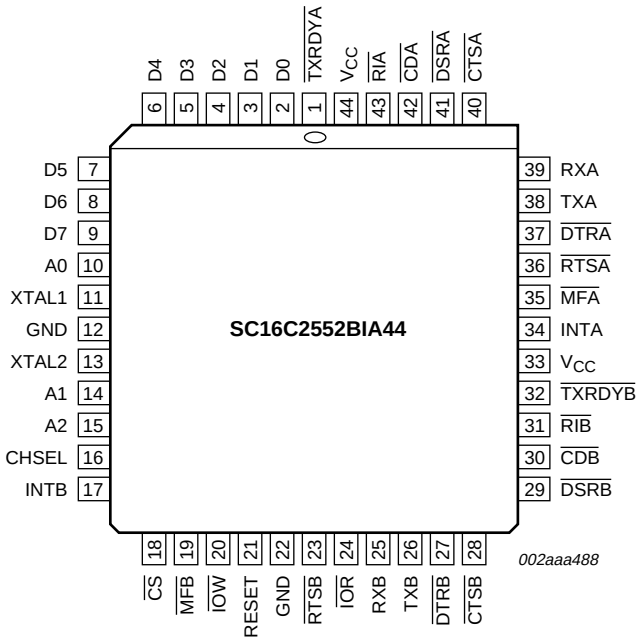


Fig 2. Pin configuration for PLCC44

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	10	I	**Register select.** A0 to A2 are used during read and write operations to select the UART register to read from or write to.
A1	14	I	
A2	15	I	
$\overline{CDA}$	42	I	**Carrier detect A, B (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	30	I	
CHSEL	16	I	**Channel select.** UART channel A or B is selected by the logic state of this pin when $\overline{CS}$ is a logic 0. A logic 0 on CHSEL selects the UART channel B, while a logic 1 selects UART channel A. Bit 0 of AFR register can temporarily override CHSEL function, allowing user to write to both channel registers simultaneously with one write cycle.
$\overline{CTSA}$	40	I	**Clear to Send A, B (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on the $\overline{CTSn}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C2552B. Status can be tested by reading MSR[4].
$\overline{CTSB}$	28	I	
$\overline{CS}$	18	I	**Chip select (active LOW).** This function selects channel A or channel B in accordance with the logical state of the CHSEL pin. This allows data to be transferred between the user CPU and the SC16C2552B.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
D0	2	I/O	**Data bus (bidirectional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU.
D1	3	I/O	
D2	4	I/O	
D3	5	I/O	
D4	6	I/O	
D5	7	I/O	
D6	8	I/O	
D7	9	I/O	
$\overline{DSRA}$	41	I	**Data Set Ready A, B (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART.
$\overline{DSRB}$	29	I	
$\overline{DTRA}$	37	O	**Data Terminal Ready A, B (active LOW).** These outputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that the SC16C2552B is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTRn}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset.
$\overline{DTRB}$	27	O	
GND	12, 22	I	**Signal and power ground.**
INTA	34	O	**Interrupt A, B (active HIGH).** This function is associated with individual channel interrupts. Interrupts are enabled in the Interrupt Enable Register (IER). Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.
INTB	17	O	
$\overline{IOR}$	24	I	**Read strobe (active LOW).** A logic 0 transition on this pin will load the contents of an internal register defined by address bits A[2:0] onto the SC16C2552B data bus (D[7:0]) for access by external CPU.
$\overline{IOW}$	20	I	**Write strobe (active LOW).** A logic 0 transition on this pin will transfer the contents of the data bus (D[7:0]) from the external CPU to an internal register that is defined by address bits A[2:0].
$\overline{MFA}$	35	O	**Multi-function A, B.** This function is associated with an individual channel function, A or B. User programmable bits 2:1 of the Alternate Function Register (AFR) selects a signal function or output on these pins. $\overline{OP2}$ (interrupt enable), $\overline{BAUDOUT}$, and $\overline{RXRDY}$ are signal functions that may be selected by the AFR. These signal functions are described as follows: **$\overline{OP2}$.** When $\overline{OP2}$ is selected, the $\overline{MFn}$ pin is a logic 0 when MCR[3] is set to a logic 1. A logic 1 is the default signal condition that is available following a master reset or power-up. **$\overline{BAUDOUT}$.** When $\overline{BAUDOUT}$ function is selected, the 16× baud rate clock output is available at this pin. **$\overline{RXRDY}$.** $\overline{RXRDY}$ is primarily intended for monitoring DMA mode 1 transfers for the receive data FIFOs. A logic 0 indicates there is receive data to read/unload, i.e., receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{MFB}$	19	O	
RESET	21	I	**Reset (active HIGH).** A logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. See Section 7.11 “SC16C2552B external reset condition” for initialization details.
$\overline{RIA}$	43	I	**Ring Indicator A, B (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt if modem status interrupt is enabled.
$\overline{RIB}$	31	I	

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{RTSA}$	36	O	**Request to Send A, B (active LOW).** These outputs are associated with individual UART channels A through B. A logic 0 on the $\overline{RTSn}$ pin indicates the transmitter is ready to transmit data. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating that the transmitter is ready to transmit data. After a reset, this pin will be set to a logic 1.
$\overline{RTSB}$	23	O	
RXA	39	I	**Receive data A, B.** These inputs are associated with individual serial channel data to the SC16C2552B receive input circuits A through B. The RXn signal will be a logic 1 during reset, idle (no data). During the local Loopback mode, the RXn input pin is disabled and TXn data is connected to the UART RXn input, internally.
RXB	25	I	
TXA	38	O	**Transmit data A, B.** These outputs are associated with individual serial transmit channel data from the SC16C2552B. The TXn signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the TXn output pin is disabled and TXn data is internally connected to the UART RXn input.
TXB	26	O	
$\overline{TXRDYA}$	1	O	**Transmit Ready A, B (active LOW).** These outputs provide the TX FIFO/THR status for individual transmit channels (A, B). $\overline{TXRDYn}$ is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFOs. An individual channel's $\overline{TXRDYA}$, $\overline{TXRDYB}$ buffer ready status is indicated by logic 0, i.e., at least one location is empty and available in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{TXRDYB}$	32	O	
V_{CC}	33, 44	I	**Power supply input.**
XTAL1	11	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to this pin to provide custom data rates. See Section 6.5 "Programmable baud rate generator".
XTAL2	13	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1.

6. Functional description

The SC16C2552B provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The SC16C2552B is fabricated with an advanced CMOS process.

The SC16C2552B is an upward solution that provides a dual UART capability with 16 bytes of transmit and receive FIFO memory, instead of none in the 16C450. The SC16C2552B is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C2552B by the transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable receive FIFO trigger interrupt levels are uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C2552B is capable of operation up to 1.5 Mbit/s with a 24 MHz crystal. With a crystal or external clock input of 7.3728 MHz, the user can select data rates up to 460.8 kbit/s.

The rich feature set of the SC16C2552B is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls are all standard features.

6.1 UART A-B functions

The UART provides the user with the capability to bidirectionally transfer information between an external CPU, the SC16C2552B package, and an external serial device. A logic 0 on chip select pin $\overline{CS}$ and a logic 1 on CHSEL allows the user to configure, send data, and/or receive data via UART channel A. A logic 0 on chip select pin $\overline{CS}$ and a logic 0 on CHSEL allows the user to configure, send data, and/or receive data via UART channel B. Individual channel select functions are shown in Table 3.

Table 3. Serial port selection

Chip select	UART select
$\overline{CS}$ = 1	none
$\overline{CS}$ = 0	UART channel selected as follows:
	CHSEL = 1: UART channel A
	CHSEL = 0: UART channel B

During a write mode cycle, the setting of AFR[0] to a logic 1 will override the CHSEL selection and allow a simultaneous write to both UART channel sections. This functional capability allows the registers in both UART channels to be modified concurrently, saving individual channel initialization time. Caution should be considered, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode.

6.2 Internal registers

The SC16C2552B provides two sets of internal registers (A and B) consisting of 13 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 4. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), a user accessible scratchpad register (SPR), and an Alternate Function Register (AFR).

Table 4. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM, AFR)[1]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
0	1	0	Alternate Function Register	Alternate Function Register

[1] The baud rate register and AFR register sets are accessible only when $\overline{CS}$ is a logic 0 and LCR[7] is a logic 1 for the register set (A/B) being accessed.

6.3 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. The user can set the receive trigger level via FCR[7:6], but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. A time-out interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character, or the receive trigger interrupt is generated when RX FIFO level is equal to the program RX trigger value.

6.4 Time-out interrupts

The interrupts are enabled by IER[3:0]. Care must be taken when handling these interrupts. Following a reset, if the transmitter interrupt is enabled, the SC16C2552B will issue an interrupt to indicate that the Transmit Holding Register is empty. The ISR register provides the current singular highest priority interrupt only. A condition can exist where a higher priority interrupt may mask the lower priority interrupt(s). Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C2552B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time.

6.5 Programmable baud rate generator

The SC16C2552B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A baud rate generator is provided for each UART channel, allowing independent TX/RX channel control. The programmable Baud Rate Generator (BRG) is capable of accepting an input clock up to 80 MHz, as required for supporting a 5 Mbit/s data rate. The SC16C2552B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal is connected externally between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 5).

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C2552B divides the basic external clock by 16. The basic 16× clock provides table rates to support standard and custom applications using the same system design. The rate table is configured via the DLL and DLM internal register functions. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

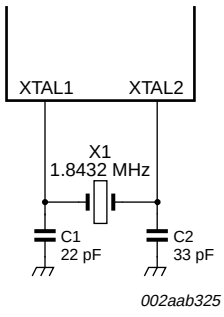


Fig 3. Crystal oscillator connection

Table 5. Baud rate generator programming table using a 1.8432 MHz clock

Output baud rate	Output 16× clock divisor (decimal)	Output 16× clock divisor (HEX)	DLM program value (HEX)	DLL program value (HEX)
50	2304	900	09	00
75	1536	600	06	00
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

6.6 DMA operation

The SC16C2552B FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[6:5] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C2552B activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the receive trigger level and the transmit FIFO. In this mode, the SC16C2552B sets the interrupt output pin when characters in the transmit FIFO is below 16, or the characters in the receive FIFOs are above the receive trigger level.

6.7 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, INT enable and MCR[2] in the MCR register (bits 3:2) control the modem $\overline{RI}$ and $\overline{CD}$ inputs, respectively. MCR signals $\overline{DTR}$ (bit 0) and $\overline{RTS}$ (bit 1) are used to control the modem $\overline{DSR}$ and $\overline{CTS}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 4). The $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from their normal modem control inputs pins, and instead are connected internally to $\overline{RTS}$, $\overline{DTR}$, $\overline{OP2}$ and $\overline{OP1}$. Loopback test data is entered into the transmit holding register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then

made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[3:0]) instead of the four Modem Status Register bits 7:4. The interrupts are still controlled by the IER.

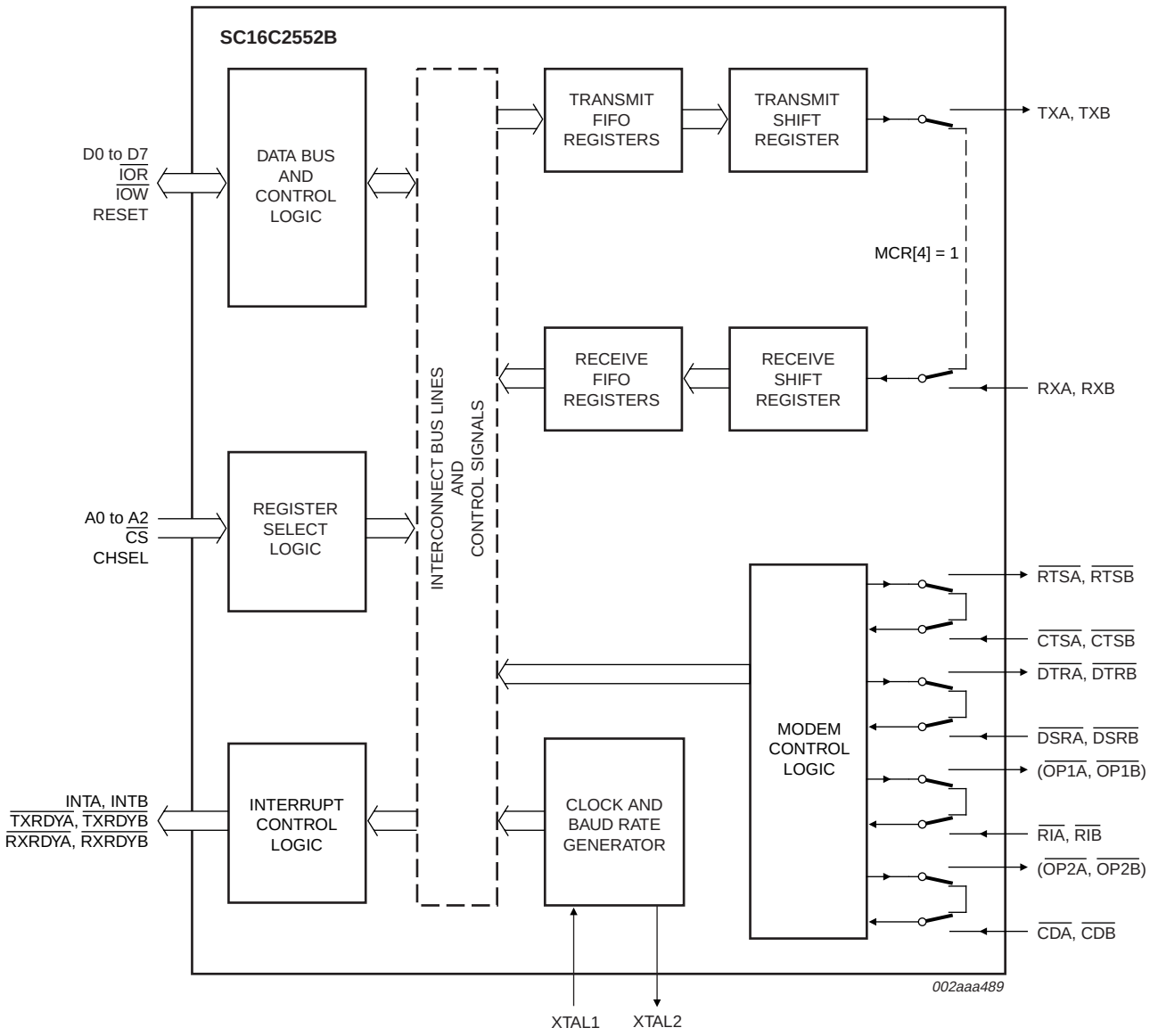


Fig 4. Internal Loopback mode diagram

7. Register descriptions

Table 6 details the assigned bit functions for the SC16C2552B internal registers. The assigned bit functions are further defined in Section 7.1 through Section 7.11.

Table 6. SC16C2552B internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General register set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register interrupt	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFOs enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	0	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	0	0	0	loopback	$\overline{OP2}$ output control	$\overline{OP1}$	$\overline{RTS}$	$\overline{DTR}$
1	0	1	LSR	60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special register set[3]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0	1	0	AFR	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

[1] The value shown represents the register's initialized hexadecimal value; X = not applicable.

[2] The 'General register set' registers are accessible only when $\overline{CS}$ is a logic 0 and LCR[7] is logic 0.

[3] The Baud rate register and AFR register sets are accessible only when $\overline{CS}$ is a logic 0 and LCR[7] is a logic 1. Set A is accessible when CHSEL is a logic 1, and Set B is accessible when CHSEL is a logic 0.

7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 through D0) to the TSR and UART via the THR, providing that the THR is empty. The THR empty flag in the LSR[5] register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR.

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC16C2552B and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA, INTB output pins.

Table 7. Interrupt Enable Register bits description

Bit	Symbol	Description
7:4	IER[7:4]	not used; initialized to logic 0
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[3:0]. logic 0 = disable the Modem Status Register interrupt (normal default condition) logic 1 = enable the Modem Status Register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[4:1]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt
1	IER[1]	Transmit Holding Register interrupt. In the 16C450 mode, this interrupt will be issued whenever the THR is empty and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO and THR are empty. logic 0 = disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition) logic 1 = enable the TXRDY (ISR level 3) interrupt
0	IER[0]	Receive Holding Register. In the 16C450 mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. logic 0 = disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition) logic 1 = enable the RXRDY (ISR level 2) interrupt

7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1) and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR register or by loading the THR with new data characters.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[3:0] enables the SC16C2552B in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of receive errors or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels and select the DMA mode.

7.3.1 DMA mode

7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation and is similar to the 16C450 mode. Transmit Ready ($\overline{\text{TXRDY}}$) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ($\overline{\text{RXRDY}}$) at the $\overline{\text{MFn}}$ pin will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character and AFR[2:1] is set to the $\overline{\text{RXRDY}}$ mode.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO has at least one empty location. $\overline{\text{TXRDY}}$ remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$ at the $\overline{\text{MFn}}$ pin remains a logic 0 as long as the FIFO fill level is above the programmed trigger level, and AFR[2:1] is set to the RXRDY mode.

7.3.2 FIFO mode

Table 8. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 9.
5:4	FCR[5:4]	Not used; initialized to logic 0.
3	FCR[3]	DMA mode select. logic 0 = set DMA mode ‘0’ (normal default condition) logic 1 = set DMA mode ‘1’ **Transmit operation in mode ‘0’:** When the SC16C2552B is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or Transmit Holding Register, the $\overline{\text{TXRDYn}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDYn}}$ pin will go to a logic 1 after the first character is loaded into the Transmit Holding Register. **Receive operation in mode ‘0’:** When the SC16C2552B is in 16C450 mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ signal at the $\overline{\text{MFn}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ signal at the $\overline{\text{MFn}}$ pin will go to a logic 1 when there are no more characters in the receiver. Note that the AFR register must be set to the RXRDY mode prior to any possible reading of the $\overline{\text{RXRDY}}$ signal.

Table 8. FIFO Control Register bits description *…continued*

Bit	Symbol	Description
3 (continued)		**Transmit operation in mode '1':** When the SC16C2552B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$n pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty. **Receive operation in mode '1':** When the SC16C2552B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-out has occurred, the $\overline{\text{RXRDY}}$ signal at the $\overline{\text{MF}}$n pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO. Note that the AFR register must be set to the RXRDY mode prior to any possible reading of the $\overline{\text{RXRDY}}$ signal.
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the Transmit Shift Register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the Receive Shift Register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFOs enabled. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO. **This bit must be a '1' when other FCR bits are written to or they will not be programmed.**

Table 9. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

7.4 Interrupt Status Register (ISR)

The SC16C2552B provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 10 shows the data values (bits 3:0) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 10. Interrupt source

Priority level	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	1	0	TXRDY (Transmitter Holding Register empty)
4	0	0	0	0	MSR (Modem Status Register)

Table 11. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the 16C450 mode. They are set to a logic 1 when the FIFOs are enabled in the SC16C2552B mode. logic 0 or cleared = default condition
5:4	ISR[5:4]	not used; initialized to a logic 0
3:1	ISR[3:1]	INT priority bits. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2 and 3 (see Table 10).
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits and the parity are selected by writing the appropriate bits in this register.

Table 12. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5:3	LCR[5:3]	Programs the parity conditions (see Table 13)
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 14). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 15). logic 0 or cleared = default condition

Table 13. LCR[5:3] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
X	0	1	odd parity
0	1	1	even parity
0	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 14. LCR[2] stop bit length

LCR[2]	Word length (bits)	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 15. LCR[1:0] word length

LCR[1]	LCR[0]	Word length (bits)
0	0	5
0	1	6
1	0	7
1	1	8

7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 16. Modem Control Register bits description

Bit	Symbol	Description
7:5	MCR[7:5]	reserved; initialized to a logic 0
4	MCR[4]	Loopback. Enable the local Loopback mode (diagnostics). In this mode the transmitter output (TX) and the receiver input (RX), $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$ and $\overline{RI}$ are disconnected from the SC16C2552B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 4). In this mode, the receiver and transmitter interrupts remain fully operational. The modem control interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable Loopback mode (normal default condition) logic 1 = enable local Loopback mode (diagnostics)
3	MCR[3]	$\overline{OP2}$. Used to control the modem $\overline{CD}$ signal in the Loopback mode. logic 0 = sets $\overline{OP2}$ to a logic 1 (normal default condition). In the Loopback mode, sets $\overline{CD}$ internally to a logic 1. logic 1 = sets $\overline{OP2}$ to a logic 0. In the Loopback mode, sets $\overline{CD}$ internally to a logic 0.
2	MCR[2]	$\overline{OP1}$. This bit is used in the Loopback mode only. In the Loopback mode, this bit is used to write the state of the modem $\overline{RI}$ interface signal.
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTS}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{RTS}$ output to a logic 0
0	MCR[0]	$\overline{DTR}$ logic 0 = force $\overline{DTR}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{DTR}$ output to a logic 0

7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C2552B and the CPU.

Table 17. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error. logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when RHR register is read.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the Transmit Holding Register and the Transmit Shift Register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to logic 1 whenever the Transmit FIFO and Transmit Shift Register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the Transmit Holding Register into the Transmit Shift Register. The bit is reset to a logic 0 concurrently with the loading of the Transmit Holding Register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt. logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error. logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error. logic 0 = no parity error (normal default condition logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error. logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the Receive Shift Register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the Receive Shift Register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready. logic 0 = no data in Receive Holding Register or FIFO (normal default condition) logic 1 = data has been received and is saved in the Receive Holding Register or FIFO

7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem or other peripheral device to which the SC16C2552B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 18. Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	Carrier Detect, CD. During normal operation, this bit is the complement of the $\overline{CD}$ input. Reading this bit in the Loopback mode produces the state of MCR[3] ($\overline{OP2A}$/$\overline{OP2B}$).
6	MSR[6]	Ring Indicator, RI. During normal operation, this bit is the complement of the $\overline{RI}$ input. Reading this bit in the Loopback mode produces the state of MCR[2] ($\overline{OP1A}$/$\overline{OP2A}$).
5	MSR[5]	Data Set Ready, DSR. During normal operation, this bit is the complement of the $\overline{DSR}$ input. During the Loopback mode, this bit is equivalent to MCR[0] ($\overline{DTR}$).
4	MSR[4]	Clear To Send, CTS. During normal operation, this bit is the complement of the $\overline{CTS}$ input. During the Loopback mode, this bit is equivalent to MCR[1] ($\overline{RTS}$).
3	MSR[3]	$\Delta\overline{CD}$ [1] logic 0 = no $\overline{CD}$ change (normal default condition) logic 1 = the $\overline{CD}$ input to the SC16C2552B has changed state since the last time it was read. A modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] logic 0 = no $\overline{RI}$ change (normal default condition) logic 1 = the $\overline{RI}$ input to the SC16C2552B has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] logic 0 = no $\overline{DSR}$ change (normal default condition) logic 1 = the $\overline{DSR}$ input to the SC16C2552B has changed state since the last time it was read. A modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] logic 0 = no $\overline{CTS}$ change (normal default condition) logic 1 = the $\overline{CTS}$ input to the SC16C2552B has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR bit 3:0 is set to logic 1, a Modem Status Interrupt will be generated.

7.9 Scratchpad Register (SPR)

The SC16C2552B provides a temporary data register to store 8 bits of user information.

7.10 Alternate Function Register (AFR)

This is a read/write register used to select specific modes of $\overline{MF}$ operation and to allow both UART register's sets to be written concurrently.

Table 19. Alternate Function Register bit description

Bit	Symbol	Description
7:3	AFR[7:3]	Not used. All are initialized to logic 0.
2:1	AFR[2:1]	Selects a signal function for output on the $\overline{MFA}$, $\overline{MFB}$ pins. These signal functions are described as: $\overline{OP2}$ (interrupt enable), $\overline{BAUDOUT}$, or $\overline{RXRDY}$. Only one signal function can be selected at a time. See Table 20.
0	AFR[0]	When this bit is set, CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by CPU when both channels are initialized to the same state. The external CPU can set or clear this bit by accessing either register set. When this bit is set, the Channel Select pin, CHSEL, still selects the channel to be accessed during read operation. Setting or clearing this bit has no effect on read operations. The user should ensure that LCR[7] of both channels are in the same state before executing a concurrent write to the registers at address 0, 1, or 2. logic 0 = no concurrent write (normal default condition) logic 1 = register set A and B are written concurrently with a single external CPU I/O write operation.

Table 20. $\overline{MFA}$, $\overline{MFB}$ function selection

AFR[2]	AFR[1]	MF function
0	0	$\overline{OP2}$
0	1	$\overline{BAUDOUT}$
1	0	$\overline{RXRDY}$
1	1	reserved

7.11 SC16C2552B external reset condition

Table 21. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
FCR	FCR[7:0] = 0
AFR	AFR[7:0] = 0

Table 22. Reset state for outputs

Output	Reset state
TXA, TXB	HIGH
$\overline{OP2A}$, $\overline{OP2B}$	HIGH
$\overline{RTSA}$, $\overline{RTSB}$	HIGH
$\overline{DTRA}$, $\overline{DTRB}$	HIGH
INTA, INTB	LOW
$\overline{TXRDYA}$, $\overline{TXRDYB}$	LOW

8. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	7	V
V_n	voltage on any other pin	at D7 to D0 pins	GND – 0.3	V_{CC} + 0.3	V
		at input only pins	GND – 0.3	5.3	V
T_{amb}	operating temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}/pack	total power dissipation per package		-	500	mW

9. Static characteristics

Table 24. Static characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %; unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage		–0.3	+0.45	–0.3	+0.6	–0.5	+0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage		1.8	V_{CC}	2.4	V_{CC}	3.0	V_{CC}	V
V_{IL}	LOW-level input voltage	except X1 clock	–0.3	+0.65	–0.3	+0.8	–0.5	+0.8	V
V_{IH}	HIGH-level input voltage	except X1 clock	1.6	-	2.0	-	2.2	-	V
V_{OL}	LOW-level output voltage	on all outputs[1]							
		I_{OL} = 5 mA (data bus)	-	-	-	-	-	0.4	V
		I_{OL} = 4 mA (other outputs)	-	-	-	0.4	-	-	V
		I_{OL} = 2 mA (data bus)	-	0.4	-	-	-	-	V
		I_{OL} = 1.6 mA (other outputs)	-	0.4	-	-	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA (data bus)	-	-	-	-	2.4	-	V
		I_{OH} = –1 mA (other outputs)	-	-	2.0	-	-	-	V
		I_{OH} = –800 µA (data bus)	1.85	-	-	-	-	-	V
		I_{OH} = –400 µA (other outputs)	1.85	-	-	-	-	-	V
I_{LIL}	LOW-level input leakage current		-	±10	-	±10	-	±10	µA
$I_{L(clk)}$	clock leakage current		-	±30	-	±30	-	±30	µA
I_{CC}	supply current	f = 5 MHz	-	3.5	-	4.5	-	4.5	mA
C_i	input capacitance		-	5	-	5	-	5	pF

[1] Except XTAL2, V_{OL} = 1 V typical.

10. Dynamic characteristics

Table 25. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %; unless otherwise specified.

Symbol	Parameter	Conditions		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
t_{WH}	pulse width HIGH			10	-	6	-	6	-	ns
t_{WL}	pulse width LOW			10	-	6	-	6	-	ns
f_{XTAL1}	frequency on pin XTAL1		[1][2]	-	48	-	80		80	MHz
t_{6s}	address set-up time			0	-	0	-	0	-	ns
t_{6h}	address hold time			0	-	0	-	0	-	ns
t_{7d}	$\overline{IOR}$ delay from chip select			10	-	10	-	10	-	ns
t_{7w}	$\overline{IOR}$ strobe width	25 pF load		77	-	26	-	23	-	ns
t_{7h}	chip select hold time from $\overline{IOR}$			0	-	0	-	0	-	ns
t_{9d}	read cycle delay	25 pF load		20	-	20	-	20	-	ns
t_{12d}	delay from $\overline{IOR}$ to data	25 pF load		-	77	-	26	-	23	ns
t_{12h}	data disable time	25 pF load		-	15	-	15	-	15	ns
t_{13d}	$\overline{IOW}$ delay from chip select			10	-	10	-	10	-	ns
t_{13w}	$\overline{IOW}$ strobe width			20	-	20	-	15	-	ns
t_{13h}	chip select hold time from $\overline{IOW}$			0	-	0	-	0	-	ns
t_{15d}	write cycle delay			25	-	25	-	20	-	ns
t_{16s}	data set-up time			20	-	20	-	15	-	ns
t_{16h}	data hold time			15	-	5	-	5	-	ns
t_{17d}	delay from $\overline{IOW}$ to output	25 pF load		-	100	-	33	-	29	ns
t_{18d}	delay to set interrupt from Modem input	25 pF load		-	100	-	24	-	23	ns
t_{19d}	delay to reset interrupt from $\overline{IOR}$	25 pF load		-	100	-	24	-	23	ns
t_{20d}	delay from stop to set interrupt		[3]	-	T_{RCLK}	-	T_{RCLK}	-	T_{RCLK}	s
t_{21d}	delay from $\overline{IOR}$ to reset interrupt	25 pF load		-	100	-	29	-	28	ns
t_{22d}	delay from start to set interrupt			-	100	-	45	-	40	ns
t_{23d}	delay from $\overline{IOW}$ to transmit start		[3]	$8T_{RCLK}$	$24T_{RCLK}$	$8T_{RCLK}$	$24T_{RCLK}$	$8T_{RCLK}$	$24T_{RCLK}$	s
t_{24d}	delay from $\overline{IOW}$ to reset interrupt			-	100	-	45	-	40	ns
t_{25d}	delay from stop to set $\overline{RXRDY}$		[3]	-	T_{RCLK}	-	T_{RCLK}	-	T_{RCLK}	s
t_{26d}	delay from $\overline{IOR}$ to reset $\overline{RXRDY}$			-	100	-	45	-	40	ns
t_{27d}	delay from $\overline{IOW}$ to set $\overline{TXRDY}$			-	100	-	45	-	40	ns

Table 25. Dynamic characteristics *...continued*

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %; unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
t_{28d}	delay from start to reset $\overline{TXRDY}$	[3]	-	$8T_{RCLK}$	-	$8T_{RCLK}$	-	$8T_{RCLK}$	s
t_{RESET}	RESET pulse width	[4]	200	-	40	-	40	-	ns
N	baud rate divisor		1	$(2^{16} - 1)$	1	$(2^{16} - 1)$	1	$(2^{16} - 1)$	

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] Maximum frequency = $\frac{1}{t_{w(clk)}}$

[3] RCLK is an internal signal derived from divisor latch LSB (DLL) and divisor latch MSB (DLM) divisor latches.

[4] Reset pulse must happen when these signals are inactive: $\overline{CS}$, $\overline{IOW}$, $\overline{IOR}$.

10.1 Timing diagrams

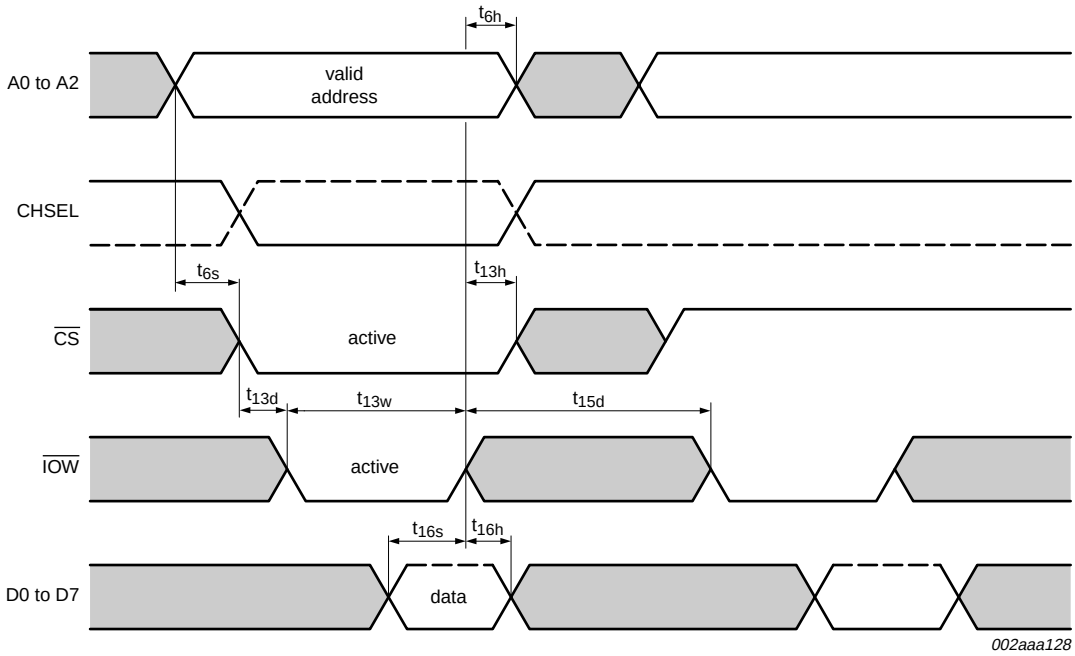


Fig 5. General write timing

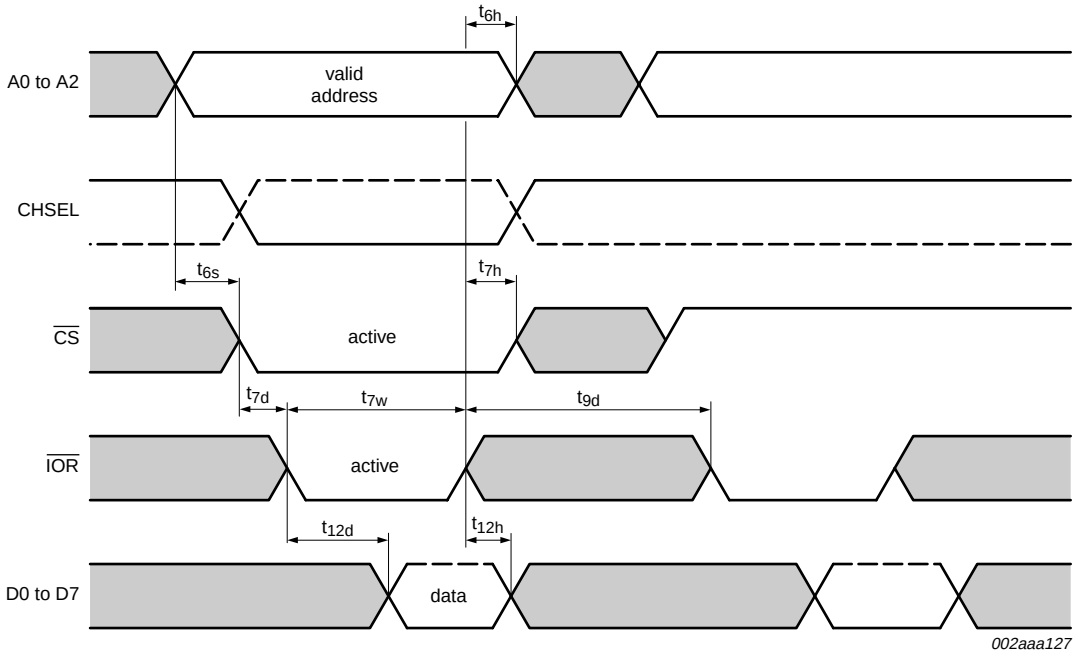


Fig 6. General read timing

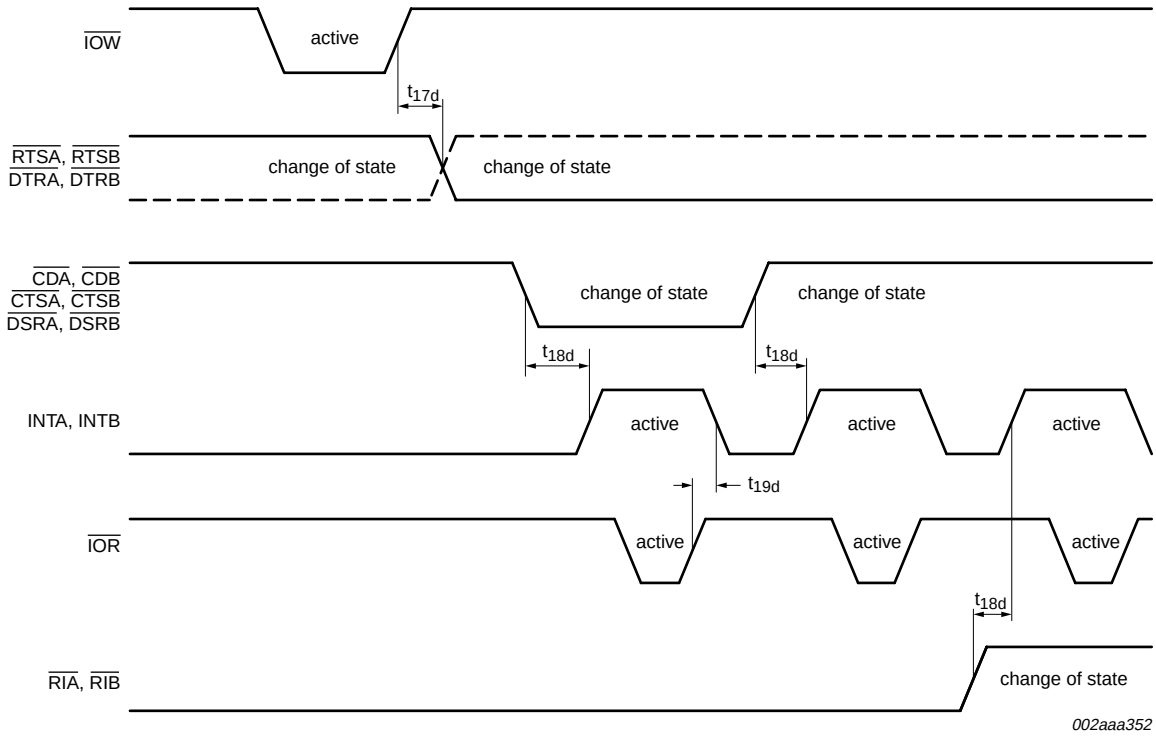
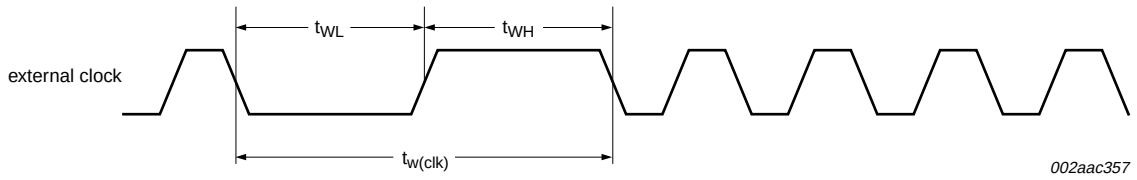


Fig 7. Modem input/output timing



$$f_{XTAL1} = \frac{1}{t_{w(clk)}}$$

Fig 8. External clock timing

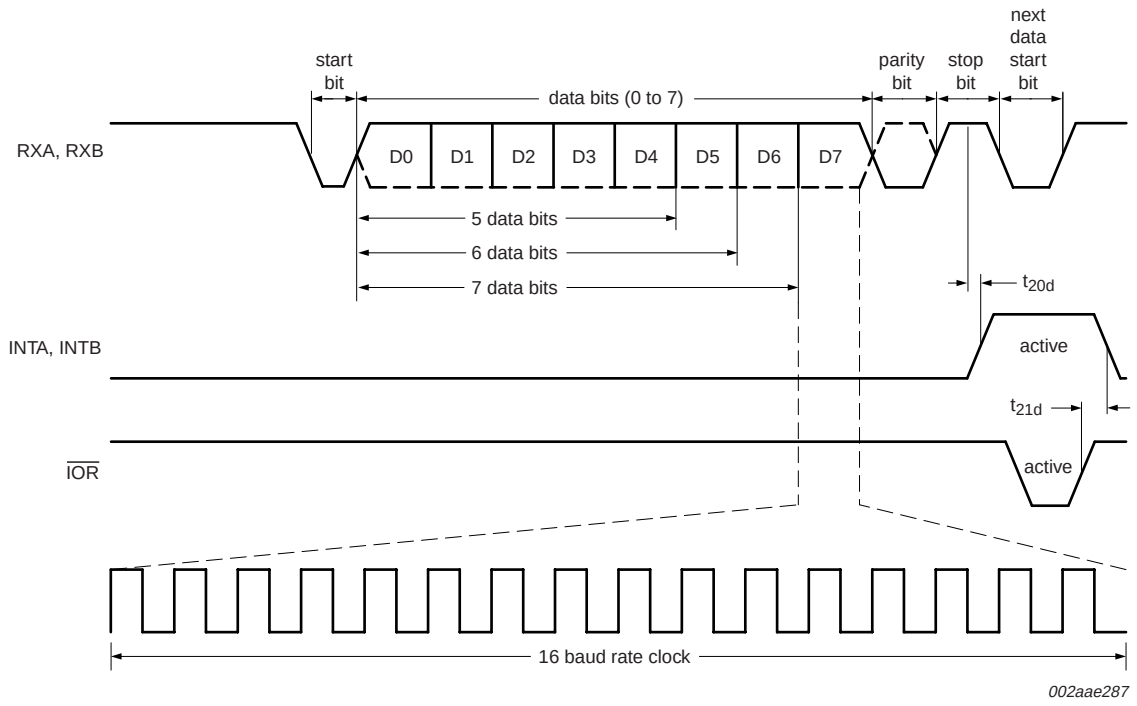


Fig 9. Receive timing

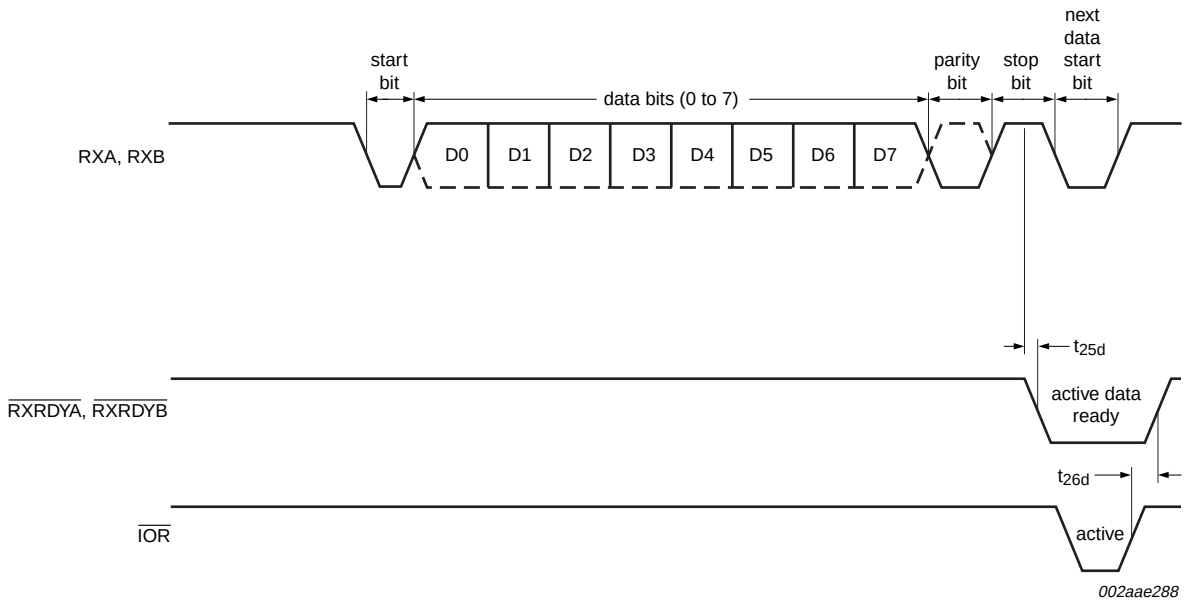


Fig 10. Receive ready timing in non-FIFO mode

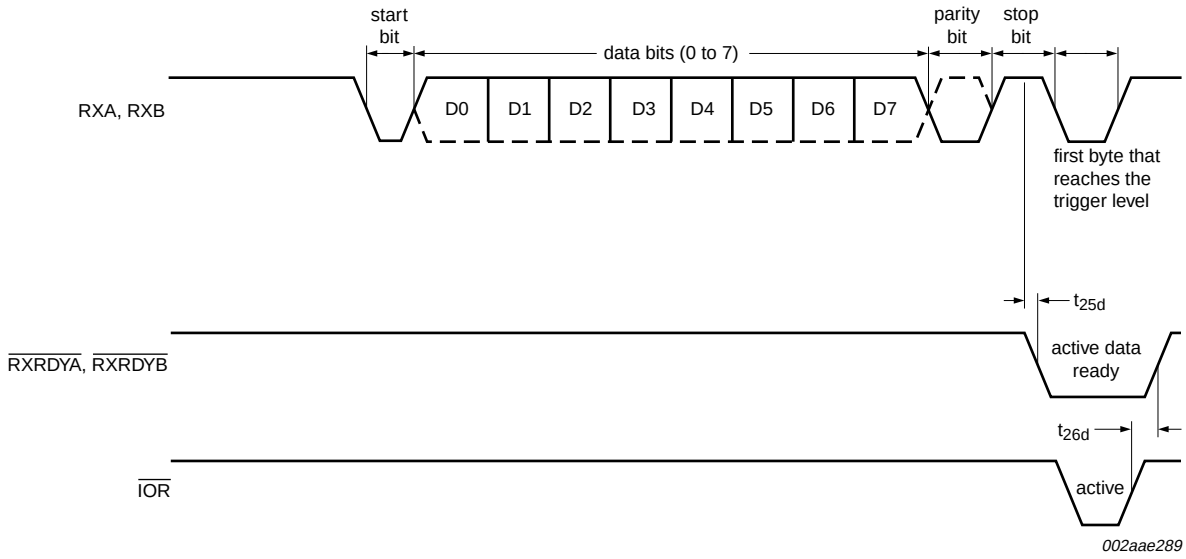


Fig 11. Receive ready timing in FIFO mode

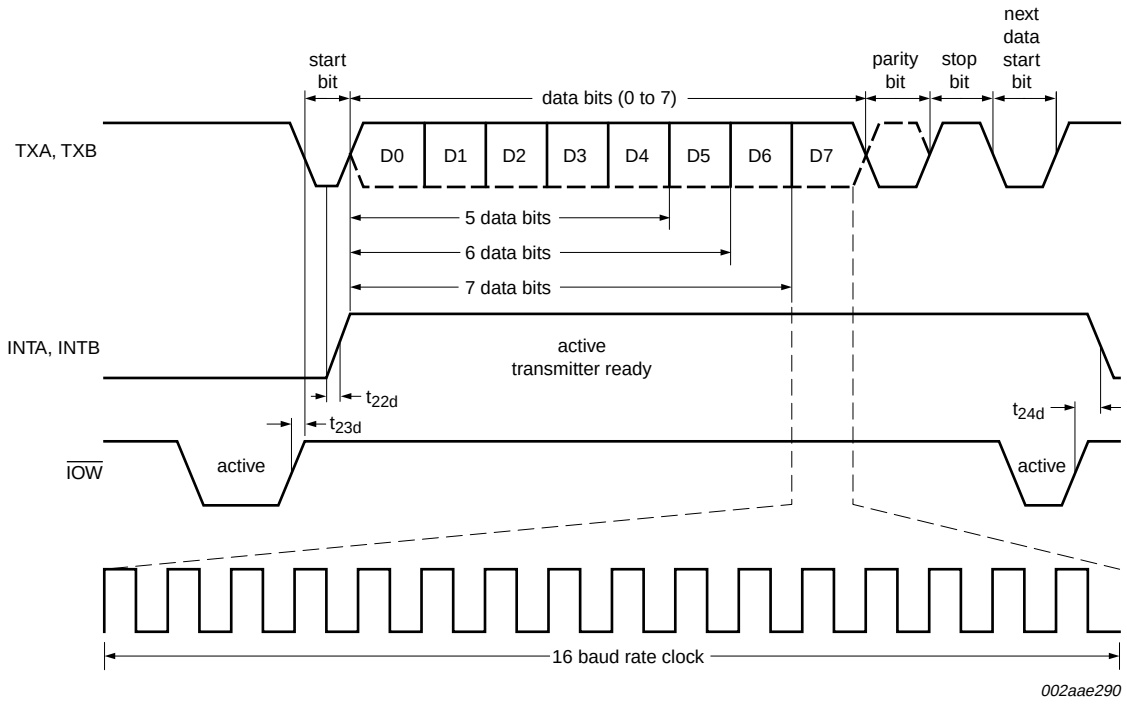


Fig 12. Transmit timing

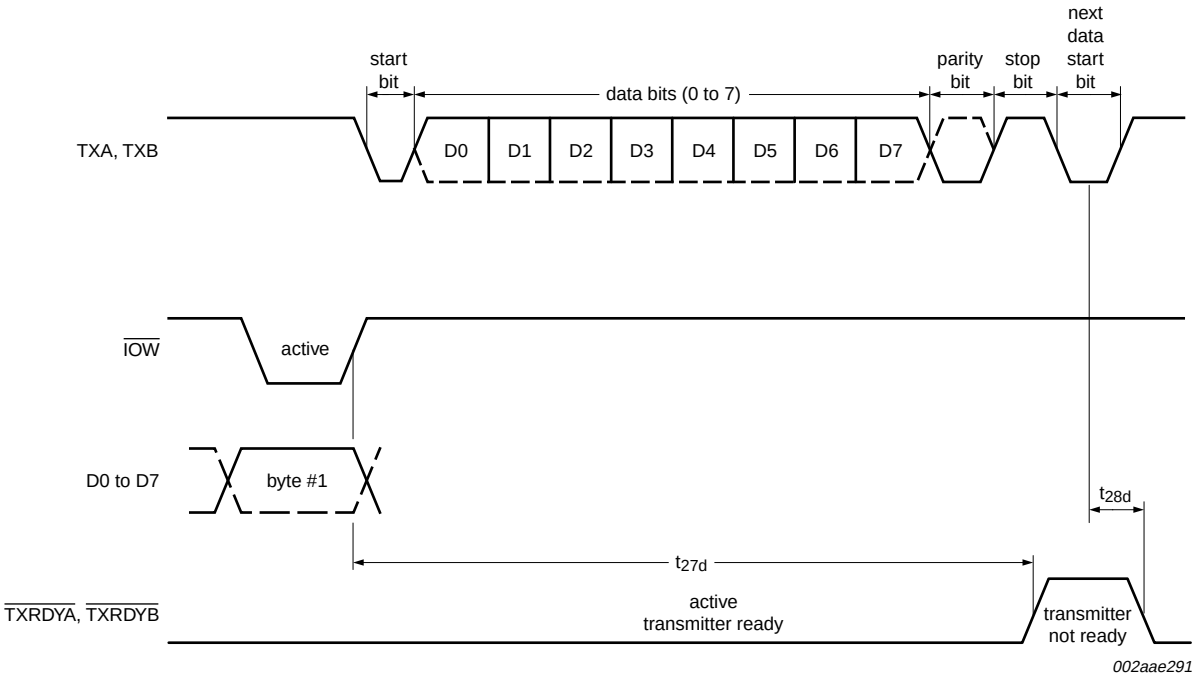


Fig 13. Transmit ready timing in non-FIFO mode

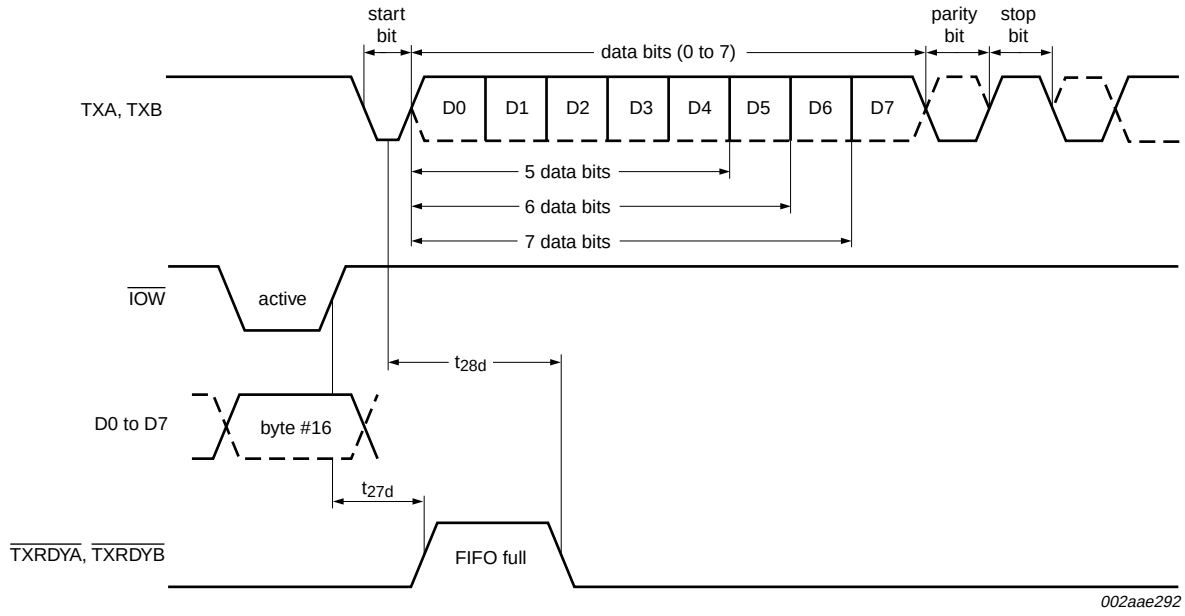
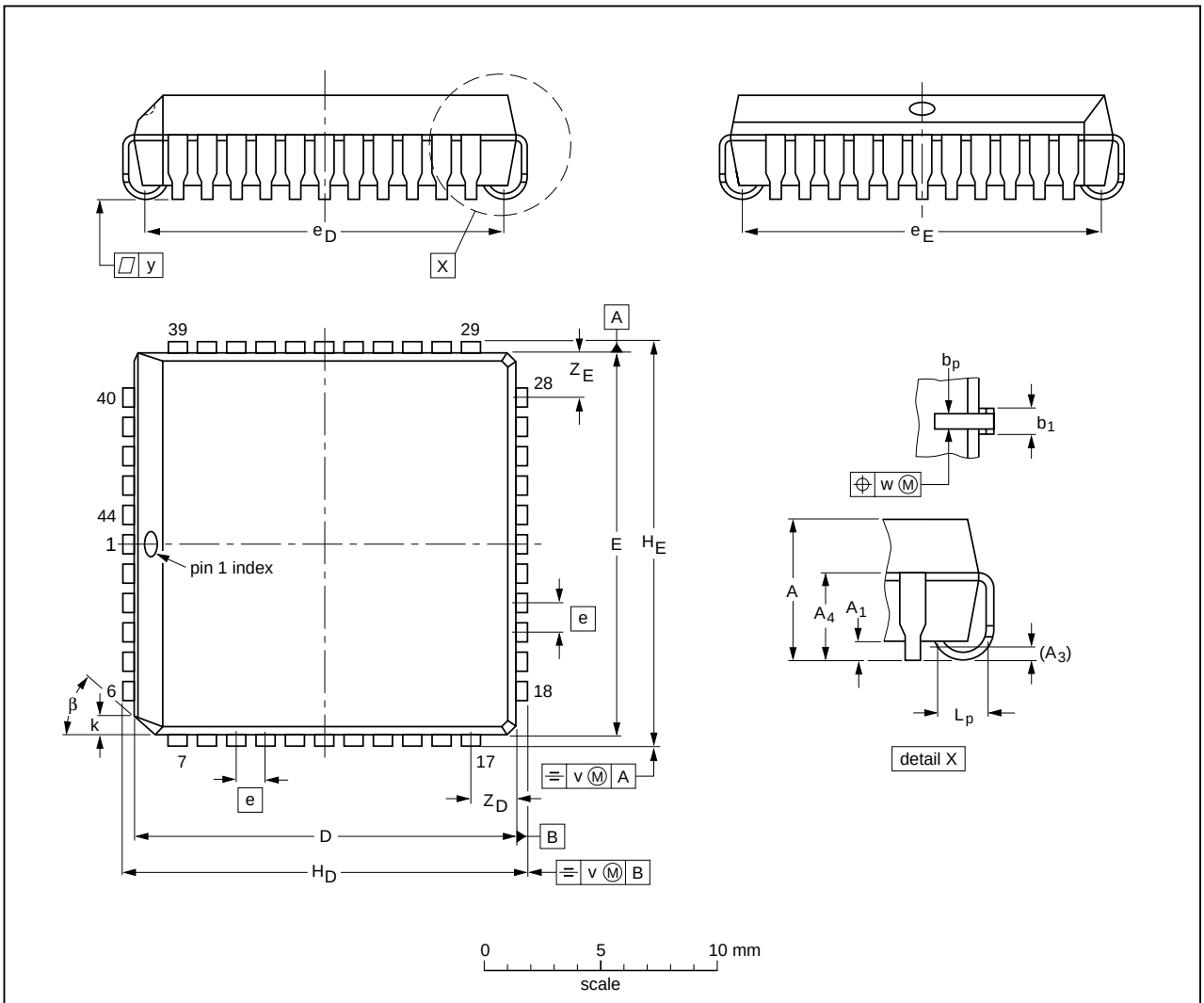


Fig 14. Transmit ready timing in FIFO mode (DMA mode '1')

11. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 15. Package outline SOT187-2 (PLCC44)

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 26 and 27

Table 26. SnPb eutectic process (from J-STD-020C)

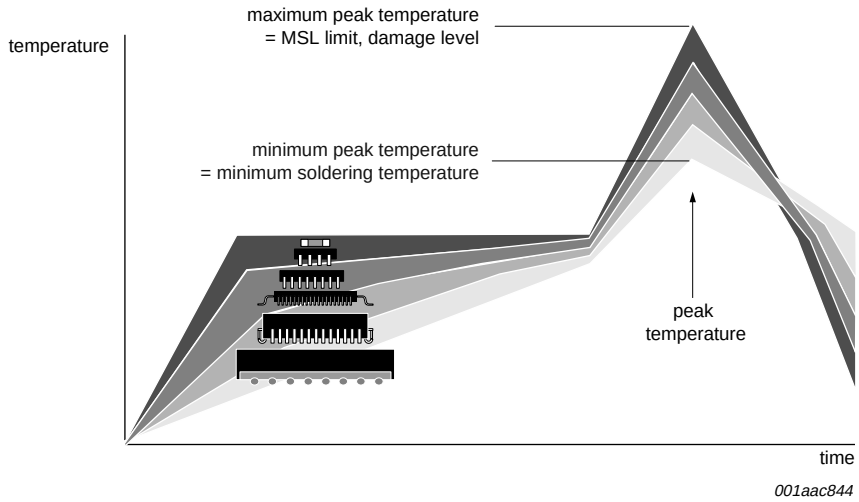
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 27. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 28. Abbreviations

Acronym	Description
CPU	Central Processing Unit
DLL	Divisor Latch LSB
DLM	Divisor Latch MSB
DMA	Direct Memory Access
FIFO	First In, First Out
ISDN	Integrated Service Digital Network
LSB	Least Significant Bit
MSB	Most Significant Bit
UART	Universal Asynchronous Receiver and Transmitter

14. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC16C2552B_3	20090212	Product data sheet	-	SC16C2552B-02

Modifications:

- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.
- Legal texts have been adapted to the new company name where appropriate.
- Section 2 “Features”:
  - added (new) 5th bullet item
  - added Footnote 1
- Figure 1: changed signal names from “MFA, MFB” to “$\overline{MFA}$, $\overline{MFB}$”
- Section 7.3.1 “DMA mode”:
  - 1st paragraph, last sentence: changed from “MF register” to “AFR[2:1]”
  - 2nd paragraph, last sentence: changed from “MF register” to “AFR[2:1]”
- Table 18 “Modem Status Register bits description”:
  - description of bit 7: changed from “($\overline{OPA}$/OPB)” to “($\overline{OP2A}$/$\overline{OP2B}$)”
  - description of bit 6: changed from “($\overline{OP1}$)” to “($\overline{OP1A}$/$\overline{OP2A}$)”
- Table 23 “Limiting values”:
  - symbol V_n split to show 2 separate conditions: “at D7 to D0 pins” and “at input only pins”
  - changed symbol “$P_{tot(pack)}$” to “P_{tot}/pack”
- Table 24 “Static characteristics”:
  - descriptive line below table title changed from “V_{CC} = 2.5 V, 3.3 V or 5.0 V ± 10 %” to “tolerance of V_{CC} ± 10 %”
  - changed symbol/parameter from “$V_{IL(CK)}$, LOW-level clock input voltage” to “$V_{IL(clk)}$, clock LOW-level input voltage”
  - changed symbol/parameter from “$V_{IH(CK)}$, HIGH-level clock input voltage” to “$V_{IH(clk)}$, clock HIGH-level input voltage”
  - changed symbol/parameter from “I_{CL}, clock leakage” to “$I_{L(clk)}$, clock leakage current”
  - Table note [1]: changed from “Except x_2” to “Except XTAL2”
- Table 25 “Dynamic characteristics”:
  - descriptive line below table title changed from “V_{CC} = 2.5 V, 3.3 V or 5.0 V ± 10 %” to “tolerance of V_{CC} ± 10 %”
  - changed symbol “t_{1w}, t_{2w}” to 2 separate symbols “t_{WH}” and “t_{WL}”
  - changed symbol/parameter “t_{3w}, clock frequency” to “f_{XTAL1}, frequency on pin XTAL1”
  - added Table note [2]
  - symbols t_{20d}, t_{23d}, t_{25d} and t_{28d}: Unit changed from “R_{clk}” to “s” (second)
  - symbols t_{20d}, t_{23d}, t_{25d} and t_{28d}: appended “T_{RCLK}” to Min and Max values
  - added Table note [3]
  - symbol N: removed “R_{clk}” from Unit column (N is a number)
  - added Table note [4] and its reference at t_{RESET}

Table 29. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications: (continued)	• Section 10.1 “Timing diagrams”: – Figure 7, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14: appended (channel) “A” and/or “B” to signal names – Figure 8 “External clock timing”: changed symbols “t_{1w}, t_{2w}, t_{3w}” to “t_{WH}, t_{WL}, $t_{w(clk)}$”, respectively – Figure 8 “External clock timing”: added equation – Figure 10, Figure 11, Figure 13, Figure 14: at the top of these drawings, changed phrase from “DATA BITS (5-8)” to “data bits (0 to 7)” • updated soldering information • added Section 13 “Abbreviations”			
SC16C2552B-02 (9397 750 14442)	20041213	Product data	-	SC16C2552B-01
SC16C2552B-01 (9397 750 11966)	20040330	Product data	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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