



# PCA9505/06

40-bit I<sup>2</sup>C-bus I/O port with  $\overline{\text{RESET}}$ ,  $\overline{\text{OE}}$  and  $\overline{\text{INT}}$

Rev. 03 — 6 June 2007

Product data sheet

## 1. General description

The PCA9505/PCA9506 provide 40-bit parallel input/output (I/O) port expansion for I<sup>2</sup>C-bus applications organized in 5 banks of 8 I/Os. At 5 V supply voltage, the outputs are capable of sourcing 10 mA and sinking 15 mA with a total package load of 600 mA to allow direct driving of 40 LEDs. Any of the 40 I/O ports can be configured as an input or output. Output ports are totem-pole and their logic state changes at the Acknowledge (bank change). The PCA9505 is identical to the PCA9506 except that it includes 100 k $\Omega$  internal pull-up resistors on all the I/Os. The PCA9506 does not include the internal pull-ups on the I/Os to reduce power consumption when used as outputs or when the input is driven by a push-pull driver.

The device can be configured to have each input port to be masked in order to prevent it from generating interrupts when its state changes and to have the I/O data logic state to be inverted when read by the system master.

An open-drain interrupt ( $\overline{\text{INT}}$ ) output pin allows monitoring of the input pins and is asserted each time a change occurs in one or several input ports (unless masked).

The Output Enable ( $\overline{\text{OE}}$ ) pin 3-states any I/O selected as an output and can be used as an input signal to blink or dim LEDs (PWM with frequency > 80 Hz and change duty cycle).

The internal Power-On Reset (POR) or hardware reset ( $\overline{\text{RESET}}$ ) pin initializes the 40 I/Os as inputs. Three address select pins configure one of 8 slave addresses.

The PCA9506 is available in 56-pin TSSOP and HVQFN packages, while the PCA9505 is available only in a TSSOP package. They are both specified over the -40 °C to +85 °C industrial temperature range.

## 2. Features

- Standard mode (100 kHz) and Fast mode (400 kHz) compatible I<sup>2</sup>C-bus serial interface
- 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- 40 configurable I/O pins that default to inputs at power-up
- PCA9505 includes 100 k $\Omega$  internal pull-up resistors on all the I/Os
- Outputs:
  - ◆ Totem-pole (10 mA source, 15 mA sink) with controlled edge rate output structure
  - ◆ Active LOW output enable ( $\overline{\text{OE}}$ ) input pin 3-states all outputs
  - ◆ Output state change on Acknowledge
  - ◆ Open-drain active LOW interrupt ( $\overline{\text{INT}}$ ) output pin allows monitoring of logic level change of pins programmed as inputs

- Inputs:
  - ◆ Programmable Interrupt Mask Control for input pins that do not require an interrupt when their states change
  - ◆ Polarity Inversion register allows inversion of the polarity of the I/O pins when read
- Active LOW reset ( $\overline{\text{RESET}}$ ) input pin resets device to power-up default state
- 3 programmable address pins allowing 8 devices on the same bus
- Designed for live insertion
  - ◆ Minimize line disturbance ( $I_{\text{OFF}}$  and power-up 3-state)
  - ◆ Signal transient rejection (50 ns noise filter and robust I<sup>2</sup>C-bus state machine)
- Low standby current
- -40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA
- Offered in TSSOP56 (PCA9505, PCA9506) and HVQFN56 (PCA9506) packages

### 3. Applications

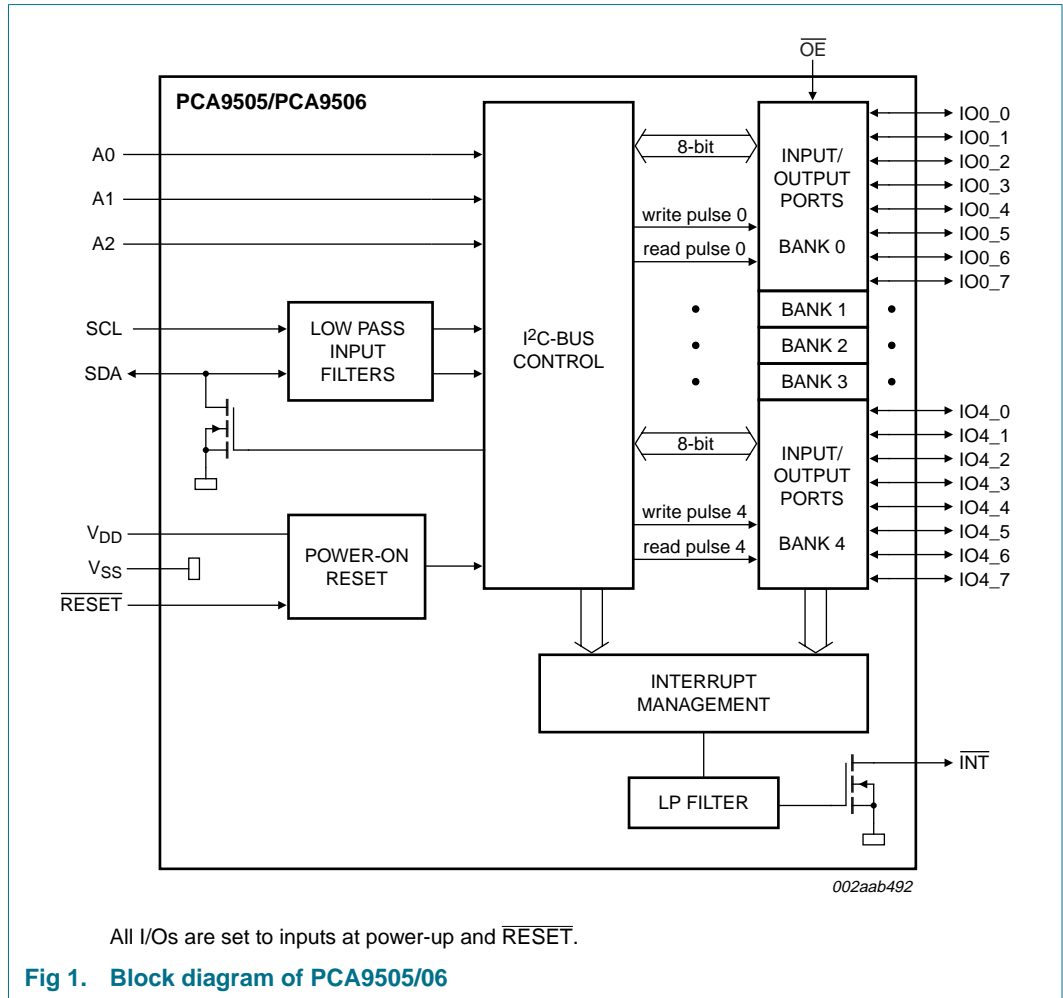
- Servers
- RAID systems
- Industrial control
- Medical equipment
- PLCs
- Cell phones
- Gaming machines
- Instrumentation and test measurement

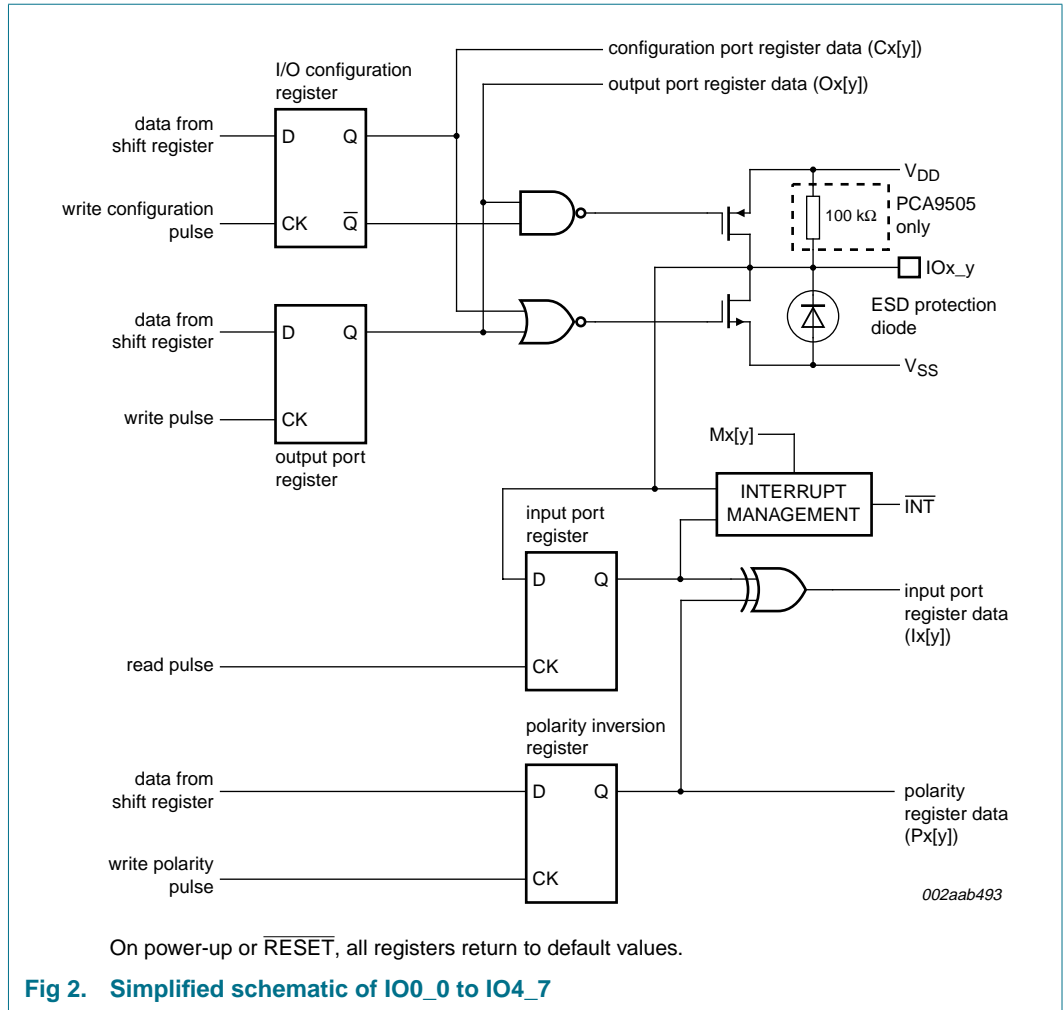
### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9505DGG	PCA9505DGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCA9506DGG	PCA9506DGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCA9506BS	PCA9506BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-1

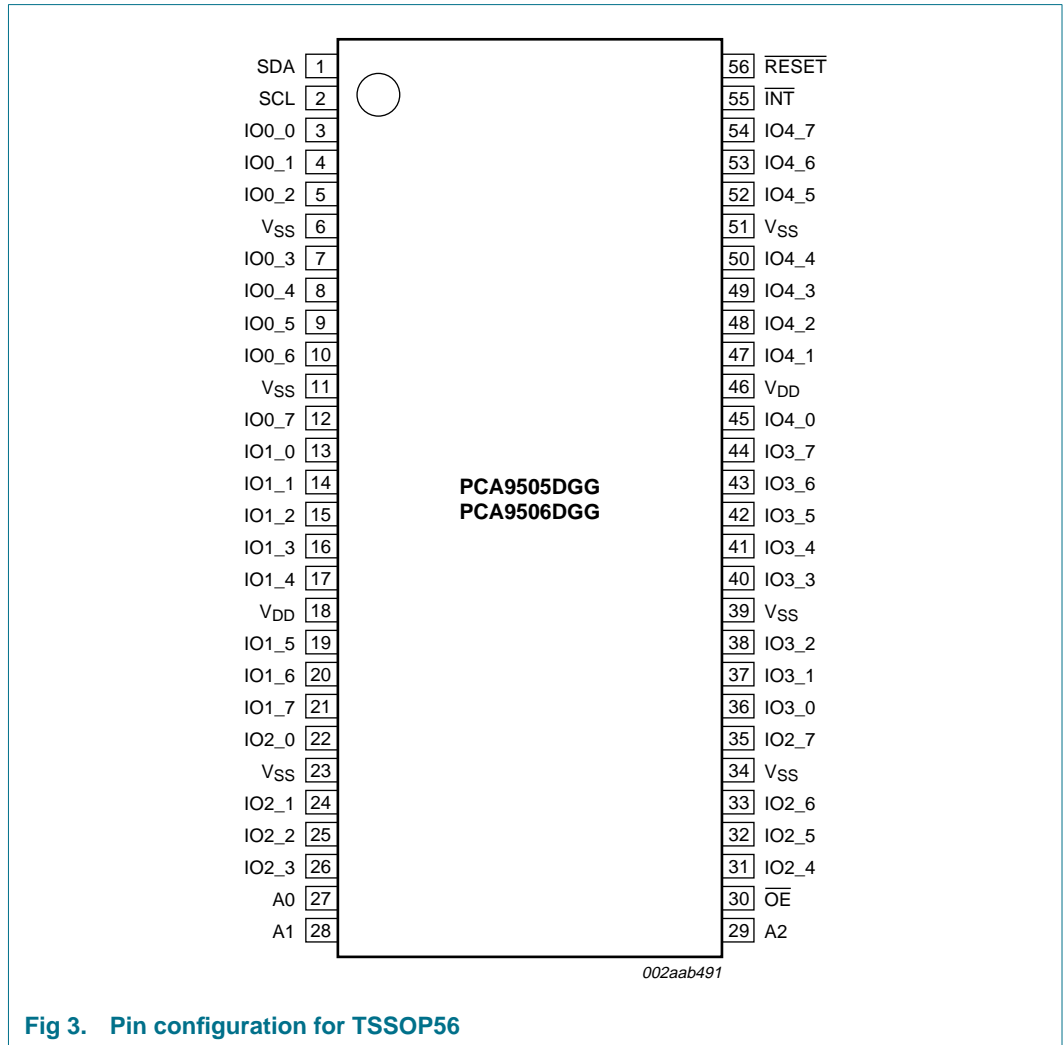
5. Block diagram

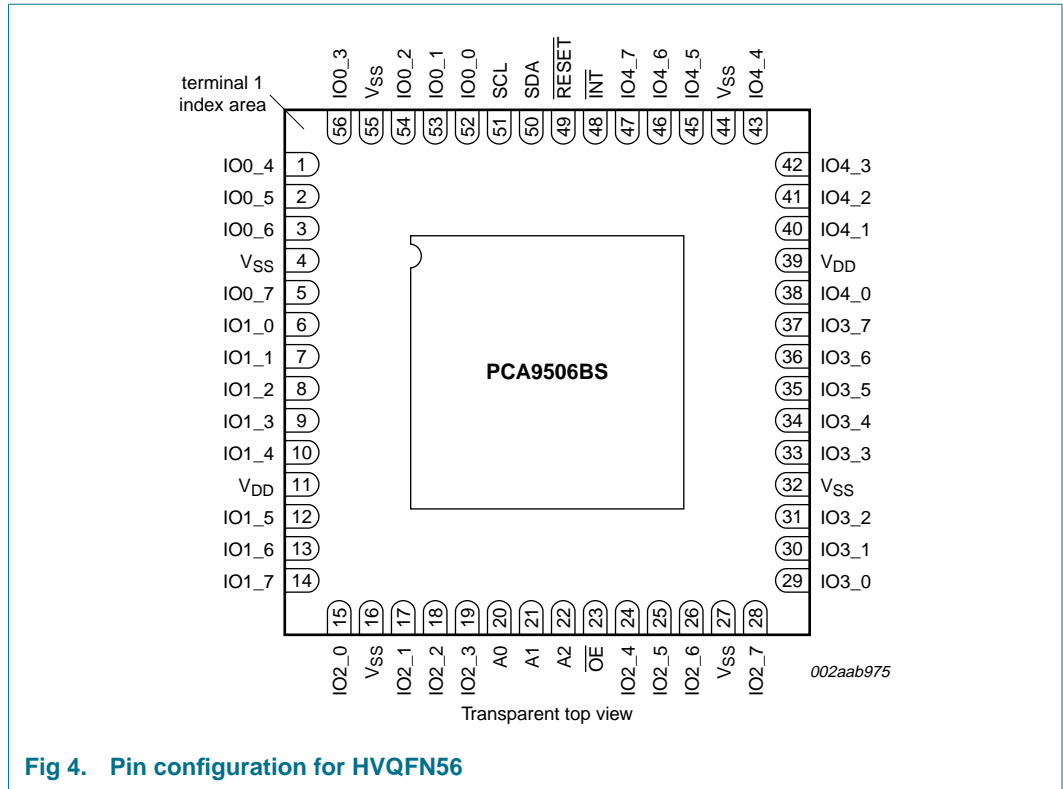




## 6. Pinning information

### 6.1 Pinning





## 6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	TSSOP56	HVQFN56		
SDA	1	50	I/O	serial data line
SCL	2	51	I	serial clock line
IO0_0 to IO0_7	3, 4, 5, 7, 8, 9, 10, 12	52, 53, 54, 56, 1, 2, 3, 5	I/O	input/output bank 0
IO1_0 to IO1_7	13, 14, 15, 16, 17, 19, 20, 21	6, 7, 8, 9, 10, 12, 13, 14	I/O	input/output bank 1
IO2_0 to IO2_7	22, 24, 25, 26, 31, 32, 33, 35	15, 17, 18, 19, 24, 25, 26, 28	I/O	input/output bank 2
IO3_0 to IO3_7	36, 37, 38, 40, 41, 42, 43, 44	29, 30, 31, 33, 34, 35, 36, 37	I/O	input/output bank 3
IO4_0 to IO4_7	45, 47, 48, 49, 50, 52, 53, 54	38, 40, 41, 42, 43, 45, 46, 47	I/O	input/output bank 4
V <sub>SS</sub>	6, 11, 23, 34, 39, 51	4, 16, 27, 32, 44, 55	power supply	ground supply voltage
V <sub>DD</sub>	18, 46	11, 39	power supply	supply voltage
A0	27	20	I	address input 0
A1	28	21	I	address input 1
A2	29	22	I	address input 2

Table 2. Pin description ...continued

Symbol	Pin		Type	Description
	TSSOP56	HVQFN56		
$\overline{\text{OE}}$	30	23	I	active LOW output enable input
$\overline{\text{INT}}$	55	48	O	active LOW interrupt output
$\overline{\text{RESET}}$	56	49	I	active LOW reset input

[1] HVQFN package die supply ground is connected to both V<sub>SS</sub> pins and exposed center pad. V<sub>SS</sub> pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

## 7. Functional description

Refer to [Figure 1 “Block diagram of PCA9505/06”](#) and [Figure 2 “Simplified schematic of IO0\\_0 to IO4\\_7”](#).

### 7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9505/06 is shown in [Figure 5](#). Slave address pins A2, A1, and A0 choose 1 of 8 slave addresses and need to be connected to V<sub>DD</sub> (1) or V<sub>SS</sub> (0). To conserve power, no internal pull-up resistors are incorporated on A2, A1, and A0.

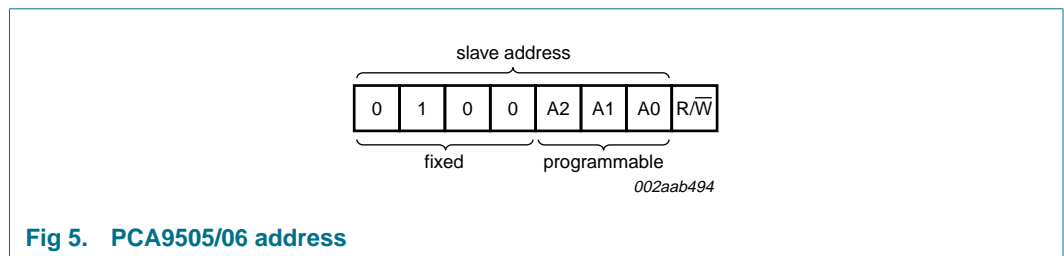


Fig 5. PCA9505/06 address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

### 7.2 Command register

Following the successful acknowledgement of the slave address + R/W bit, the bus master will send a byte to the PCA9505/06, which will be stored in the Command register.

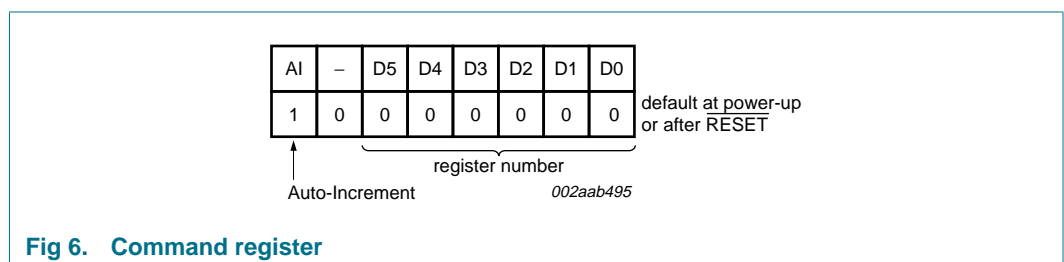


Fig 6. Command register

The lowest 6 bits are used as a pointer to determine which register will be accessed. The registers are:

- IP: Input Port registers (5 registers)
- OP: Output Port registers (5 registers)
- PI: Polarity Inversion registers (5 registers)
- IOC: I/O Configuration registers (5 registers)
- MSK: Mask interrupt registers (5 registers)

If the Auto-Increment flag is set ( $\text{AI} = 1$ ), the 3 least significant bits are automatically incremented after a read or write. This allows the user to program and/or read the 5 register banks sequentially.

If more than 5 bytes of data are written and  $\text{AI} = 1$ , previous data in the selected registers will be overwritten. Reserved registers are skipped and not accessed (refer to [Table 3](#)).

If the Auto-Increment flag is cleared ( $\text{AI} = 0$ ), the 3 least significant bits are not incremented after data is read or written. During a read operation, the same register bank is read each time. During a write operation, data is written to the same register bank each time.

Only a Command register code with the 5 least significant bits equal to the 25 allowable values as defined in [Table 3](#) are valid. Reserved or undefined command codes must not be accessed for proper device functionality. At power-up, this register defaults to 0x80, with the AI bit set to logic 1, and the lowest 7 bits set to logic 0.

During a write operation, the PCA9505/06 will acknowledge a byte sent to OPx, PIx, and IOCx and MSKx registers, but will not acknowledge a byte sent to the IPx registers since these are read-only registers.



### 7.3 Register definitions

Table 3. Register summary

Register # (hex)	D5	D4	D3	D2	D1	D0	Symbol	Access	Description
<b>Input Port registers</b>									
00	0	0	0	0	0	0	IP0	read only	Input Port register bank 0
01	0	0	0	0	0	1	IP1	read only	Input Port register bank 1
02	0	0	0	0	1	0	IP2	read only	Input Port register bank 2
03	0	0	0	0	1	1	IP3	read only	Input Port register bank 3
04	0	0	0	1	0	0	IP4	read only	Input Port register bank 4
05	0	0	0	1	0	1	-	-	reserved for future use
06	0	0	0	1	1	0	-	-	reserved for future use
07	0	0	0	1	1	1	-	-	reserved for future use
<b>Output Port registers</b>									
08	0	0	1	0	0	0	OP0	read/write	Output Port register bank 0
09	0	0	1	0	0	1	OP1	read/write	Output Port register bank 1
0A	0	0	1	0	1	0	OP2	read/write	Output Port register bank 2
0B	0	0	1	0	1	1	OP3	read/write	Output Port register bank 3
0C	0	0	1	1	0	0	OP4	read/write	Output Port register bank 4
0D	0	0	1	1	0	1	-	-	reserved for future use
0E	0	0	1	1	1	0	-	-	reserved for future use
0F	0	0	1	1	1	1	-	-	reserved for future use
<b>Polarity Inversion registers</b>									
10	0	1	0	0	0	0	PI0	read/write	Polarity Inversion register bank 0
11	0	1	0	0	0	1	PI1	read/write	Polarity Inversion register bank 1
12	0	1	0	0	1	0	PI2	read/write	Polarity Inversion register bank 2
13	0	1	0	0	1	1	PI3	read/write	Polarity Inversion register bank 3
14	0	1	0	1	0	0	PI4	read/write	Polarity Inversion register bank 4
15	0	1	0	1	0	1	-	-	reserved for future use
16	0	1	0	1	1	0	-	-	reserved for future use
17	0	1	0	1	1	1	-	-	reserved for future use
<b>I/O Configuration registers</b>									
18	0	1	1	0	0	0	IOC0	read/write	I/O Configuration register bank 0
19	0	1	1	0	0	1	IOC1	read/write	I/O Configuration register bank 1
1A	0	1	1	0	1	0	IOC2	read/write	I/O Configuration register bank 2
1B	0	1	1	0	1	1	IOC3	read/write	I/O Configuration register bank 3
1C	0	1	1	1	0	0	IOC4	read/write	I/O Configuration register bank 4
1D	0	1	1	1	0	1	-	-	reserved for future use
1E	0	1	1	1	1	0	-	-	reserved for future use
1F	0	1	1	1	1	1	-	-	reserved for future use

Table 3. Register summary ...continued

Register # (hex)	D5	D4	D3	D2	D1	D0	Symbol	Access	Description
<b>Mask Interrupt registers</b>									
20	1	0	0	0	0	0	MSK0	read/write	Mask Interrupt register bank 0
21	1	0	0	0	0	1	MSK1	read/write	Mask Interrupt register bank 1
22	1	0	0	0	1	0	MSK2	read/write	Mask Interrupt register bank 2
23	1	0	0	0	1	1	MSK3	read/write	Mask Interrupt register bank 3
24	1	0	0	1	0	0	MSK4	read/write	Mask Interrupt register bank 4
25	1	0	0	1	0	1	-	-	reserved for future use
26	1	0	0	1	1	0	-	-	reserved for future use
27	1	0	0	1	1	1	-	-	reserved for future use

### 7.3.1 IP0 to IP4 - Input Port registers

These registers are read-only. They reflect the incoming logic levels of the port pins regardless of whether the pin is defined as an input or an output by the I/O Configuration register. If the corresponding P<sub>x</sub>[y] bit in the PI registers is set to logic 0, or the inverted incoming logic levels if the corresponding P<sub>x</sub>[y] bit in the PI register is set to logic 1. Writes to these registers have no effect.

Table 4. IP0 to IP4 - Input Port registers (address 00h to 04h) bit description

Legend: \* default value 'X' determined by the externally applied logic level.

Address	Register	Bit	Symbol	Access	Value	Description
00h	IP0	7 to 0	I0[7:0]	R	XXXX XXXX*	Input Port register bank 0
01h	IP1	7 to 0	I1[7:0]	R	XXXX XXXX*	Input Port register bank 1
02h	IP2	7 to 0	I2[7:0]	R	XXXX XXXX*	Input Port register bank 2
03h	IP3	7 to 0	I3[7:0]	R	XXXX XXXX*	Input Port register bank 3
04h	IP4	7 to 0	I4[7:0]	R	XXXX XXXX*	Input Port register bank 4

The Polarity Inversion register can invert the logic states of the port pins. The polarity of the corresponding bit is inverted when P<sub>x</sub>[y] bit in the PI register is set to logic 1. The polarity of the corresponding bit is not inverted when P<sub>x</sub>[y] bits in the PI register is set to logic 0.

### 7.3.2 OP0 to OP4 - Output Port registers

These registers reflect the outgoing logic levels of the pins defined as outputs by the I/O Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the values that are in the flip-flops controlling the output selection, **not** the actual pin values.

$Ox[y] = 0$ : IOx\_y = 0 if IOx\_y defined as output (Cx[y] in IOC register = 0).

$Ox[y] = 1$ : IOx\_y = 1 if IOx\_y defined as output (Cx[y] in IOC register = 0).

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

**Table 5. OP0 to OP4 - Output Port registers (address 08h to 0Ch) bit description**

Legend: \* default value.

Address	Register	Bit	Symbol	Access	Value	Description
08h	OP0	7 to 0	O0[7:0]	R/W	0000 0000*	Output Port register bank 0
09h	OP1	7 to 0	O1[7:0]	R/W	0000 0000*	Output Port register bank 1
0Ah	OP2	7 to 0	O2[7:0]	R/W	0000 0000*	Output Port register bank 2
0Bh	OP3	7 to 0	O3[7:0]	R/W	0000 0000*	Output Port register bank 3
0Ch	OP4	7 to 0	O4[7:0]	R/W	0000 0000*	Output Port register bank 4

### 7.3.3 PI0 to PI4 - Polarity Inversion registers

These registers allow inversion of the polarity of the corresponding Input Port register.

$Px[y] = 0$ : The corresponding Input Port register data polarity is retained.

$Px[y] = 1$ : The corresponding Input Port register data polarity is inverted.

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

**Table 6. PI0 to PI4 - Polarity Inversion registers (address 10h to 14h) bit description**

Legend: \* default value.

Address	Register	Bit	Symbol	Access	Value	Description
10h	PI0	7 to 0	P0[7:0]	R/W	0000 0000*	Polarity Inversion register bank 0
11h	PI1	7 to 0	P1[7:0]	R/W	0000 0000*	Polarity Inversion register bank 1
12h	PI2	7 to 0	P2[7:0]	R/W	0000 0000*	Polarity Inversion register bank 2
13h	PI3	7 to 0	P3[7:0]	R/W	0000 0000*	Polarity Inversion register bank 3
14h	PI4	7 to 0	P4[7:0]	R/W	0000 0000*	Polarity Inversion register bank 4

### 7.3.4 IOC0 to IOC4 - I/O Configuration registers

These registers configure the direction of the I/O pins.

Cx[y] = 0: The corresponding port pin is an output.

Cx[y] = 1: The corresponding port pin is an input.

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

**Table 7. IOC0 to IOC4 - I/O Configuration registers (address 18h to 1Ch) bit description**

Legend: \* default value.

Address	Register	Bit	Symbol	Access	Value	Description
18h	IOC0	7 to 0	C0[7:0]	R/W	1111 1111*	I/O Configuration register bank 0
19h	IOC1	7 to 0	C1[7:0]	R/W	1111 1111*	I/O Configuration register bank 1
1Ah	IOC2	7 to 0	C2[7:0]	R/W	1111 1111*	I/O Configuration register bank 2
1Bh	IOC3	7 to 0	C3[7:0]	R/W	1111 1111*	I/O Configuration register bank 3
1Ch	IOC4	7 to 0	C4[7:0]	R/W	1111 1111*	I/O Configuration register bank 4

### 7.3.5 MSK0 to MSK4 - Mask interrupt registers

These registers mask the interrupt due to a change in the I/O pins configured as inputs. 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Mx[y] = 0: A level change at the I/O will generate an interrupt if IOx\_y defined as input (Cx[y] in IOC register = 1).

Mx[y] = 1: A level change in the input port will not generate an interrupt if IOx\_y defined as input (Cx[y] in IOC register = 1).

**Table 8. MSK0 to MSK4 - Mask interrupt registers (address 20h to 24h) bit description**

Legend: \* default value.

Address	Register	Bit	Symbol	Access	Value	Description
20h	MSK0	7 to 0	M0[7:0]	R/W	1111 1111*	Mask Interrupt register bank 0
21h	MSK1	7 to 0	M1[7:0]	R/W	1111 1111*	Mask Interrupt register bank 1
22h	MSK2	7 to 0	M2[7:0]	R/W	1111 1111*	Mask Interrupt register bank 2
23h	MSK3	7 to 0	M3[7:0]	R/W	1111 1111*	Mask Interrupt register bank 3
24h	MSK4	7 to 0	M4[7:0]	R/W	1111 1111*	Mask Interrupt register bank 4

## 7.4 Power-on reset

When power is applied to V<sub>DD</sub>, an internal Power-On Reset (POR) holds the PCA9505/06 in a reset condition until V<sub>DD</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9505/06 registers and I<sup>2</sup>C-bus state machine will initialize to their default states. Thereafter, V<sub>DD</sub> must be lowered below 0.2 V to reset the device.

## 7.5 $\overline{\text{RESET}}$ input

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of t<sub>w(rst)</sub>. The PCA9505/06 registers and I<sup>2</sup>C-bus state machine will be held in their default states until the  $\overline{\text{RESET}}$  input is once again HIGH.

## 7.6 Interrupt output ( $\overline{\text{INT}}$ )

The open-drain active LOW interrupt is activated when one of the port pins changes state and the port pin is configured as an input and the interrupt on it is not masked. The interrupt is deactivated when the port pin input returns to its previous state or the Input Port register is read.

**Remark:** Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

Only a read of the Input Port register that contains the bit(s) image of the input(s) that generated the interrupt clears the interrupt condition.

If more than one input register changed state before a read of the Input Port register is initiated, the interrupt is cleared when all the input registers containing all the inputs that changed are read.

Example: If IO0\_5, IO2\_3, and IO3\_7 change state at the same time, the interrupt is cleared only when INREG0, INREG2, and INREG3 are read.

## 7.7 Output enable input ( $\overline{\text{OE}}$ )

The active LOW output enable pin allows to enable or disable all the I/Os at the same time. When a LOW level is applied to the  $\overline{\text{OE}}$  pin, all the I/Os configured as outputs are enabled and the logic value programmed in their respective OP registers is applied to the pins. When a HIGH level is applied to the  $\overline{\text{OE}}$  pin, all the I/Os configured as outputs are 3-stated.

For applications requiring LED blinking with brightness control, this pin can be used to control the brightness by applying a high frequency PWM signal on the  $\overline{\text{OE}}$  pin. LEDs can be blinked using the Output Port registers and can be dimmed using the PWM signal on the  $\overline{\text{OE}}$  pin thus controlling the brightness by adjusting the duty cycle.

## 7.8 Live insertion

The PCA9505/06 are fully specified for live insertion applications using I<sub>OFF</sub>, power-up 3-states, robust state machine, and 50 ns noise filter. The I<sub>OFF</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state's circuitry places the outputs in the high-impedance state during power-up and power-down, which prevents driver conflict and bus contention.

The robust state machine does not respond until it sees a valid START condition and the 50 ns noise filter will filter out any insertion glitches. The PCA9505/06 will not cause corruption of active data on the bus, nor will the device be damaged or cause damage to devices already on the bus when similar featured devices are being used.

## 7.9 Standby

The PCA9505/06 goes into standby when the I<sup>2</sup>C-bus is idle. Standby supply current is lower than 1  $\mu\text{A}$  (typical).

## 8. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 7](#)).

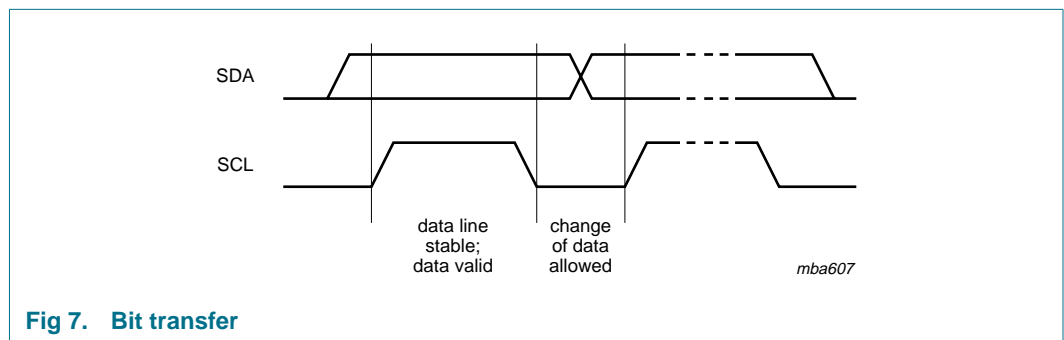


Fig 7. Bit transfer

#### 8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 8](#)).

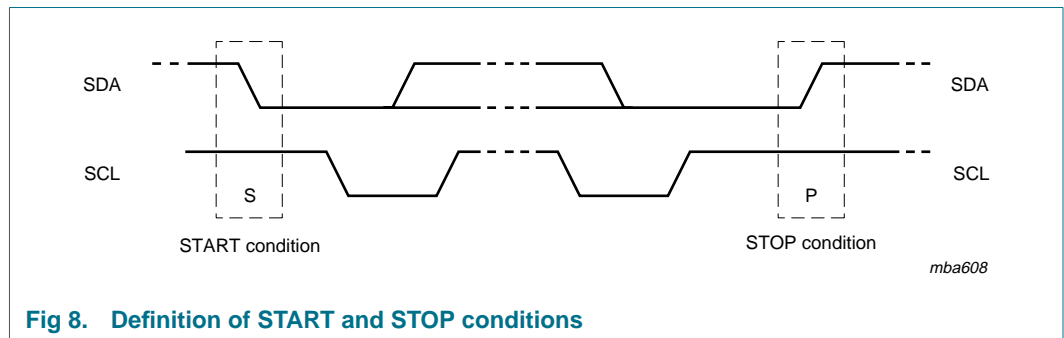


Fig 8. Definition of START and STOP conditions

### 8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 9](#)).

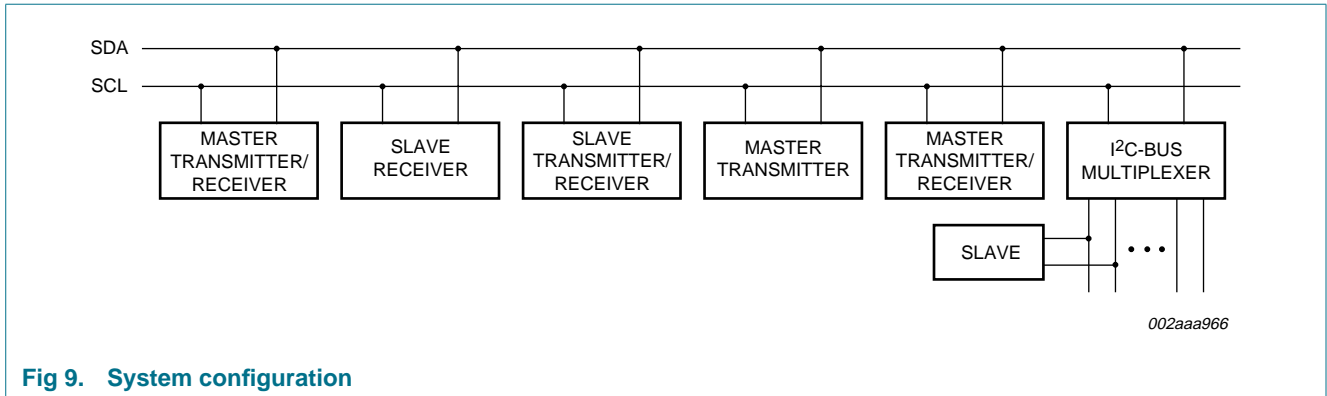


Fig 9. System configuration

### 8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

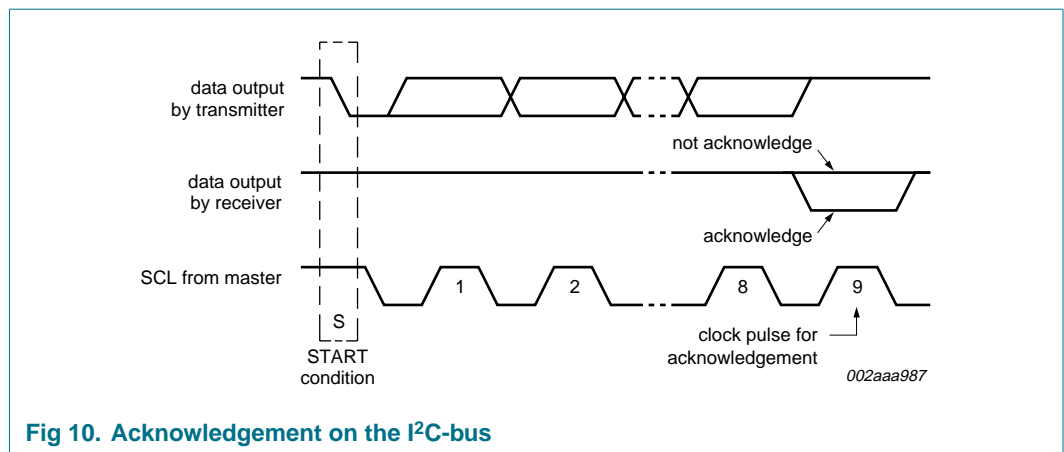
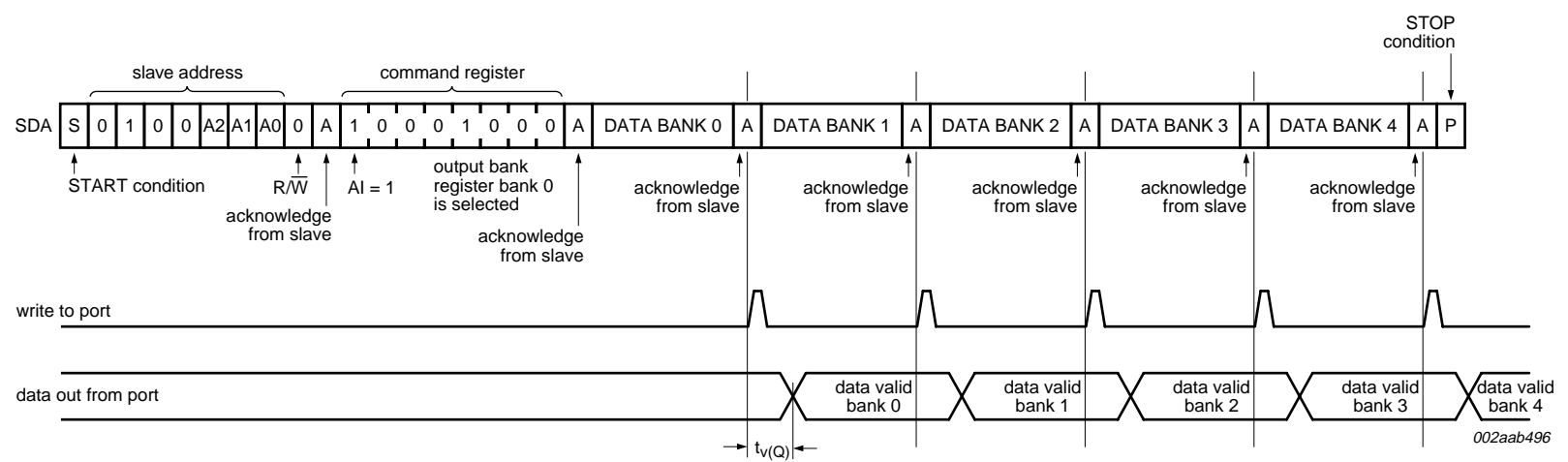


Fig 10. Acknowledgement on the I<sup>2</sup>C-bus

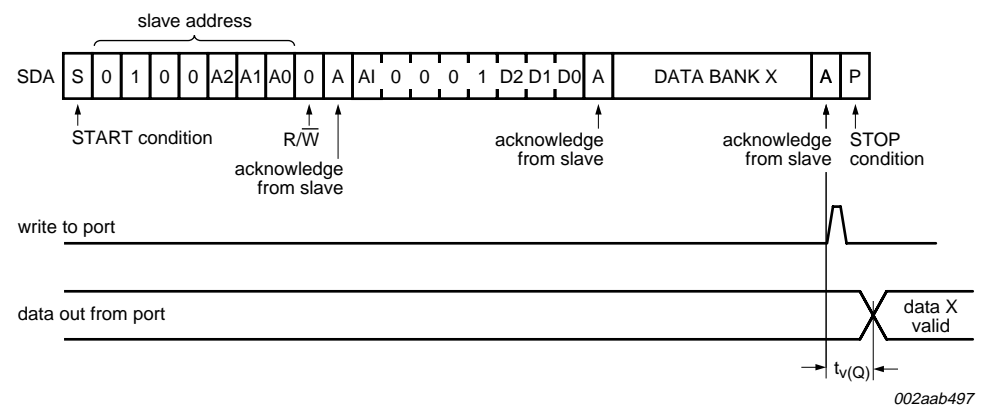
### 8.4 Bus transactions

Data is transmitted to the PCA9505/06 registers using Write Byte transfers (see [Figure 11](#), [Figure 12](#), and [Figure 13](#)). Data is read from the PCA9505/06 registers using Read and Receive Byte transfers (see [Figure 14](#)).



$\overline{\text{OE}}$  is LOW to observe a change in the outputs.  
 If more than 5 bytes are written, previous data are overwritten.

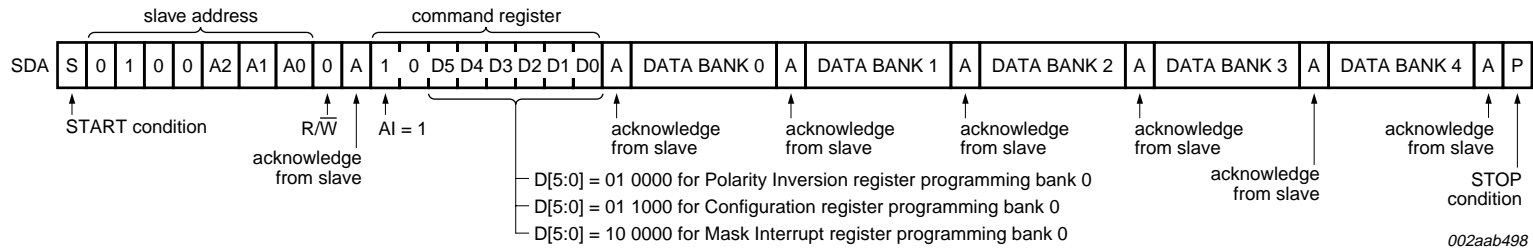
Fig 11. Write to the 5 output ports



$\overline{\text{OE}}$  is LOW to observe a change in the outputs.  
 Two, three, or four adjacent banks can be programmed by using the Auto-Increment feature (AI = 1) and change at the corresponding output port becomes effective at each acknowledge.

Fig 12. Write to a specific output port



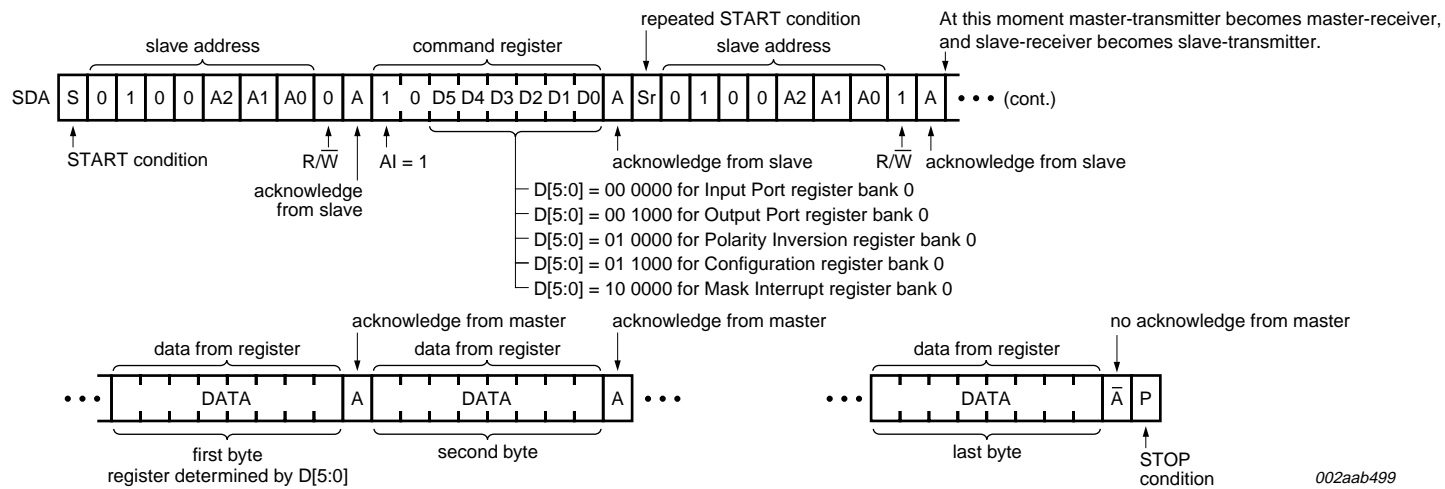


The programming becomes effective at the acknowledge.

Less than 5 bytes can be programmed by using this scheme. D5, D4, D3, D2, D1, D0 refers to the first register to be programmed.

If more than 5 bytes are written, previous data are overwritten (the sixth Configuration register will roll over to the first addressed Configuration register, the sixth Polarity Inversion register will roll over to the first addressed Polarity Inversion register and the sixth Mask Interrupt register will roll over to the first addressed Mask Interrupt register).

Fig 13. Write to the I/O Configuration, Polarity Inversion or Mask Interrupt registers



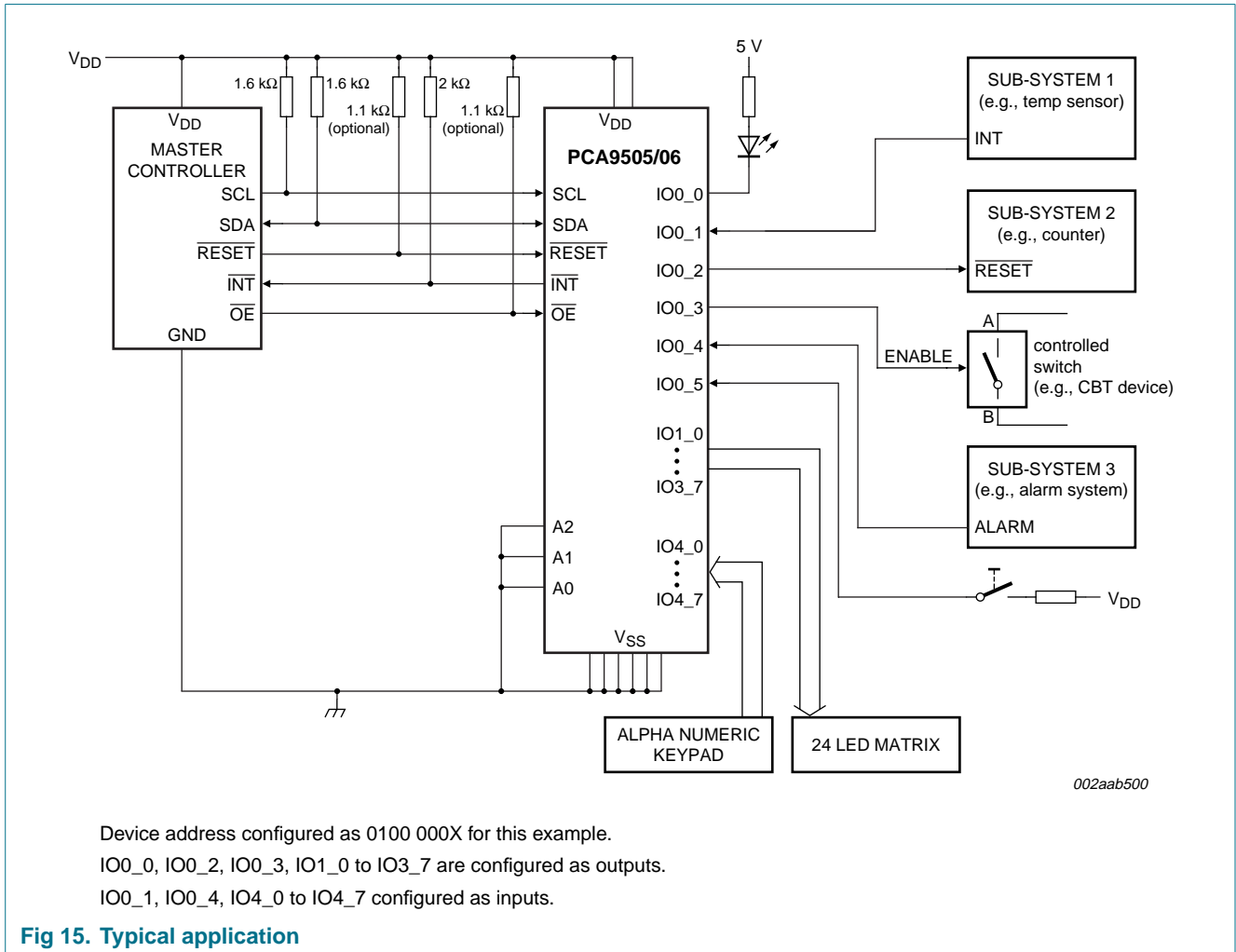
If AI = 0, the same register is read during the whole sequence.

If AI = 1, the register value is incremented after each read. When the last register bank is read, it rolls over to the first byte of the category (see category definition in [Section 7.2 "Command register"](#)).

The  $\overline{\text{INT}}$  signal is released only when the last register containing an input that changed has been read. For example, when IO2\_4 and IO4\_7 change at the same time and an Input Port register's read sequence is initiated, starting with IP0,  $\overline{\text{INT}}$  is released after IP4 is read (and not after IP2 is read).

Fig 14. Read from Input Port, Output Port, I/O Configuration, Polarity Inversion or Mask Interrupt registers

9. Application design-in information



## 10. Limiting values

**Table 9. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6	V
V <sub>I</sub>	input voltage		V <sub>SS</sub> - 0.5	5.5	V
I <sub>I</sub>	input current		-	±20	mA
V <sub>I/O(n)</sub>	input/output voltage on any other pin		V <sub>SS</sub> - 0.5	5.5	V
V <sub>I/O(IO0n)</sub>	input/output voltage on pin IO0_n		V <sub>SS</sub> - 0.5	5.5	V
I <sub>O(I/O<sub>n</sub>)</sub>	output current on an I/O pin		-20	+50	mA
I <sub>DD</sub>	supply current		-	500	mA
I <sub>SS</sub>	ground supply current		-	1100	mA
P <sub>tot</sub>	total power dissipation		-	500	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature	operating	-40	+85	°C
T <sub>j</sub>	junction temperature	operating	-	125	°C
		storage	-	150	°C

## 11. Static characteristics

**Table 10. Static characteristics**

V<sub>DD</sub> = 2.3 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Supply</b>							
V <sub>DD</sub>	supply voltage		2.3	-	5.5	V	
I <sub>DD</sub>	supply current	PCA9506 only; operating mode; no load; f <sub>SCL</sub> = 400 kHz					
		V <sub>DD</sub> = 2.3 V	-	56	95	μA	
		V <sub>DD</sub> = 3.3 V	-	98	150	μA	
		V <sub>DD</sub> = 5.5 V	-	225	300	μA	
		PCA9505 only; operating mode; no load; f <sub>SCL</sub> = 400 kHz					
		V <sub>DD</sub> = 2.3 V	-	1	1.5	mA	
		V <sub>DD</sub> = 3.3 V	-	1.5	2	mA	
		V <sub>DD</sub> = 5.5 V	-	2.7	3.5	mA	
		I <sub>stbH</sub>	HIGH-level standby current	no load; f <sub>SCL</sub> = 0 kHz; I/O = inputs; V <sub>I</sub> = V <sub>DD</sub>			
V <sub>DD</sub> = 2.3 V	-			0.15	11	μA	
V <sub>DD</sub> = 3.3 V	-			0.25	12	μA	
V <sub>DD</sub> = 5.5 V	-			0.75	15.5	μA	
I <sub>stbL</sub>	LOW-level standby current	PCA9505 only	-	2	5	μA	
V <sub>POR</sub>	power-on reset voltage <sup>[1]</sup>	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	1.70	2.0	V	

**Table 10. Static characteristics ...continued**

$V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4 \text{ V}$	20	-	-	mA
$I_L$	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$	-	5	10	pF
<b>I/Os</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.8	V
$V_{IH}$	HIGH-level input voltage		2	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.5 \text{ V}$				
		$V_{DD} = 2.3 \text{ V}$	10	-	-	mA
		$V_{DD} = 3.0 \text{ V}$	12	-	-	mA
		$V_{DD} = 4.5 \text{ V}$	15	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	$V_{OL} = 0.5 \text{ V}$ ; $V_{DD} = 4.5 \text{ V}$	-	-	0.6	A
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -10 \text{ mA}$				
		$V_{DD} = 2.3 \text{ V}$	1.6	-	-	V
		$V_{DD} = 3.0 \text{ V}$	2.3	-	-	V
		$V_{DD} = 4.5 \text{ V}$	4.0	-	-	V
$I_{LIH}$	HIGH-level input leakage current	$V_{DD} = 3.6 \text{ V}$ ; $V_I = V_{DD}$	-1	-	+1	$\mu\text{A}$
$I_{LIL}$	LOW-level input leakage current	$V_{DD} = 5.5 \text{ V}$ ; $V_I = V_{SS}$				
		PCA9506 only	-1	-	+1	$\mu\text{A}$
		PCA9505 only	-100	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	6	7	pF
$C_o$	output capacitance		-	6	7	pF
<b>Interrupt <math>\overline{\text{INT}}</math></b>						
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4 \text{ V}$	6	-	-	mA
$I_{OH}$	HIGH-level output current		-1	-	+1	$\mu\text{A}$
$C_o$	output capacitance		-	3.0	5	pF
<b>Inputs <math>\overline{\text{RESET}}</math> and <math>\overline{\text{OE}}</math></b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.8	V
$V_{IH}$	HIGH-level input voltage		2	-	5.5	V
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	3.0	5	pF
<b>Inputs A0, A1, A2</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	3.5	5	pF

[1]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.

## 12. Dynamic characteristics

Table 11. Dynamic characteristics

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency	[1]	0	100	0	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>HD;DAT</sub>	data hold time		0	-	0	-	ns
t <sub>VD;ACK</sub>	data valid acknowledge time[2]		0.1	3.45	0.1	0.9	μs
t <sub>VD;DAT</sub>	data valid time[3]		0.1	3.45	0.1	0.9	μs
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>f</sub>	fall time of both SDA and SCL signals	[4][5]	-	300	20 + 0.1C <sub>b</sub> [6]	300	ns
t <sub>r</sub>	rise time of both SDA and SCL signals	[4][5]	-	1000	20 + 0.1C <sub>b</sub> [6]	300	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	ns
<b>Port timing</b>							
t <sub>en</sub>	enable time	output	-	80	-	80	ns
t <sub>dis</sub>	disable time	output	-	40	-	40	ns
t <sub>V(Q)</sub>	data output valid time		-	250	-	250	ns
t <sub>su(D)</sub>	data input set-up time		100	-	100	-	ns
t <sub>h(D)</sub>	data input hold time		0.5	-	0.5	-	μs
<b>Interrupt timing</b>							
t <sub>V(INT_N)</sub>	valid time on pin INT_N		-	4	-	4	μs
t <sub>rst(INT_N)</sub>	reset time on pin INT_N		-	4	-	4	μs
<b>Reset</b>							
t <sub>w(rst)</sub>	reset pulse width		4	-	4	-	ns
t <sub>rec(rst)</sub>	reset recovery time		0	-	0	-	ns
t <sub>rst</sub>	reset time		100	-	100	-	ns

[1] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

[2] t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[3] t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

[4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V<sub>IL</sub> of the SCL signal) in order to bridge the undefined region SCL's falling edge.

- [5] The maximum  $t_r$  for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage  $t_f$  is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_r$ .
- [6]  $C_b$  = total capacitance of one bus line in pF.
- [7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

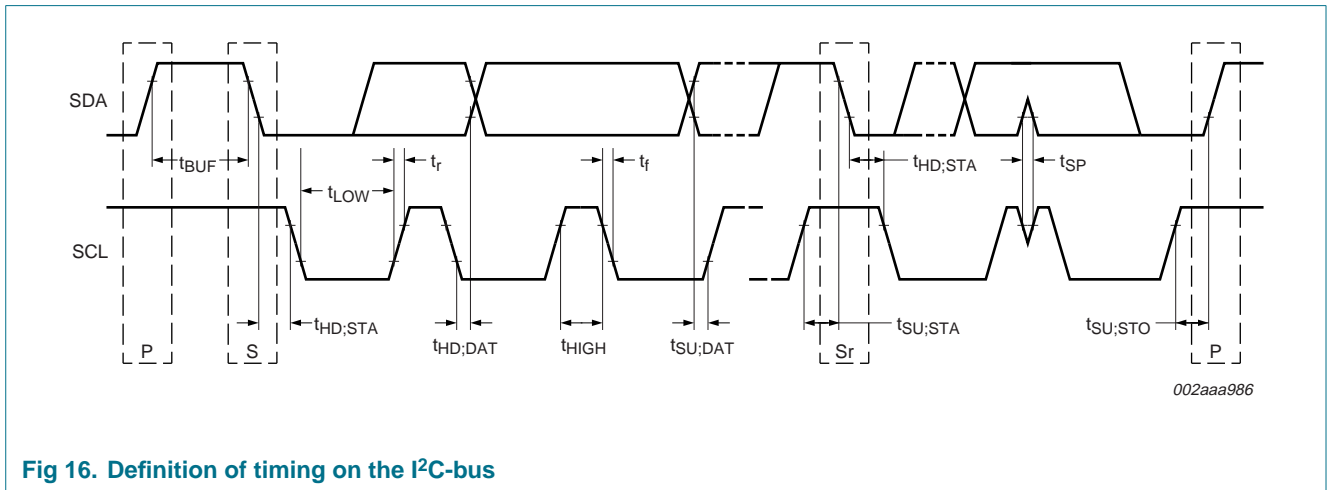


Fig 16. Definition of timing on the I<sup>2</sup>C-bus

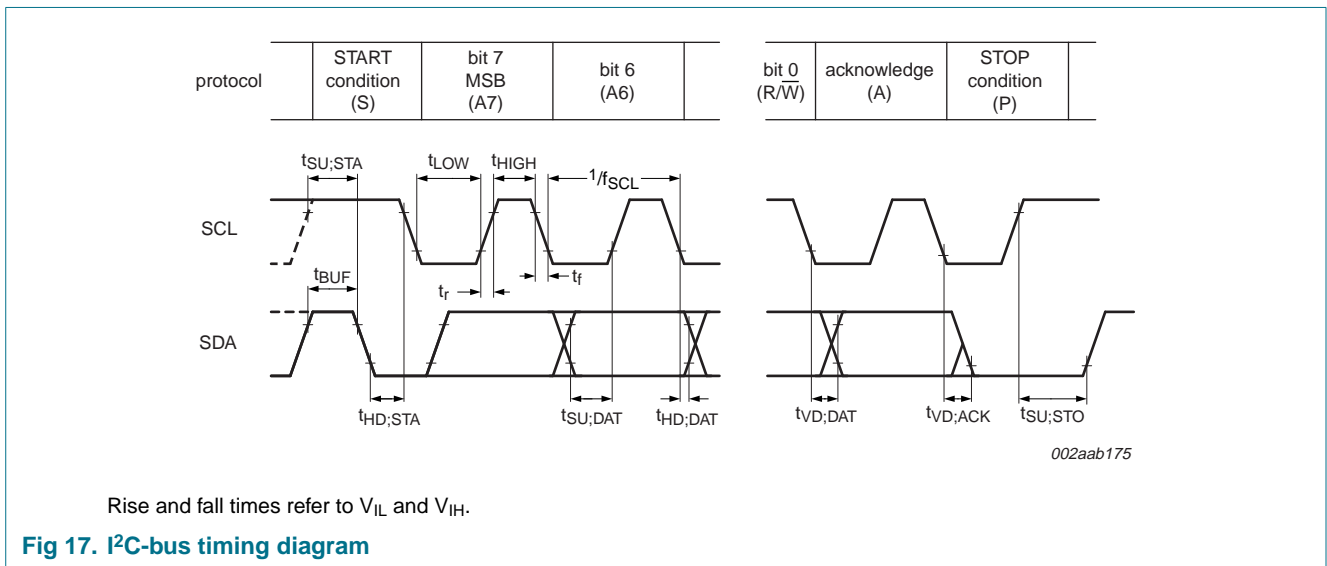


Fig 17. I<sup>2</sup>C-bus timing diagram

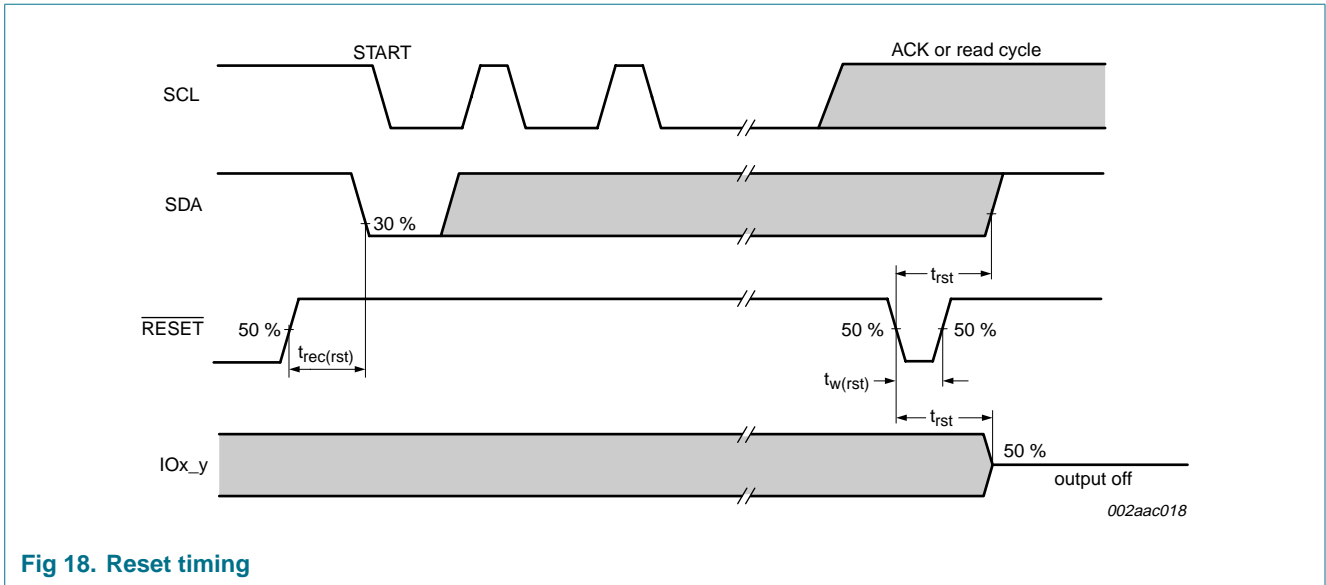


Fig 18. Reset timing

### 13. Test information

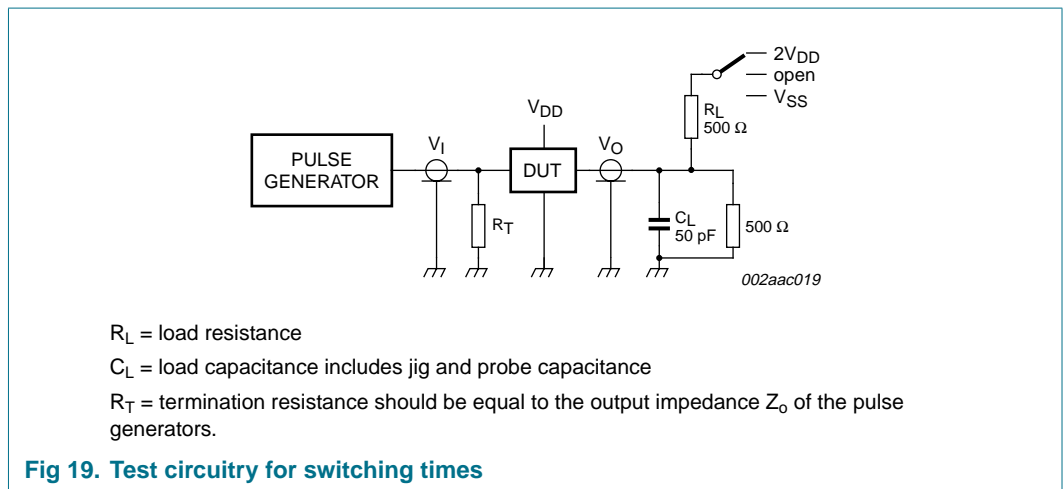


Fig 19. Test circuitry for switching times

14. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

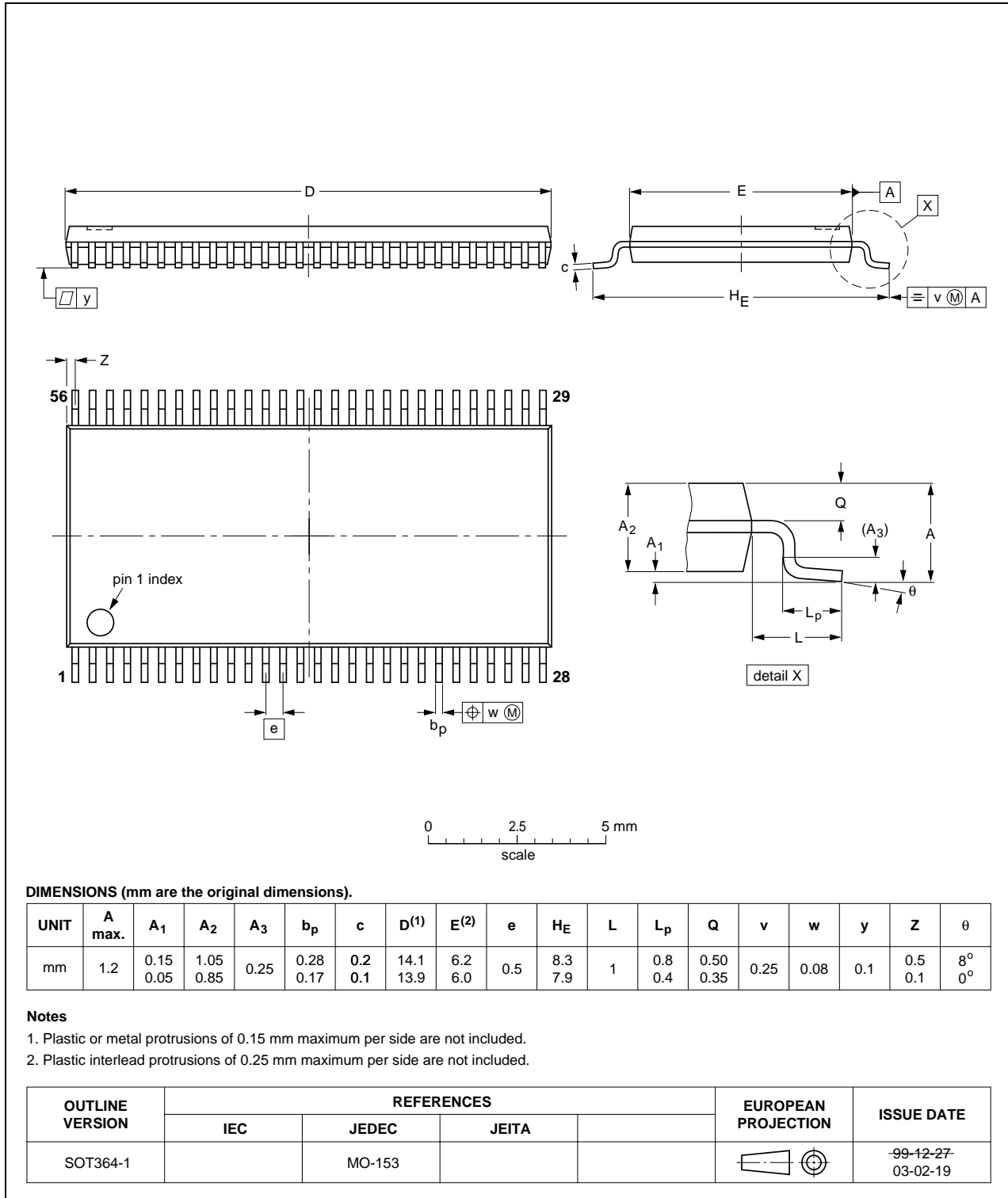


Fig 20. Package outline SOT364-1 (TSSOP56)



HVQFN56: plastic thermal enhanced very thin quad flat package; no leads;  
56 terminals; body 8 x 8 x 0.85 mm

SOT684-1

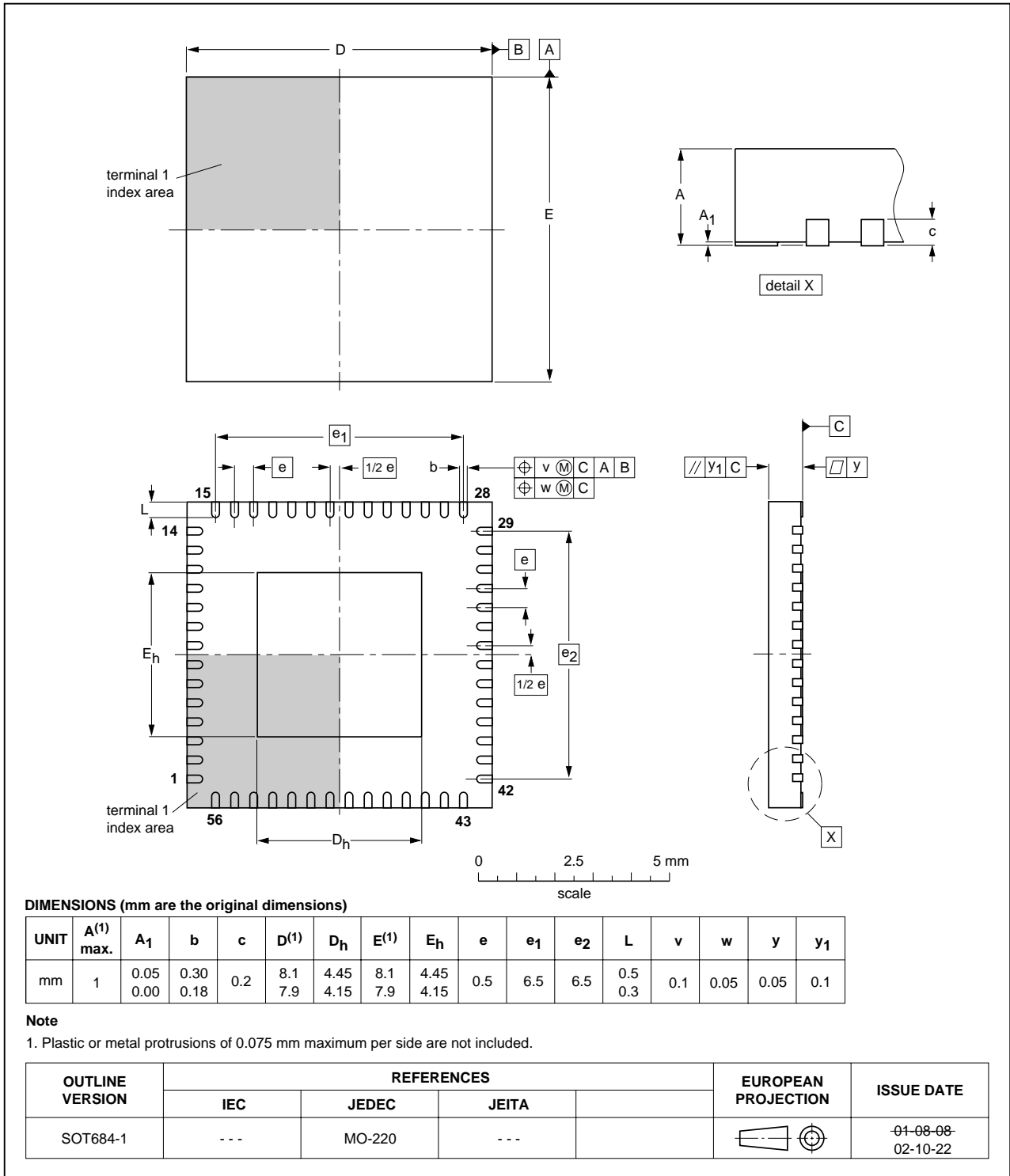


Fig 21. Package outline SOT684-1 (HVQFN56)

## 15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

## 16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 22](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 12](#) and [13](#)

**Table 12. SnPb eutectic process (from J-STD-020C)**

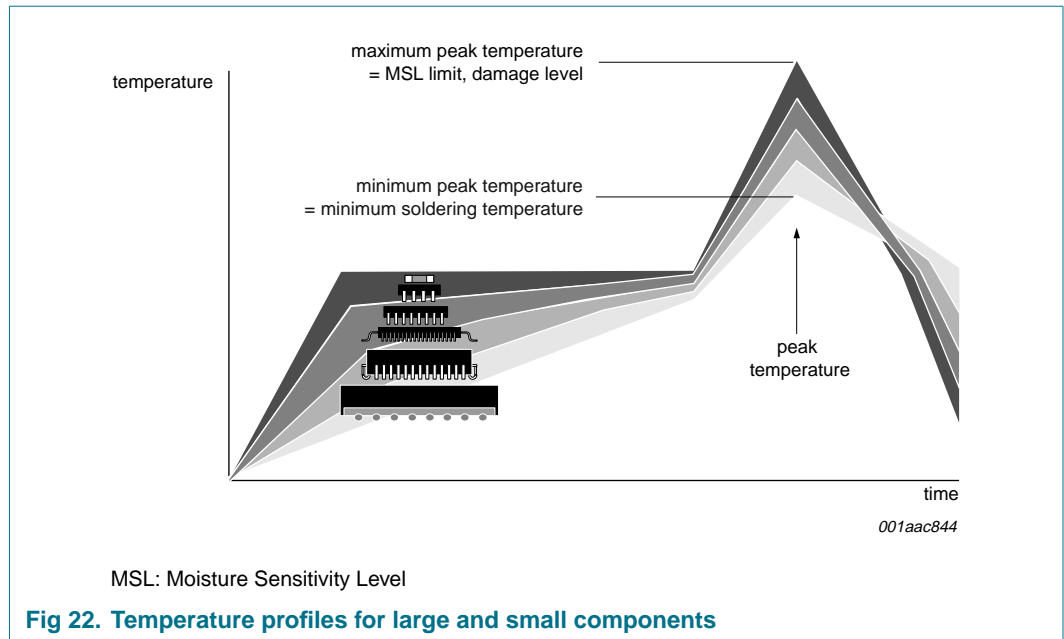
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 13. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 22](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 17. Abbreviations

**Table 14. Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
I <sup>2</sup> C-bus	Inter IC bus
LED	Light Emitting Diode
MM	Machine Model
PLC	Programmable Logic Controller
POR	Power-On Reset
PWM	Pulse Width Modulation
RAID	Redundant Array of Independent Disks

## 18. Revision history

**Table 15. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9505_9506_3	20070606	Product data sheet	-	PCA9506_2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Added device PCA9505</li> <li>• <a href="#">Section 1 “General description”</a>:                             <ul style="list-style-type: none"> <li>– 1st paragraph: added last 2 sentences</li> <li>– 6th paragraph re-written</li> </ul> </li> <li>• <a href="#">Section 2 “Features”</a>:                             <ul style="list-style-type: none"> <li>– added (new) 4th bullet item</li> <li>– moved (old) 1st sub-bullet below “Inputs:” to 4th sub-bullet below “Outputs:”</li> <li>– last bullet item re-written to indicate which package offered for each type number</li> </ul> </li> <li>• <a href="#">Table 1 “Ordering information”</a>: added Type number PCA9505DGG</li> <li>• <a href="#">Figure 2 “Simplified schematic of IO0_0 to IO4_7”</a>: added pull-up resistor for PCA9505</li> <li>• <a href="#">Table 10 “Static characteristics”</a>, sub-section “Supply”:                             <ul style="list-style-type: none"> <li>– symbol <math>I_{DD}</math>: added separate specifications for PCA9505</li> <li>– changed symbol from “<math>I_{stb}</math>, standby current” to “<math>I_{stbH}</math>, HIGH-level standby current”</li> <li>– added symbol “<math>I_{stbL}</math>, LOW-level standby current” (applies to PCA9505 only)</li> </ul> </li> <li>• <a href="#">Table 10 “Static characteristics”</a>, sub-section “I/Os”:                             <ul style="list-style-type: none"> <li>– symbol <math>I_{LIL}</math>: added separate specifications for PCA9505</li> </ul> </li> </ul>			
PCA9506_2	20060509	Product data sheet	-	PCA9506_1
PCA9506_1 (9397 750 14939)	20060214	Product data sheet	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 19.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 19.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to

result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

## 20. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

21. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	19.1	Data sheet status . . . . .	30
<b>2</b>	<b>Features</b> . . . . .	<b>1</b>	19.2	Definitions . . . . .	30
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>	19.3	Disclaimers . . . . .	30
<b>4</b>	<b>Ordering information</b> . . . . .	<b>2</b>	19.4	Trademarks . . . . .	30
<b>5</b>	<b>Block diagram</b> . . . . .	<b>3</b>	<b>20</b>	<b>Contact information</b> . . . . .	<b>30</b>
<b>6</b>	<b>Pinning information</b> . . . . .	<b>5</b>	<b>21</b>	<b>Contents</b> . . . . .	<b>31</b>
6.1	Pinning . . . . .	5			
6.2	Pin description . . . . .	6			
<b>7</b>	<b>Functional description</b> . . . . .	<b>7</b>			
7.1	Device address . . . . .	7			
7.2	Command register . . . . .	7			
7.3	Register definitions . . . . .	9			
7.3.1	IP0 to IP4 - Input Port registers . . . . .	10			
7.3.2	OP0 to OP4 - Output Port registers . . . . .	11			
7.3.3	PI0 to PI4 - Polarity Inversion registers . . . . .	11			
7.3.4	IOC0 to IOC4 - I/O Configuration registers . . . . .	12			
7.3.5	MSK0 to MSK4 - Mask interrupt registers . . . . .	12			
7.4	Power-on reset . . . . .	12			
7.5	$\overline{\text{RESET}}$ input . . . . .	12			
7.6	Interrupt output ( $\overline{\text{INT}}$ ) . . . . .	13			
7.7	Output enable input ( $\overline{\text{OE}}$ ) . . . . .	13			
7.8	Live insertion . . . . .	13			
7.9	Standby . . . . .	13			
<b>8</b>	<b>Characteristics of the I<sup>2</sup>C-bus</b> . . . . .	<b>14</b>			
8.1	Bit transfer . . . . .	14			
8.1.1	START and STOP conditions . . . . .	14			
8.2	System configuration . . . . .	14			
8.3	Acknowledge . . . . .	15			
8.4	Bus transactions . . . . .	15			
<b>9</b>	<b>Application design-in information</b> . . . . .	<b>18</b>			
<b>10</b>	<b>Limiting values</b> . . . . .	<b>19</b>			
<b>11</b>	<b>Static characteristics</b> . . . . .	<b>19</b>			
<b>12</b>	<b>Dynamic characteristics</b> . . . . .	<b>21</b>			
<b>13</b>	<b>Test information</b> . . . . .	<b>23</b>			
<b>14</b>	<b>Package outline</b> . . . . .	<b>24</b>			
<b>15</b>	<b>Handling information</b> . . . . .	<b>26</b>			
<b>16</b>	<b>Soldering</b> . . . . .	<b>26</b>			
16.1	Introduction to soldering . . . . .	26			
16.2	Wave and reflow soldering . . . . .	26			
16.3	Wave soldering . . . . .	26			
16.4	Reflow soldering . . . . .	27			
<b>17</b>	<b>Abbreviations</b> . . . . .	<b>28</b>			
<b>18</b>	<b>Revision history</b> . . . . .	<b>29</b>			
<b>19</b>	<b>Legal information</b> . . . . .	<b>30</b>			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

