DS05-11460-1E

MEMORY Mobile FCRAM™

CMOS

32 M Bit (2 M word × 16 bit)

Mobile Phone Application Specific Memory

MB82DP02183F-65L

■ DESCRIPTION

The MB82DP02183F is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 33, 554, 432 storages accessible in a 16-bit format.

This MB82DP02183F is suited for mobile applications such as Cellular Handset and PDA.

*: FCRAM is a trademark of Fujitsu Microelectronics Limited, Japan

■ FEATURES

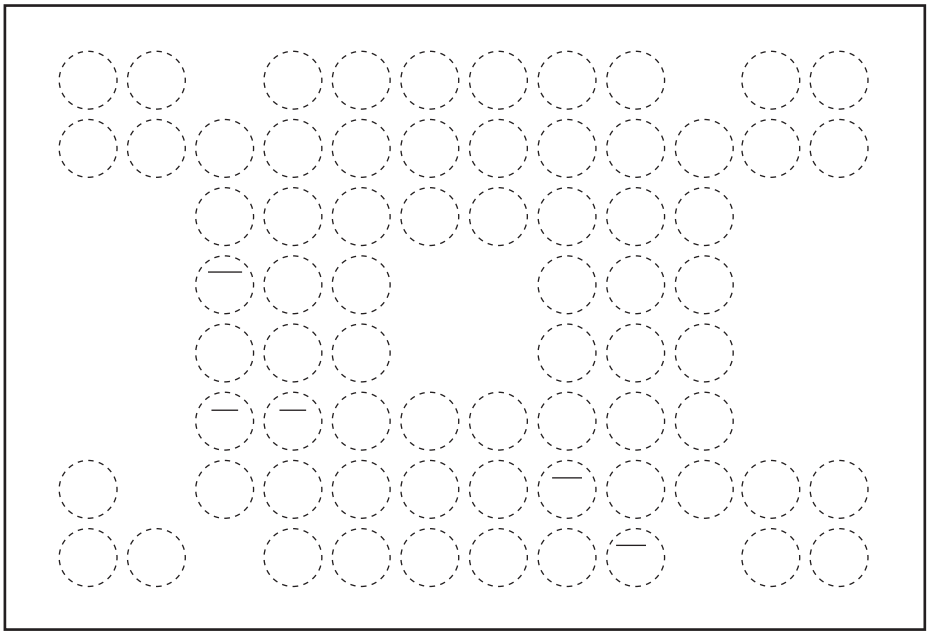
- Asynchronous SRAM Interface
- Fast Access Time : $t_{AA} = t_{CE} = 65$ ns Max
- 8 words Page Access Capability : $t_{PAA} = 20$ ns Max
- Low Voltage Operating Condition : $V_{DD} = 2.6$ V to 3.1 V
- Operating Temperature: $T_A = 0$ °C to + 70 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low Power Consumption : $I_{DDA1} = 30$ mA Max
  $I_{DDS1} = 120$ µA Max
- Various Power Down mode : Sleep
  4 M-bit Partial
  8 M-bit Partial

■ MAIN SPECIFICATIONS

Parameter	MB82DP02183F-65L
Access Time (Max) (t_{CE}, t_{AA})	65 ns
Active Current (Max) (I_{DDA1})	30 mA
Standby Current (Max) (I_{DDS1})	120 µA
Power Down Current (Max) (I_{DDPS})	10 µA

2009.8

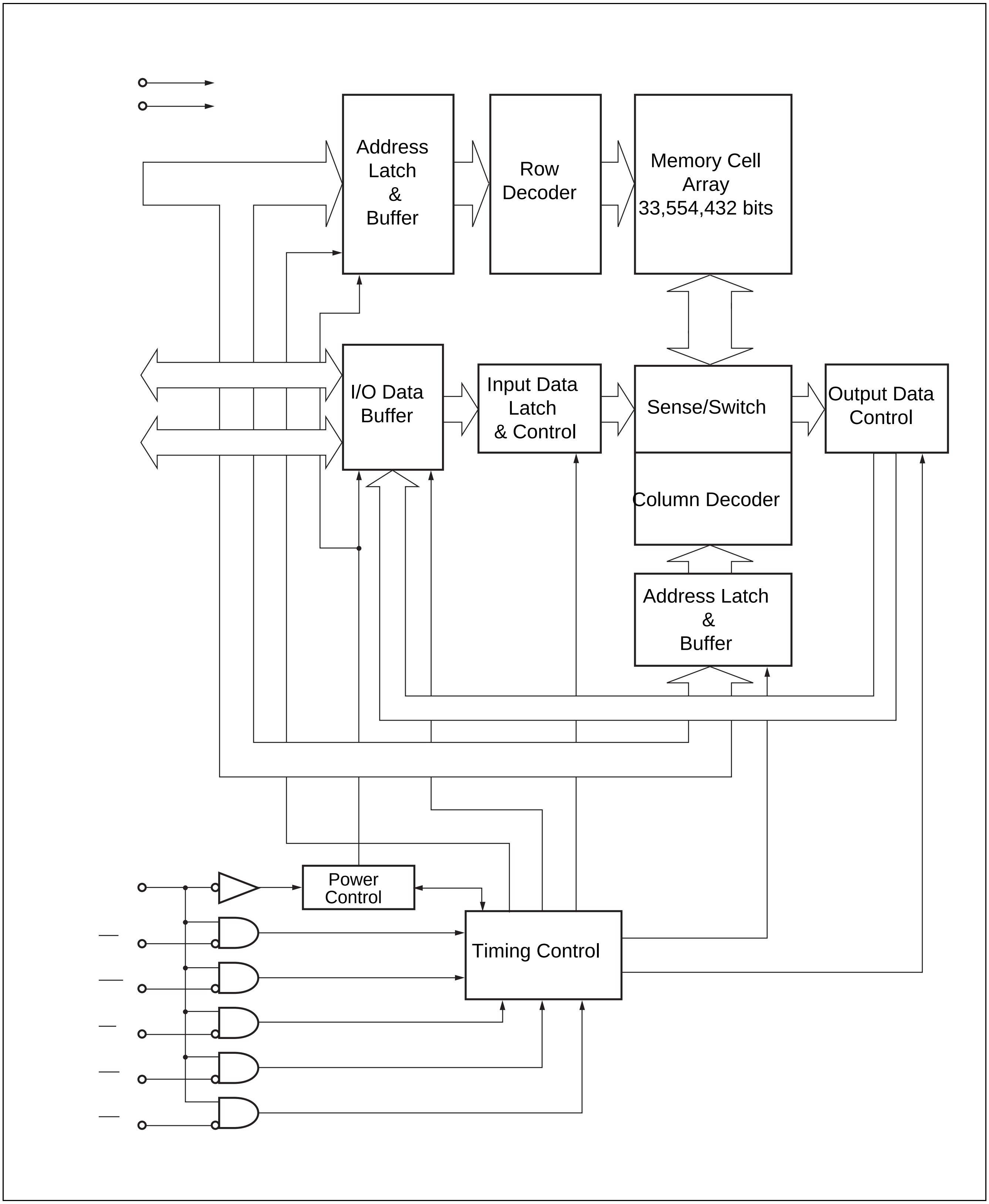
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin Name	Description
A_{20} to A_0	Address Input
$\overline{CE}1$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ_7 to DQ_0	Lower Byte Data Input/Output
DQ_{15} to DQ_8	Upper Byte Data Input/Output
V_{DD}	Power Supply Voltage
V_{SS}	Ground
NC	No Connection
DU	Don't Use

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

<table>
<tr><th>Mode</th><th>CE2</th><th>$\overline{CE1}$</th><th>$\overline{WE}$</th><th>$\overline{OE}$</th><th>$\overline{LB}$</th><th>$\overline{UB}$</th><th>A_{20} to A_0</th><th>DQ_7 to DQ_0</th><th>DQ_{15} to DQ_8</th></tr>
<tr><td>Standby (Deselect)</td><td>H</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>High-Z</td><td>High-Z</td></tr>
<tr><td>Output Disable*1</td><td rowspan="9">H</td><td rowspan="9">L</td><td>H</td><td>H</td><td>X</td><td>X</td><td>*3</td><td>High-Z</td><td>High-Z</td></tr>
<tr><td>Output Disable (No Read)</td><td rowspan="4">H</td><td rowspan="4">L</td><td>H</td><td>H</td><td>Valid</td><td>High-Z</td><td>High-Z</td></tr>
<tr><td>Read (Upper Byte)</td><td>H</td><td>L</td><td>Valid</td><td>High-Z</td><td>Output Valid</td></tr>
<tr><td>Read (Lower Byte)</td><td>L</td><td>H</td><td>Valid</td><td>Output Valid</td><td>High-Z</td></tr>
<tr><td>Read (Word)</td><td>L</td><td>L</td><td>Valid</td><td>Output Valid</td><td>Output Valid</td></tr>
<tr><td>No Write</td><td rowspan="4">L</td><td rowspan="4">H*4</td><td>H</td><td>H</td><td>Valid</td><td>Invalid</td><td>Invalid</td></tr>
<tr><td>Write (Upper Byte)</td><td>H</td><td>L</td><td>Valid</td><td>Invalid</td><td>Input Valid</td></tr>
<tr><td>Write (Lower Byte)</td><td>L</td><td>H</td><td>Valid</td><td>Input Valid</td><td>Invalid</td></tr>
<tr><td>Write (Word)</td><td>L</td><td>L</td><td>Valid</td><td>Input Valid</td><td>Input Valid</td></tr>
<tr><td>Power Down*2</td><td>L</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>High-Z</td><td>High-Z</td></tr>
</table>

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 1 s.

*2 : Power Down mode can be entered from standby state and all DQ pins are in High-Z state.
Data retention depends on the selection of Power Down program. Refer to "■ POWER DOWN" for the detail.

*3 : Can be either V_{IL} or V_{IH} but must be valid before read or write.

*4 : $\overline{OE}$ can be V_{IL} during write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{CE}$1. Refer to "(12) Read/Write Timing 1-1 ($\overline{CE}$1 Control)" in "■ TIMING DIAGRAMS".
(2) $\overline{OE}$ stays V_{IL} during write cycle.

■ POWER DOWN

Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in Power Down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from Power Down mode.
This device has three Power Down modes, Sleep, 4 M-bit Partial and 8 M-bit Partial. The selection of Power Down mode can be programmed by series of read/write operation. Each mode has following data retention features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
4 M-bit Partial	4 M bits	000000h to 03FFFFh
8 M-bit Partial	8 M bits	000000h to 07FFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

Power Down Program Sequence

The program requires total six read/write operations with unique address and data. The device should be in standby mode in the interval between each read/write operation. The following table shows the detail sequence.

Cycle #	Operation	Address	Data
#1	Read	1FFFFFh (MSB)	Read Data (RDa)
#2	Write	1FFFFFh	RDa
#3	Write	1FFFFFh	RDa
#4	Write	1FFFFFh	Don't Care (X)
#5	Write	1FFFFFh	X
#6	Read	Address Key	Read Data (RDb)

The Cycle#1 is to read from most significant address (MSB).
The Cycle#2 and Cycle#3 are to write to MSB. If the Cycle#2 or Cycle#3 is written into the different address, the program is cancelled and the data written by the Cycle#2 or Cycle#3 is valid as a normal write operation. It is recommended to write back the data (RDa) read by Cycle#1 to MSB in order to secure the data.
The Cycle#4 and Cycle#5 are to write to MSB. The data of Cycle#4 and Cycle#5 becomes the same arbitrary data (Don't-Care). If the Cycle#4 or Cycle#5 is written into different address, the program is also cancelled but write data may not be written as normal write operation.
The Cycle#6 is to read from specific address key for mode selection. And read data (RDb) is invalid.

Once this program sequence is performed from a Partial mode to the other Partial mode, the written data stored in memory cell array may be lost. Therefore, this program should be performed prior to regular read/write operation if Partial Power Down mode is used.

Address Key

The address key has following format.

Mode	Address			
	A_{20}	A_{19}	A_{18} to A_0	Hexadecimal
Sleep (default)	1	1	1	1FFFFFh
4 M-bit Partial	1	0	1	17FFFFh
8 M-bit Partial	0	1	1	0FFFFFh

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	0.5	+ 3.6	V
Input Voltage*	V_{IN}	0.5	+ 3.6	V
Output Voltage*	V_{OUT}	0.5	+ 3.6	V
Short Circuit Output Current	I_{OUT}	50	+ 50	mA
Storage Temperature	T_{STG}	55	+ 125	°C

* : All voltages are referenced to V_{SS}.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage*1	V_{DD}	2.6	3.1	V
	V_{SS}	0	0	V
Input High Voltage *1, *2	V_{IH}	V_{DD} 0.8	V_{DD} + 0.2	V
Input Low Voltage *1, *3	V_{IL}	0.3	V_{DD} 0.2	V
Ambient Temperature	T_A	0	+ 70	°C

*1 : All voltages are referenced to V_{SS}.

*2 : Maximum DC voltage on input or I/O pins is V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.

*3 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ PACKAGE PIN CAPACITANCE

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V			5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V			5	pF
Data Input/Output Capacitance	C_{IO}	V_{IO} = 0 V			8	pF

(3) Power Down Parameters

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10		ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	65		ns	
$\overline{\text{CE}}$1 High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t_{CHH}	300		s	*1
$\overline{\text{CE}}$1 High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t_{CHHP}	65		ns	*2
$\overline{\text{CE}}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0		ns	*1

*1 : Applicable also to power-up.

*2 : Applicable when Partial mode is set.

(4) Other Timing Parameters

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{\text{CE}}$1 High to $\overline{\text{OE}}$ Invalid Time for Standby Entry	t_{CHOX}	10		ns	
$\overline{\text{CE}}$1 High to $\overline{\text{WE}}$ Invalid Time for Standby Entry	t_{CHWX}	10		ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50		s	
$\overline{\text{CE}}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300		s	
Input Transition Time	t_T	1	25	ns	*2

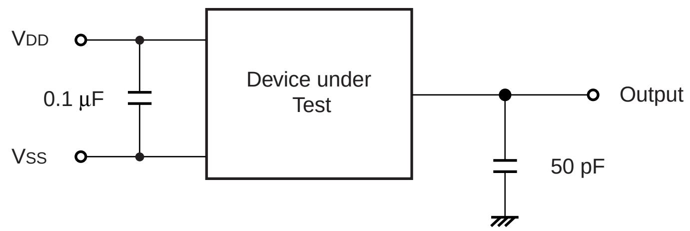
*1 : Some data might be written into any address location if t_{CHWX}(Min) is not satisfied.

*2 : The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.

(5) AC Test Conditions

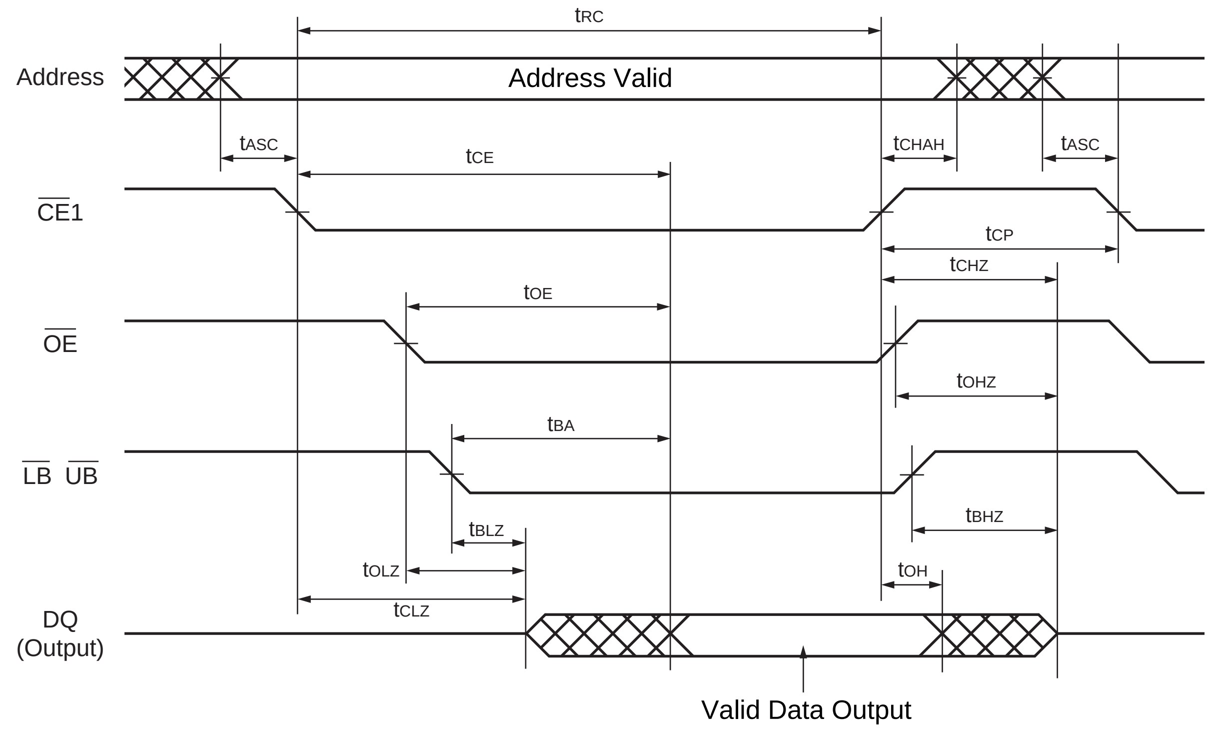
Parameter	Symbol	Test Setup	Value	Unit
Input High Voltage	V_{IH}		V_{DD} 0.8	V
Input Low Voltage	V_{IL}		V_{DD} 0.2	V
Input Timing Measurement Level	V_{REF}		V_{DD} 0.5	V
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns

- AC Measurement Output Load Circuit



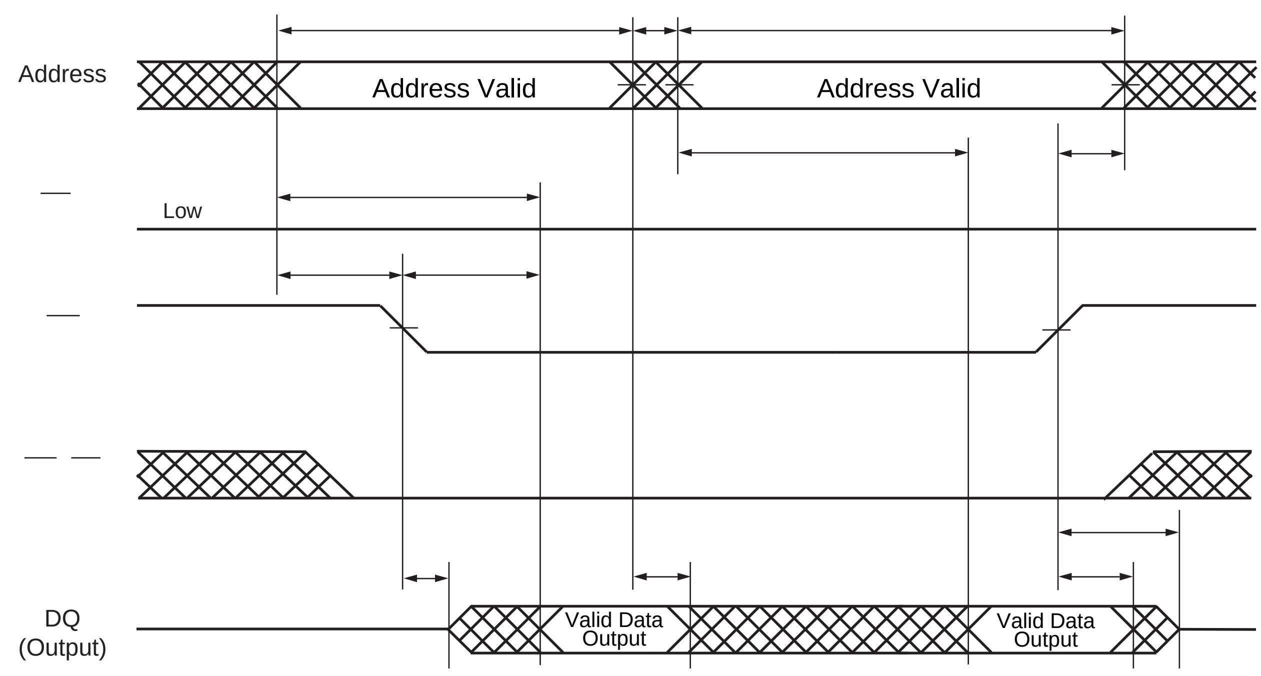
■ TIMING DIAGRAMS

(1) Read Timing 1 (Basic Timing)



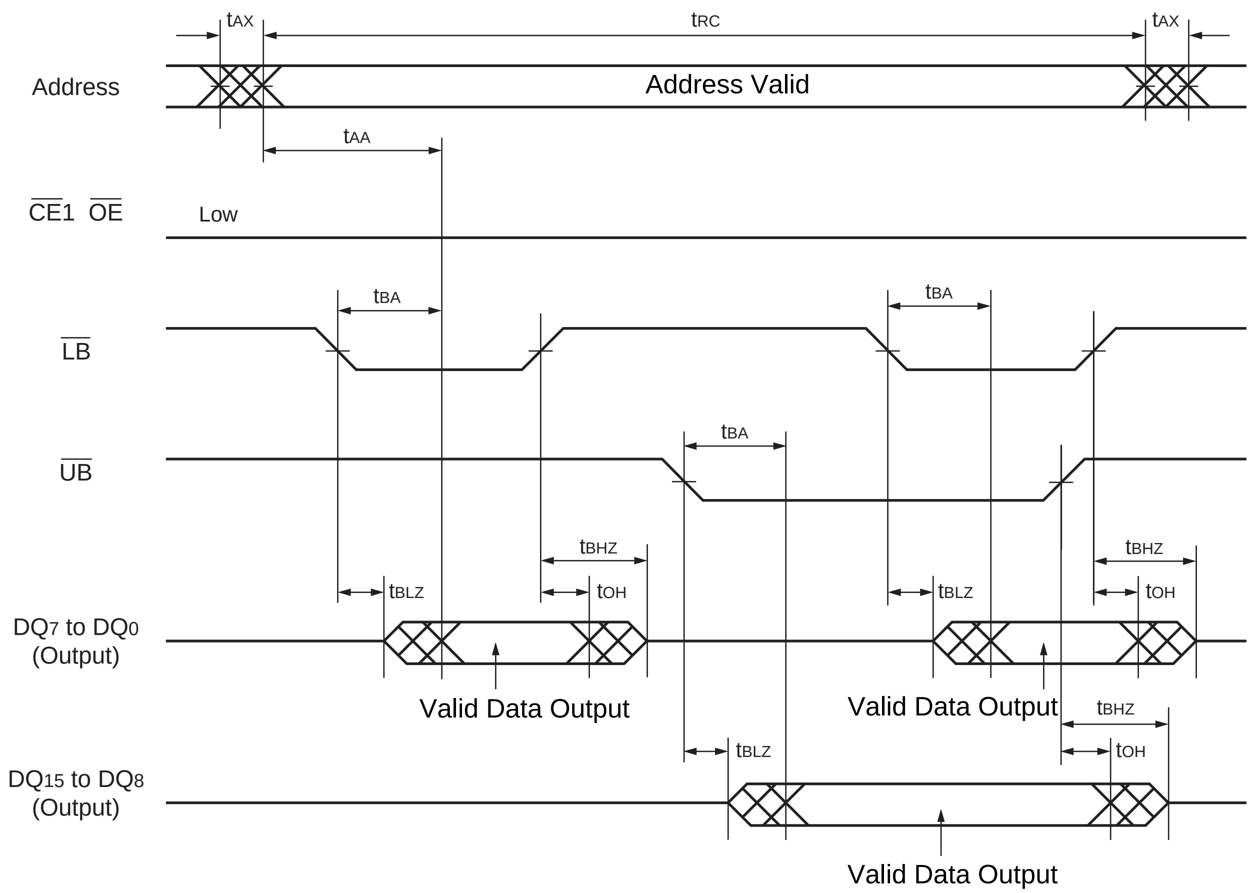
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(2) Read Timing 2 ($\overline{OE}$ Control & Address Access)



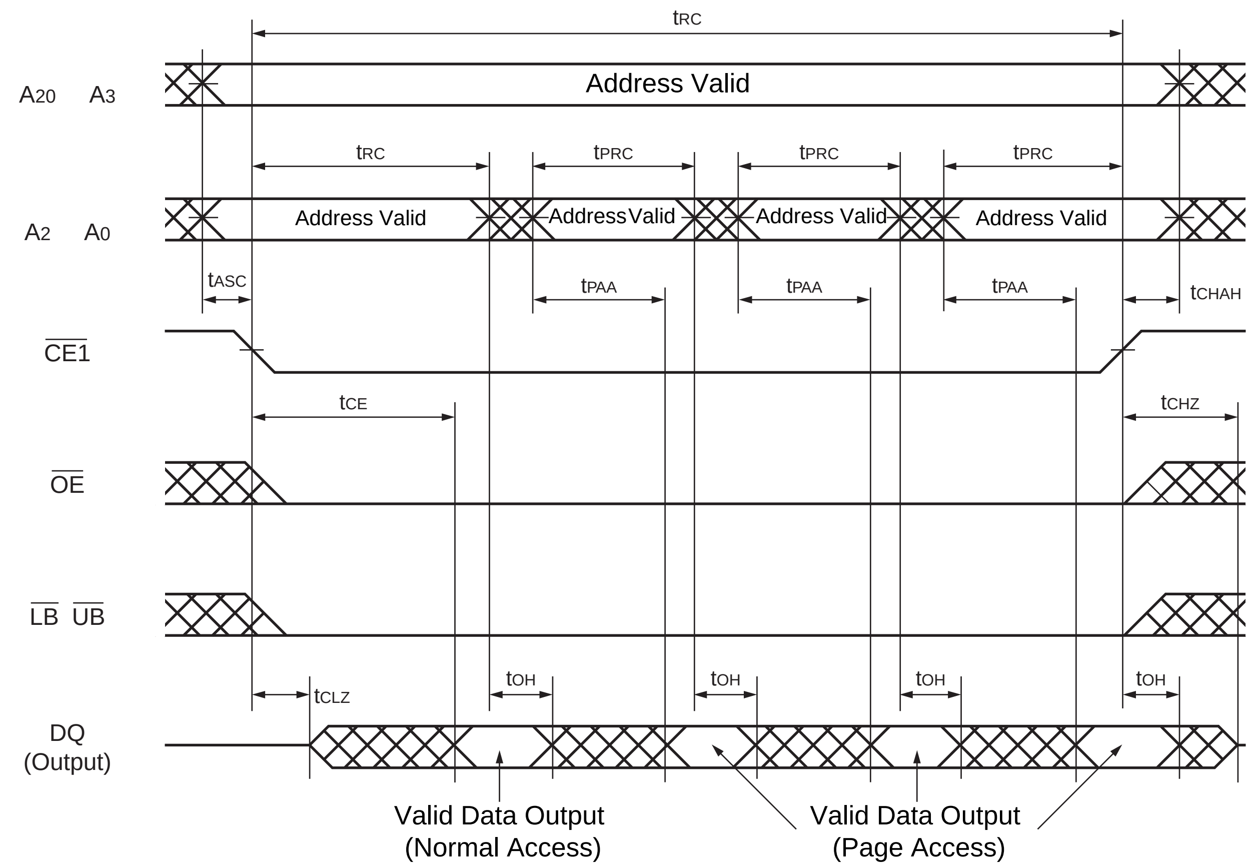
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(3) Read Timing 3 ($\overline{LB}$, $\overline{UB}$ Byte Control Access)



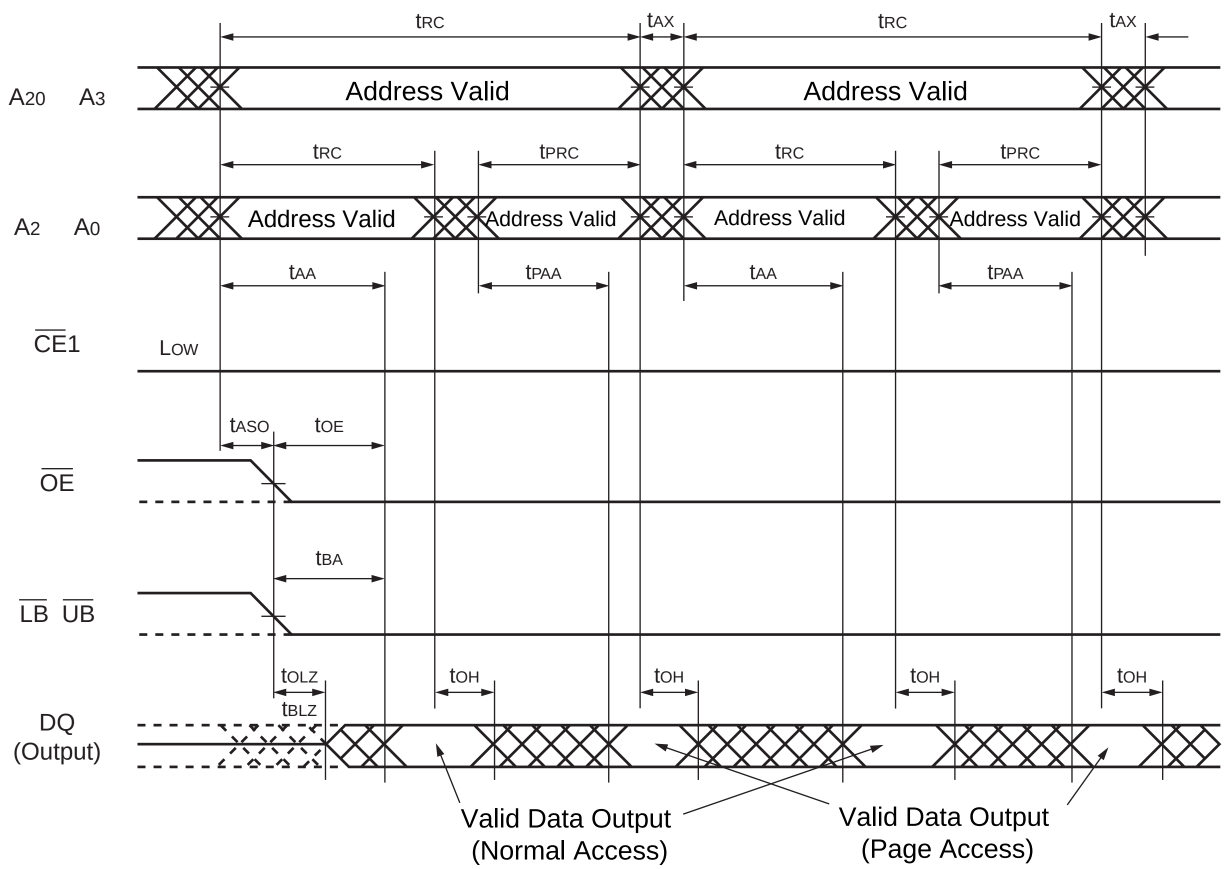
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(4) Read Timing 4 (Page Address Access after $\overline{\text{CE}}$1 Control Access)



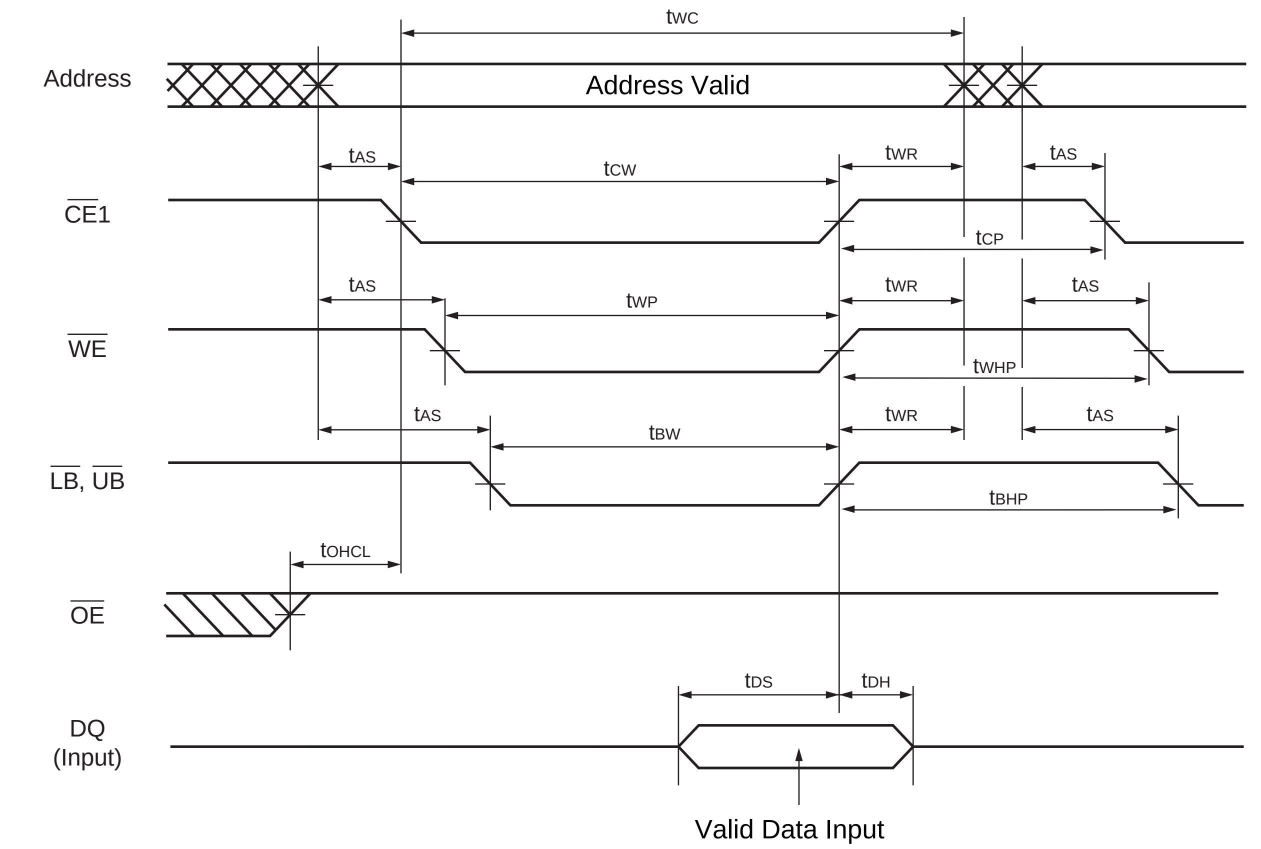
Note : This timing diagram assumes CE2 = H and $\overline{\text{WE}}$ = H.

(5) Read Timing 5 (Random and Page Address Access)



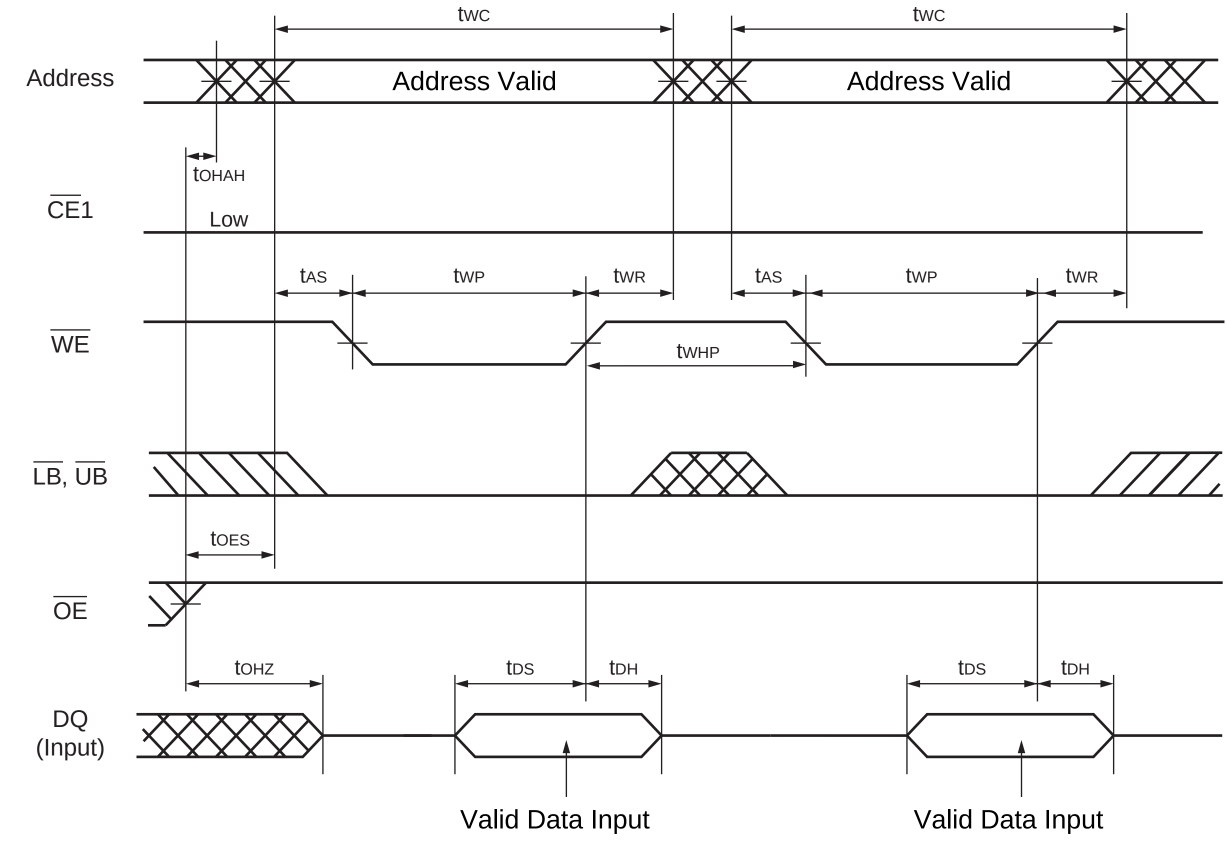
Notes : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.
Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE1}$ and $\overline{OE}$ are Low.

(6) Write Timing 1 (Basic Timing)



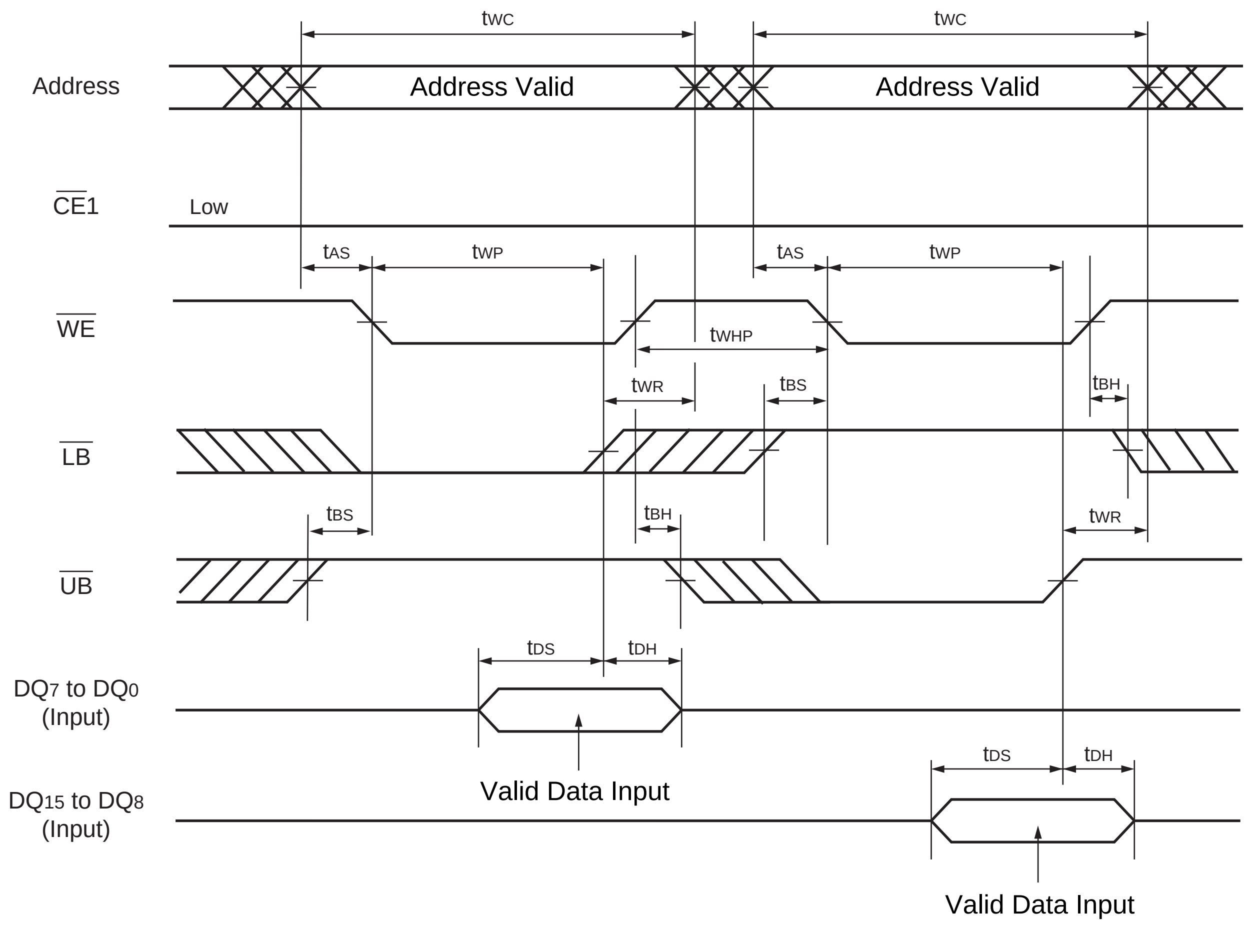
Note : This timing diagram assumes CE2 = H.

(7) Write Timing 2 ($\overline{\text{WE}}$ Control)



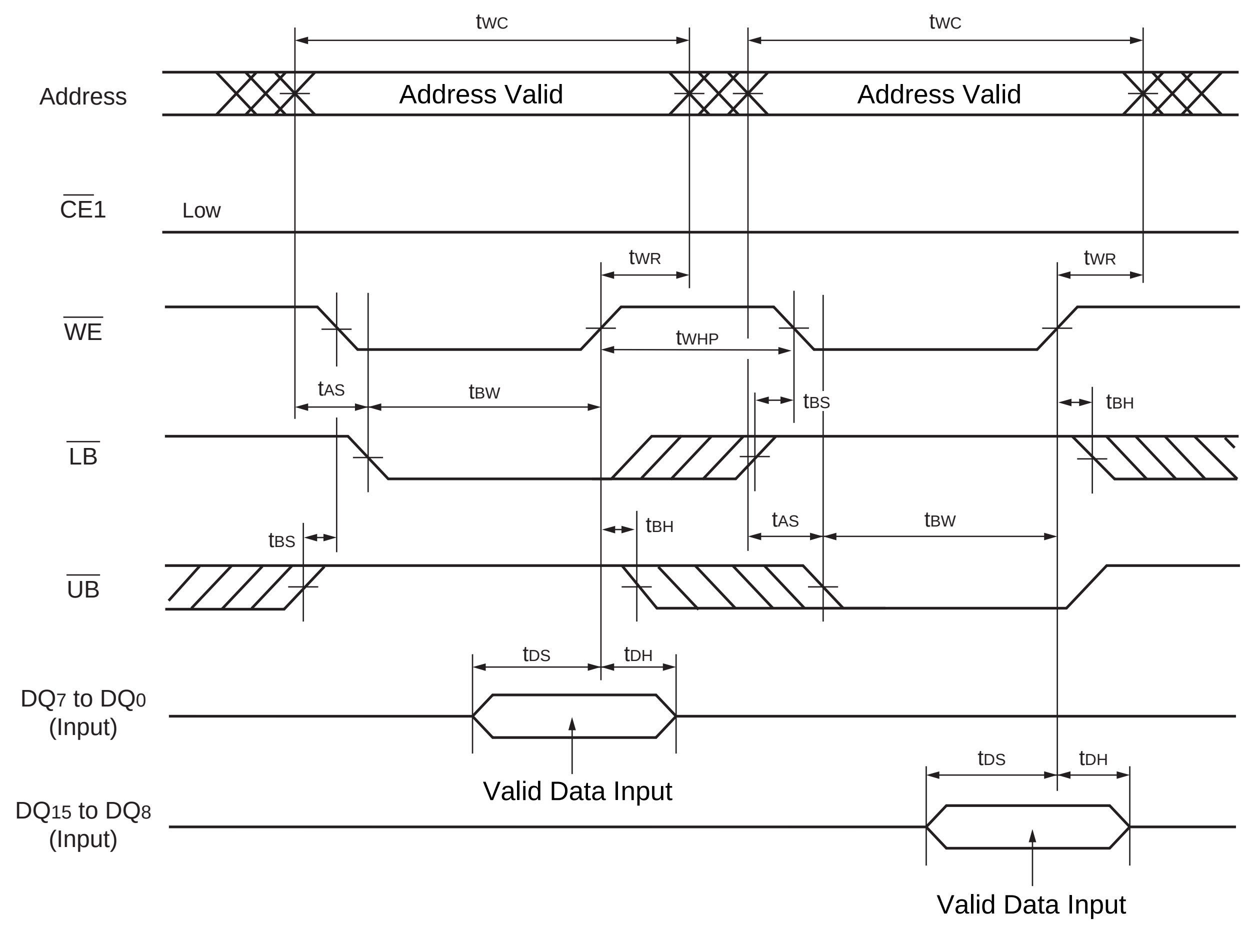
Note : This timing diagram assumes CE2 = H.

(8) Write Timing 3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



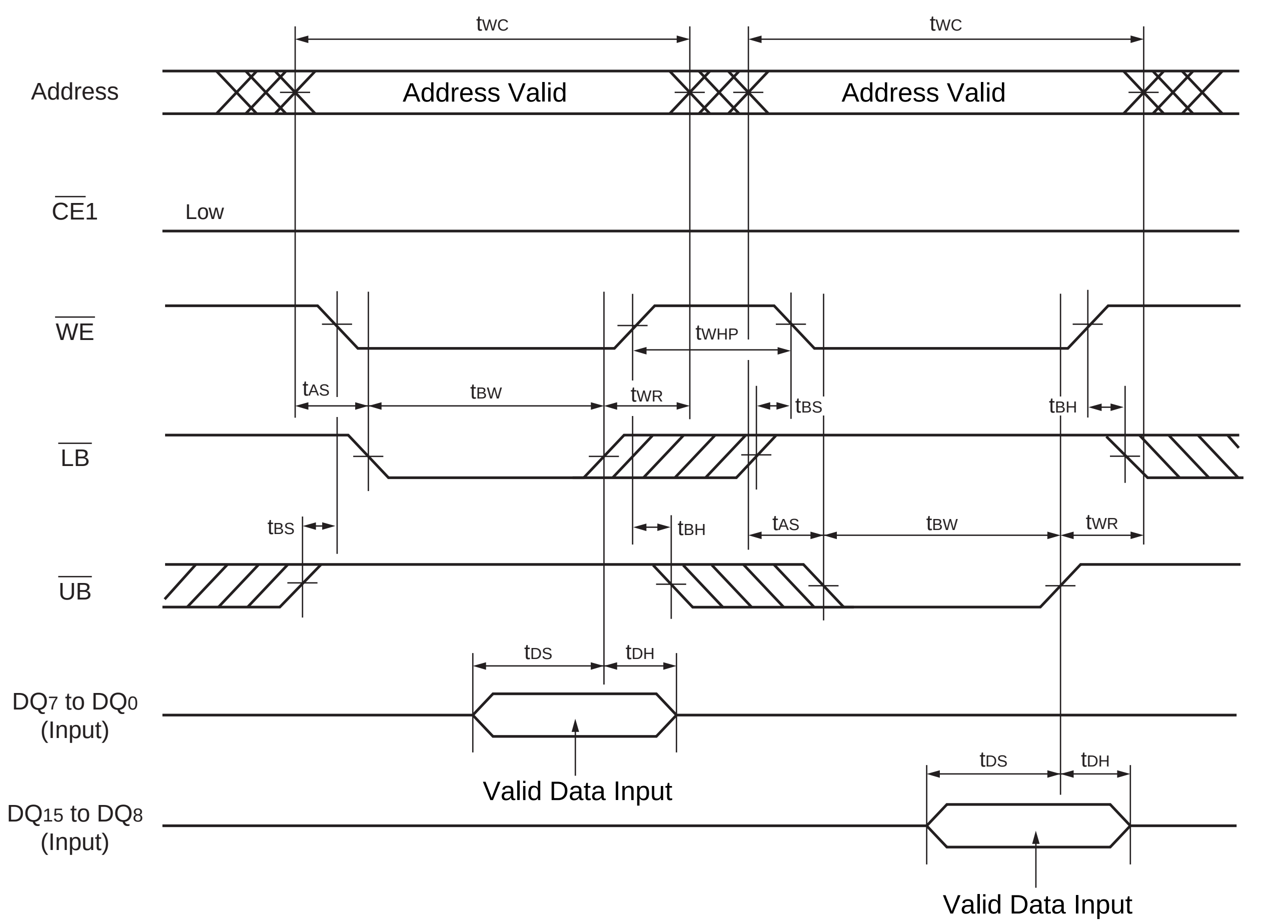
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(9) Write Timing 3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



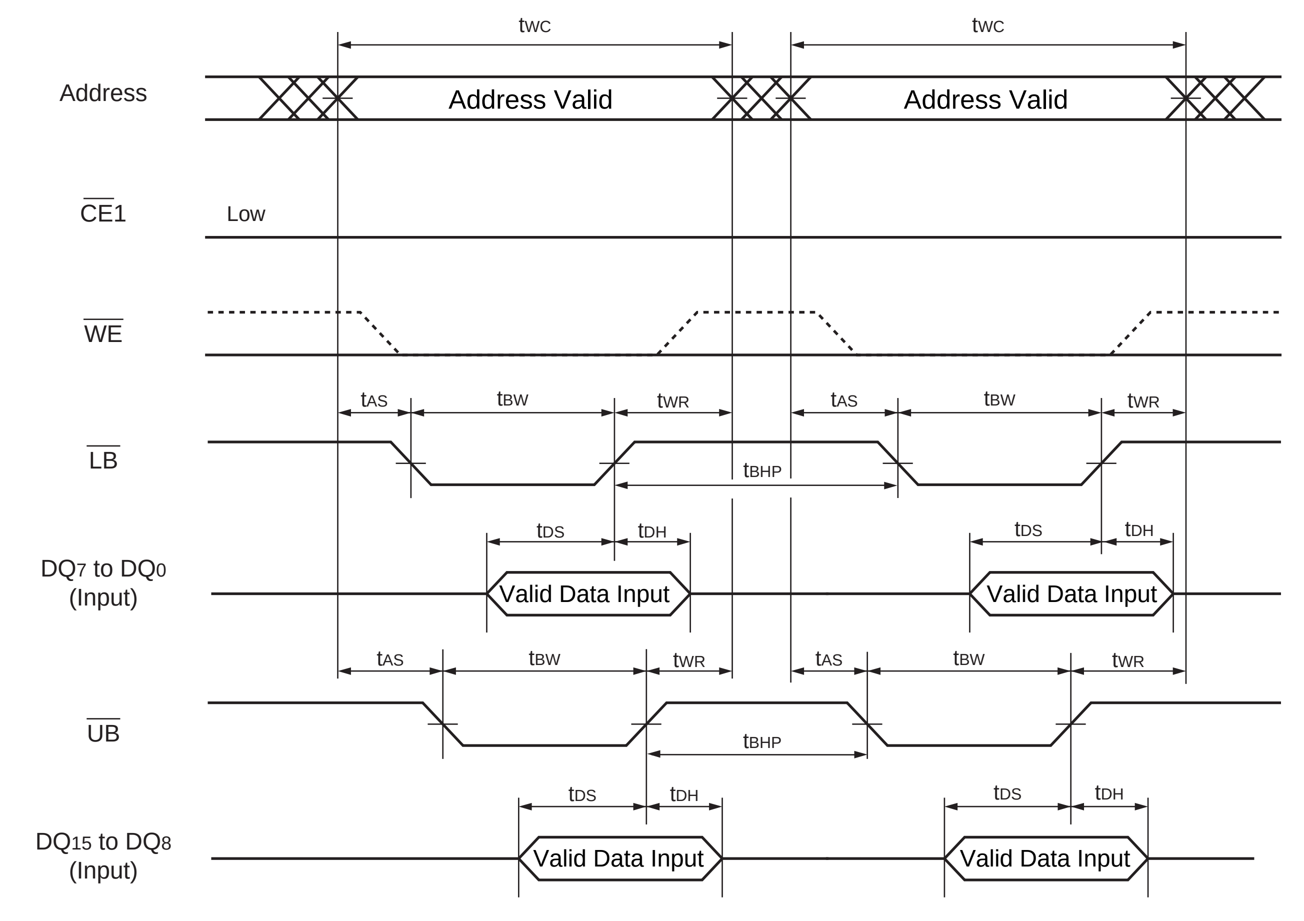
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(10) Write Timing 3-3 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)



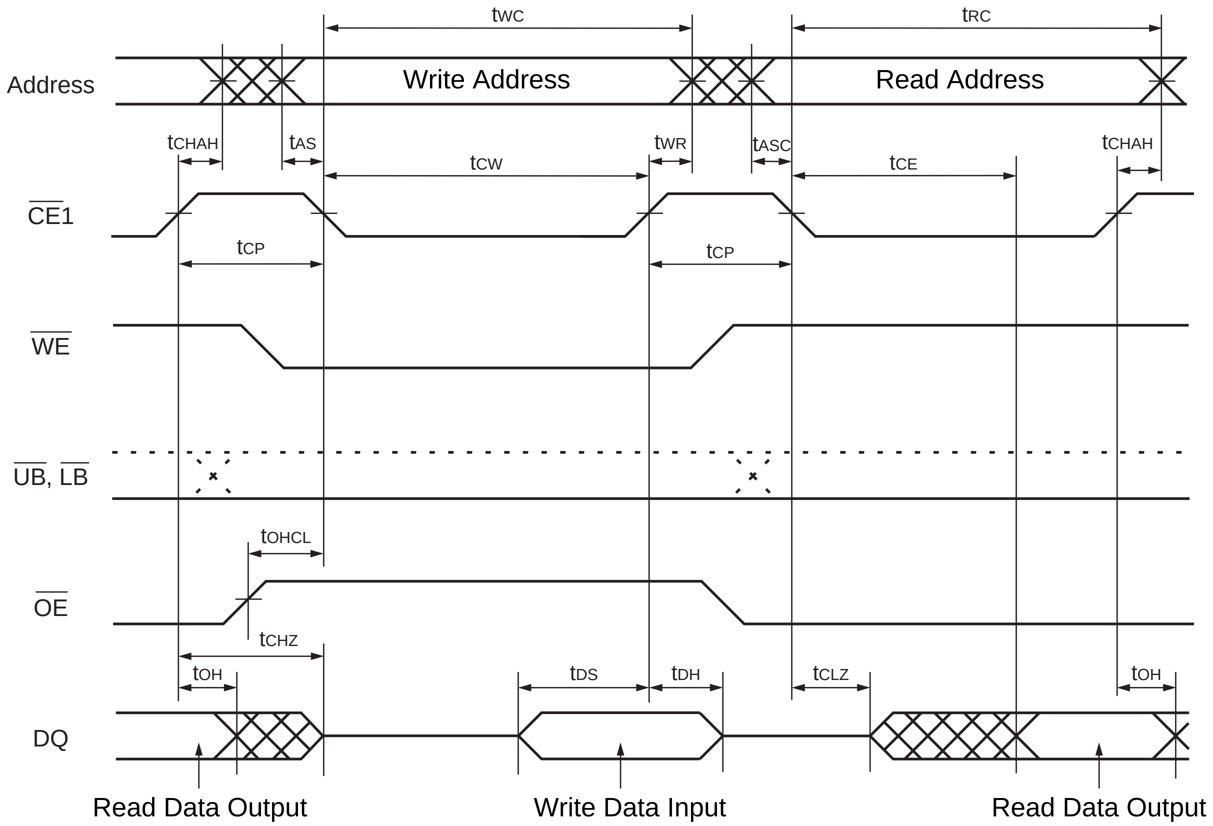
Note : This timing diagram assumes CE2 = H and $\overline{\text{OE}}$ = H.

(11) Write Timing 3-4 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



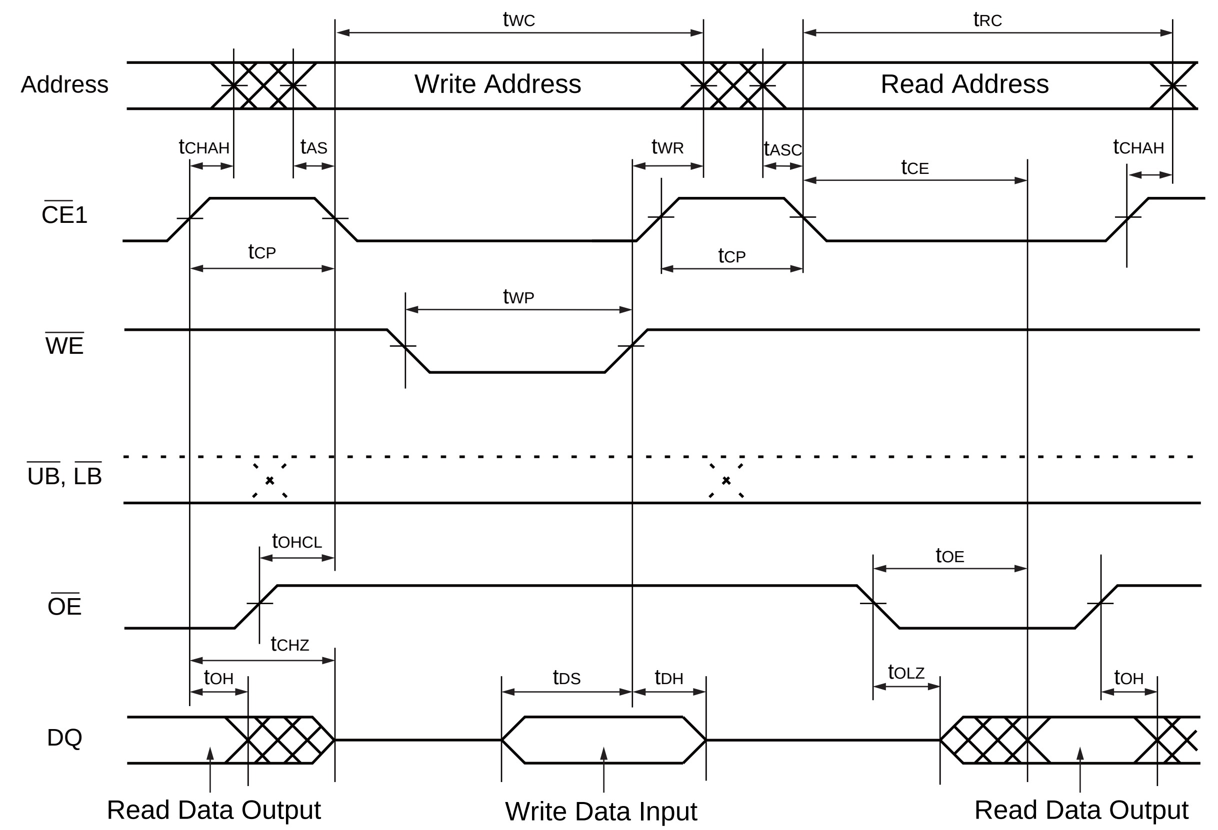
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(12) Read / Write Timing 1-1 ($\overline{CE1}$ Control)



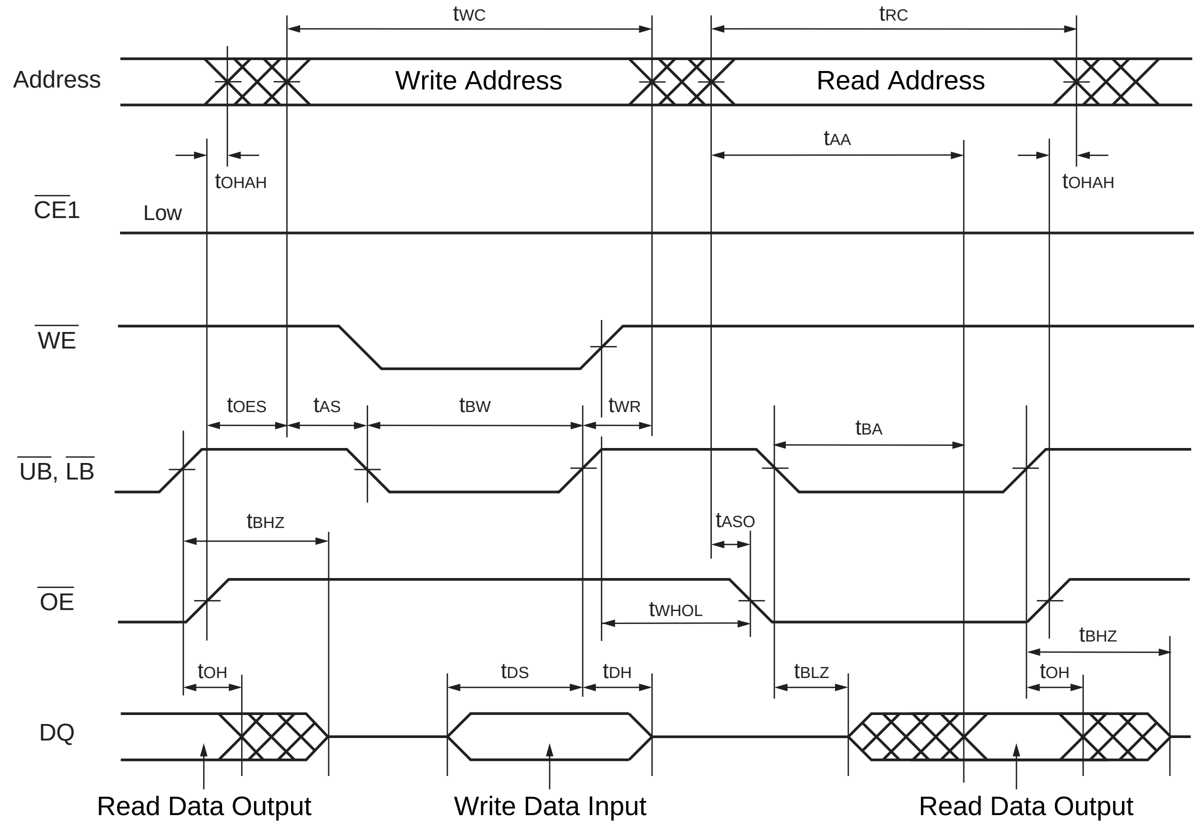
Notes : This timing diagram assumes CE2 = H.
Write address is valid from either $\overline{CE1}$ or $\overline{WE}$ of last falling edge.

(13) Read / Write Timing 1-2 ($\overline{\text{CE}}$1, $\overline{\text{WE}}$, $\overline{\text{OE}}$ Control)



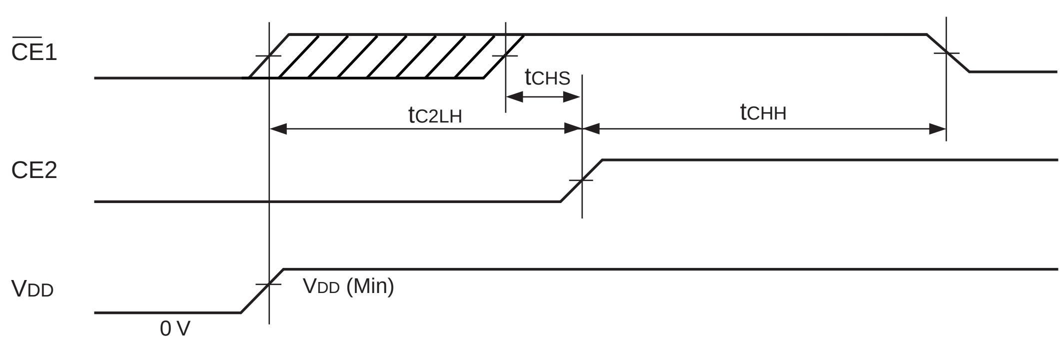
Notes : This timing diagram assumes CE2 = H.
$\overline{\text{OE}}$ can be fixed Low during write operation if it is $\overline{\text{CE}}$1 controlled write at Read-Write-Read sequence.

(15) Read / Write Timing 3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)



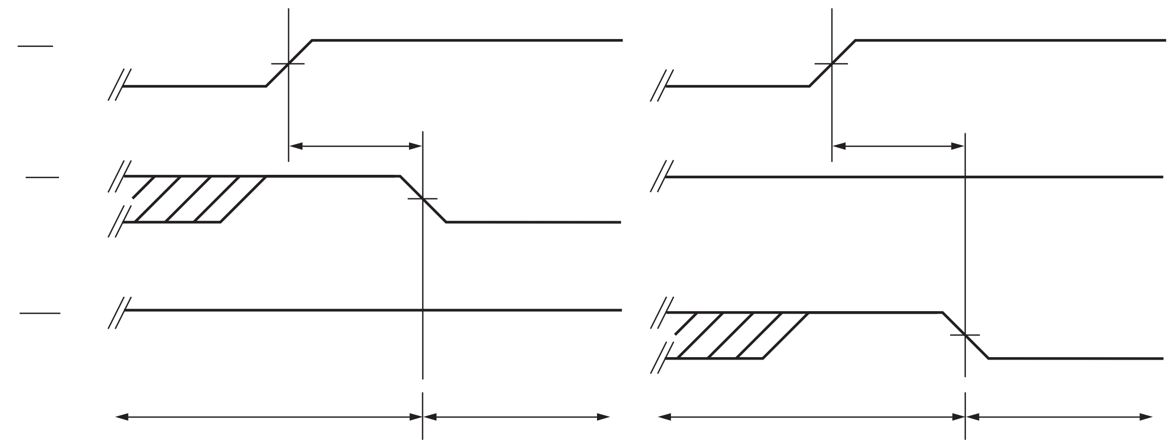
Notes : This timing diagram assumes CE2 = H.
$\overline{CE1}$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
Read data will be available after t_{AA} from $\overline{WE}$ = H if read address are not changed from write address.

(16) Power-up Timing 1



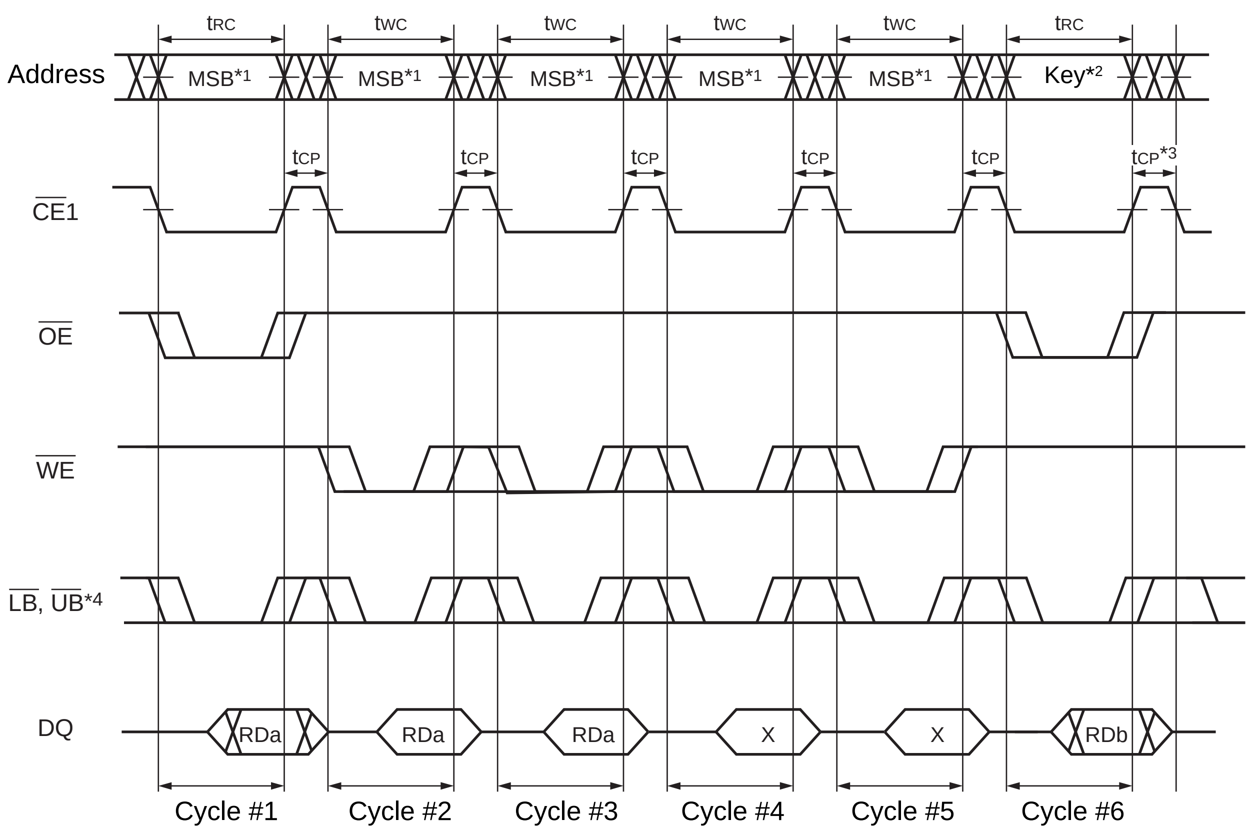
Note : The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

(19) Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for standby mode.

(20) Power Down Program Timing



*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must conform to the format specified in "■ POWER DOWN". If not, the operation and data are not guaranteed.

*3 : After t_{CP} following Cycle #6, the Power Down program is completed and returned to the normal operation.

*4 : Byte read or write is available in addition to word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) needs to be Low.

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