19-5112; Rev 0; 1/10

µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package

General Description

The MAX16072/MAX16073/MAX16074 ultra-small, ultra-low-power, microprocessor (µP) supervisory circuits feature a precision band-gap reference, comparator, and internally trimmed resistors that set the threshold voltage. Designed to monitor the system supply voltage and assert an output during power-up, power-down, and brownout conditions, these devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltage from 1.8V to 3.6V.

The MAX16072 has a push-pull, active-low reset output, the MAX16073 has a push-pull, active-high reset output, and the MAX16074 has an open-drain active-low reset output. The devices are designed to ignore fast transients on V_{CC}. The devices also include a manual reset input ($\overline{MR}$).

The MAX16072/MAX16073/MAX16074 are available in a 1mm x 1mm, space-saving, 4-bump, chip-scale package (UCSP™).

Applications

Portable/Battery-Powered Equipment

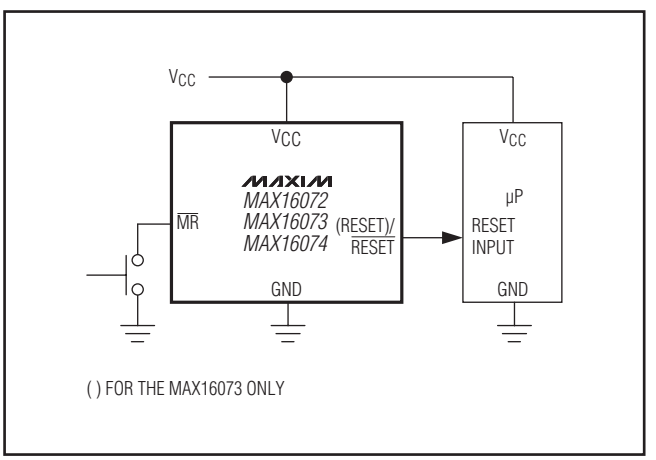
Cell Phones

PDAs

MP3 Players

Digital Cameras

Typical Operating Circuit



Features

- **Ultra-Low, 0.7µA Supply Current**
- **Ultra-Small (1mm x 1mm), 4-Bump UCSP**
- **20µs, 8ms, 34ms, and 140ms Reset Timeout Options Available**
- **Factory-Trimmed Reset Thresholds Available from 1.58V to 3.08V in Approximately 100mV Increments**
- **±2.5% Threshold Accuracy Over Temperature**
- **Manual Reset Input**
- **Guaranteed Reset Valid to V_{CC} = 1.0V**
- **Immune to Short V_{CC} Transient**

Ordering Information

PART	RESET OUTPUT TYPE	PIN-PACKAGE
MAX16072RS_ _D_+	Push-Pull, Active-Low	4 UCSP
MAX16073RS_ _D_+	Push-Pull, Active-High	4 UCSP
MAX16074RS_ _D_+	Open-Drain, Active-Low	4 UCSP

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

Insert the desired suffix numbers (from Table 1) into the blanks "RS_ _D" to indicate the reset trip threshold. Insert the desired suffix number (from Table 2) into the blank "D_+" to indicate the reset timeout. Minimum order quantity may apply.

+Denotes a lead(Pb)-free/RoHS-compliant package.

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µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC}, $\overline{MR}$ .....-0.3V to +6V
RESET, $\overline{RESET}$ Push-Pull ..... -0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ Open-Drain.....-0.3V to +6V
Output Current (all pins) ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
4-Bump UCSP (derate 3mW/°C above +70°C) 239mW

Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature .....+150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.5V to 2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.6V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +85°C		1.0		5.5	V
		T_A = -40°C to +85°C		1.2		5.5	
Supply Current	I_{CC}	V_{CC} = 1.8V for $V_{TH} \le$ 1.66V			0.7	1.2	µA
		V_{CC} = 3.6V, no load			1.0	1.5	
Detector Threshold	V_{TH}	See Table 1	V_{CC} falling, T_A = +25°C	V_{TH} - 1.5%	V_{TH}	V_{TH} + 1.5%	V
			V_{CC} falling, T_A = -40°C to +85°C	V_{TH} - 2.5%	V_{TH}	V_{TH} + 2.5%	
Detector Threshold Hysteresis	V_{HYST}	V_{CC} rising, $V_{TH} \le$ 1.66V (Note 2)			6.3		mV
Detector Threshold Tempco	ΔV_{TH}/°C	(Note 2)			40		ppm/°C
$\overline{MR}$ INPUT							
$\overline{MR}$ Input High Voltage	V_{IH}			0.7 x V_{CC}			V
	V_{IL}					0.7 x V_{CC}	
$\overline{MR}$ Pullup Resistance				25	50	75	kΩ
$\overline{RESET}$/RESET OUTPUT (Note 3)							
Output-Voltage Low	V_{OL}	$V_{CC} \ge$ 1.2V, I_{SINK} = 100µA				0.4	V
		$V_{CC} \ge$ 1.65V, I_{SINK} = 1mA				0.3	
Output-Voltage High	V_{OH}	$V_{CC} \ge$ 1.65V, I_{SOURCE} = 500µA		0.8 x V_{CC}			V
		$V_{CC} \ge$ 1.2V, I_{SOURCE} = 50µA		0.8 x V_{CC}			
Open-Drain $\overline{RESET}$ Output Leakage Current		$\overline{RESET}$ not asserted (Note 2)				0.1	µA
TIMING							
$\overline{MR}$ Minimum Pulse Width	t_{MPW}	(Note 2)		0.8			µs
$\overline{MR}$ Glitch Rejection	t_{EGR}	(Note 2)			100		ns
$\overline{MR}$ to RESET/$\overline{RESET}$ Propagation Delay	t_{OFF}	$\overline{MR}$ falling			1	2	µs
	t_{ON}	$\overline{MR}$ rising			200	400	ns
V_{CC} to Reset Delay	t_{DL}	V_{CC} = (V_{TH} + 100mV) to (V_{TH} -100mV)			20	90	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.5V to 2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.6V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Active Timeout Period	t_{RP}	V_{CC} rising, V_{CC} = (V_{TH} - 100mV) to (V_{TH} + 100mV)	MAX1607_RSD0+	20	80	120	µs
			MAX1607_RSD1+	8	13	17	ms
			MAX1607_RSD2+	34	52	69	ms
			MAX1607_RSD3+	140	210	280	ms

Note 1: Production testing done at T_A = +25°C only. Overtemperature limits are guaranteed by design and are not production tested.

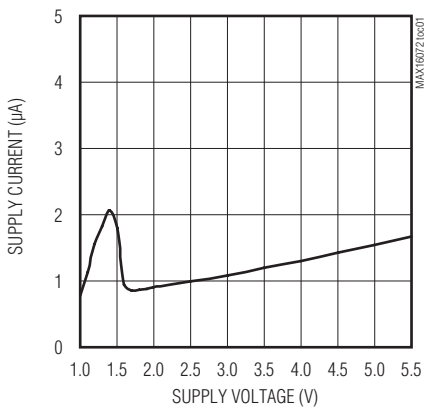
Note 2: Guaranteed by design.

Note 3: Reset is guaranteed down to V_{CC} = 1.0V.

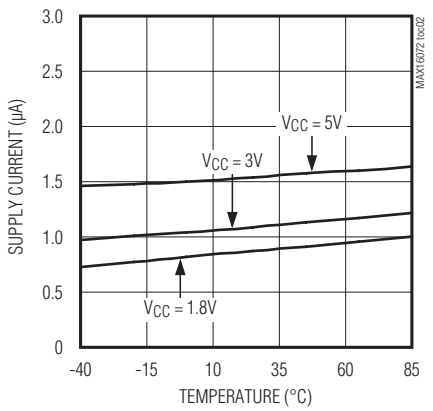
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

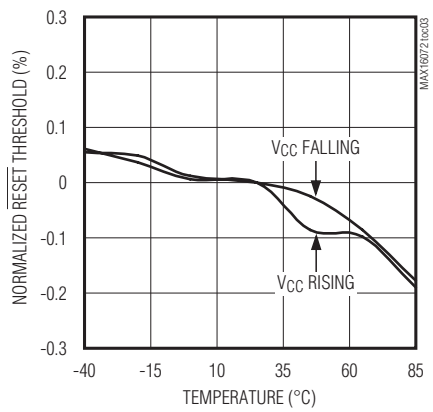
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED $\overline{\text{RESET}}$ THRESHOLD vs. TEMPERATURE

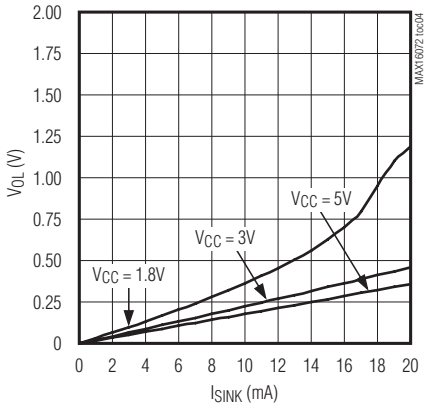


µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package

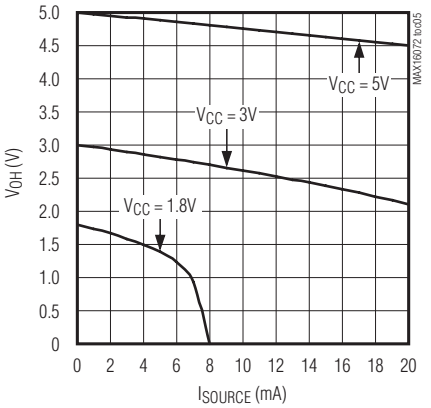
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

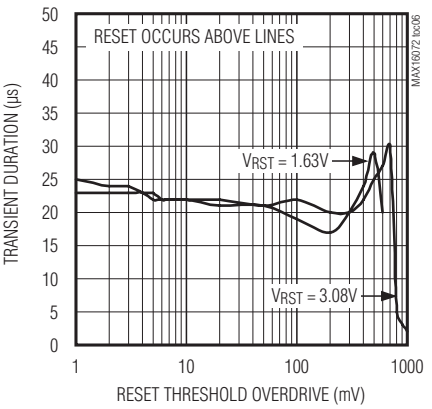
OUTPUT LOW VOLTAGE vs. SINK CURRENT



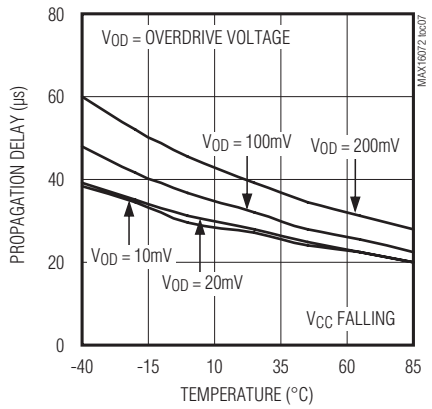
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



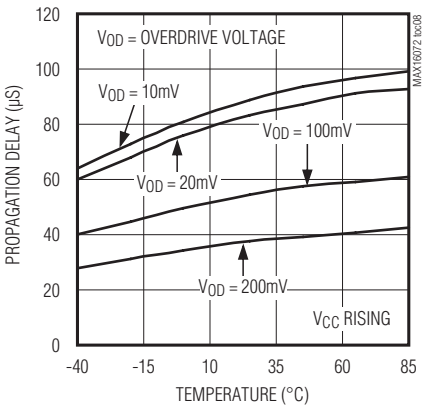
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



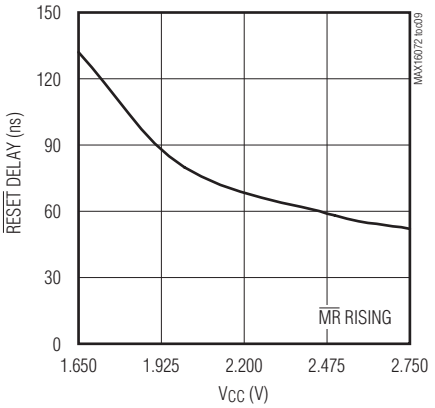
VCC TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



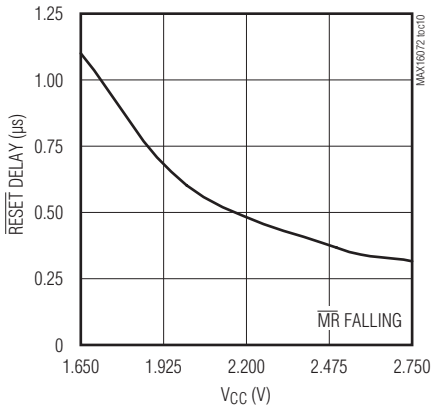
VCC TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



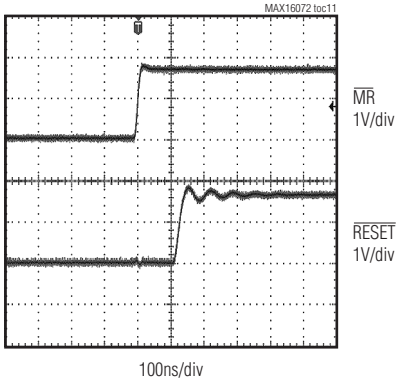
$\overline{MR}$ TO $\overline{RESET}$ DELAY (t_{ON}) vs. VCC



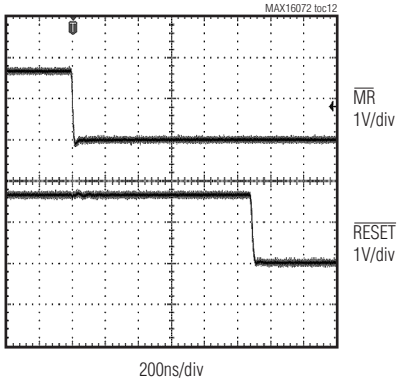
$\overline{MR}$ TO $\overline{RESET}$ DELAY (t_{OFF}) vs. VCC



$\overline{MR}$ TURN-ON

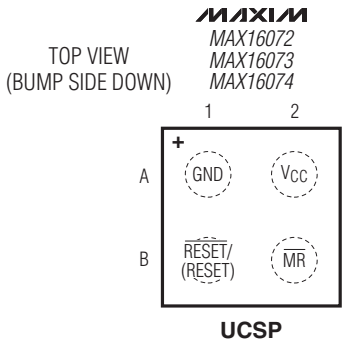


$\overline{MR}$ TURN-OFF



µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package

Bump Configuration



UCSP

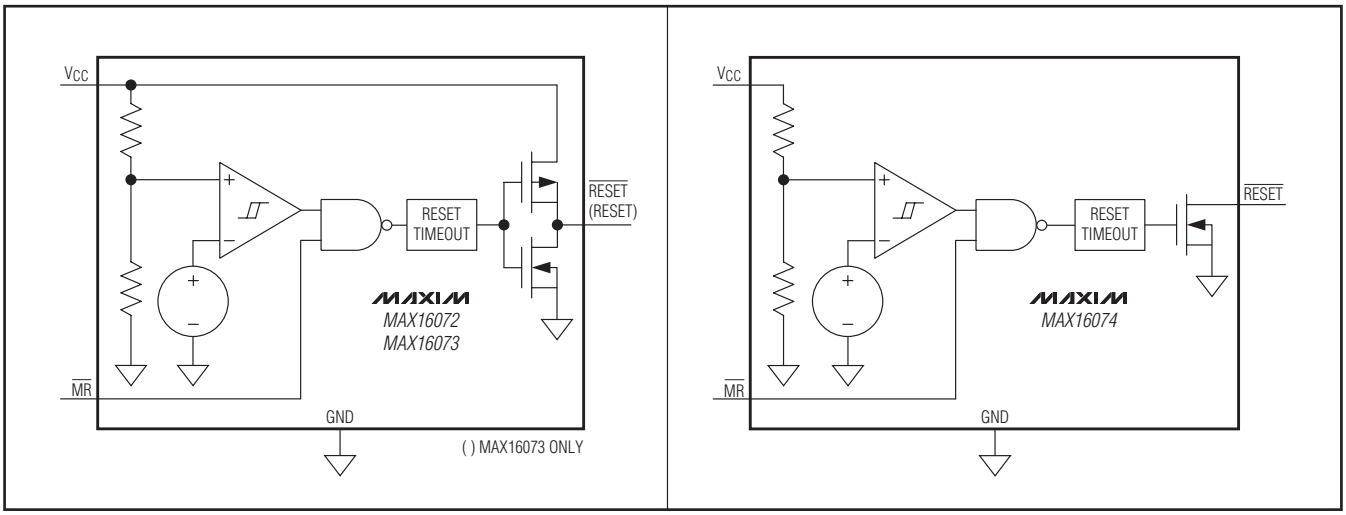
( ) FOR THE MAX16073 ONLY

Bump Description

BUMP			NAME	FUNCTION
MAX16072	MAX16073	MAX16074		
A1	A1	A1	GND	Ground
B1	—	—	$\overline{\text{RESET}}$	Active-Low Push-Pull Reset Output. $\overline{\text{RESET}}$ changes from high to low when V_{CC} drops below the detector threshold (V_{TH}) or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds V_{TH} and $\overline{\text{MR}}$ is high. When $\overline{\text{MR}}$ is low, $\overline{\text{RESET}}$ is low.
—	B1	—	RESET	Active-High Push-Pull Reset Output. $\overline{\text{RESET}}$ changes from low to high when V_{CC} drops below the detector threshold (V_{TH}) or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains high for the reset timeout period after V_{CC} exceeds V_{TH} and $\overline{\text{MR}}$ is high. When $\overline{\text{MR}}$ is low, $\overline{\text{RESET}}$ is high.
—	—	B1	$\overline{\text{RESET}}$	Active-Low Open-Drain Reset Output. $\overline{\text{RESET}}$ changes from high-impedance to active-low when V_{CC} drops below the detector threshold (V_{TH}) or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the reset threshold and $\overline{\text{MR}}$ is high. When $\overline{\text{MR}}$ is low, $\overline{\text{RESET}}$ is low.
A2	A2	A2	V_{CC}	Supply Voltage and Input for the Reset Threshold Monitor
B2	B2	B2	$\overline{\text{MR}}$	Active-Low Manual-Reset Input. Drive low to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is low and for the reset timeout period (if applicable) after $\overline{\text{MR}}$ is driven high. $\overline{\text{MR}}$ has an internal pullup resistor connected to V_{CC}, and may be left unconnected if not used.

µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package

Functional Diagrams



Detailed Description

The MAX16072/MAX16073/MAX16074 ultra-small, ultra-low-power, µP supervisory circuits feature a precision band-gap reference, comparator, and internally trimmed resistors that set specified trip threshold voltages. Designed to monitor the system supply voltage and an output during power-up, power-down, and brownout conditions, these devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltage from 1.8V to 3.6V.

The MAX16072 has a push-pull active-low reset output, the MAX16073 has a push-pull active-high reset output, and the MAX16074 has an open-drain active-low reset output. The devices are designed to ignore fast transients on V_{CC}. The devices also include a manual reset input ($\overline{MR}$). When $\overline{MR}$ is low, reset is asserted. When $\overline{MR}$ is high and V_{CC} is above the detector threshold (V_{TH}), reset is not asserted.

Supply and Monitored Input (Vcc)

The MAX16072/MAX16073/MAX16074 operate with a V_{CC} supply voltage from 1.2V to 2.75V. V_{CC} has a rising threshold of $V_{TH} + V_{HYST}$ and a falling threshold of V_{TH}. When V_{CC} rises above $V_{TH} + V_{HYST}$ and $\overline{MR}$ is high, $\overline{RESET}$ goes high (RESET goes low) after the reset timeout period (t_{RP}). See Figure 1.

When V_{CC} falls below V_{TH}, $\overline{RESET}$ goes low (RESET goes high) after a fixed delay (t_{RD}).

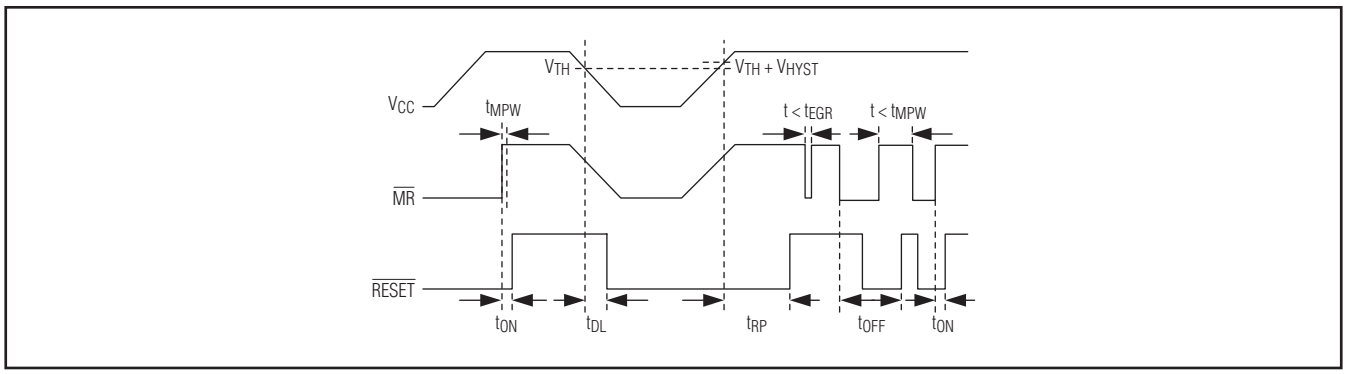


Figure 1. MAX16072/MAX16073/MAX16074 Timing Diagram

Manual Reset Input ($\overline{MR}$)

Many μP-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuit to initiate a reset. A logic-low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the reset active timeout period (t_{RP}) or delay (t_{ON}) after $\overline{MR}$ returns high. This input has an internal 50kΩ pullup resistor, so it can be left unconnected if it is not used. $\overline{MR}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. For manual operation, connect a normally open momentary switch from $\overline{MR}$ to GND; external debouncing circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connect a 0.1μF capacitor from $\overline{MR}$ to ground to provide additional noise immunity.

Applications Information

Interfacing to μP with Bidirectional Reset Pins

Since $\overline{RESET}$ on the MAX16074 is open-drain, this device interfaces easily with μPs that have bidirectional reset pins. Connecting the μP supervisor's $\overline{RESET}$ output directly to the μP's $\overline{RESET}$ pin with a single pullup resistor allows either device to assert reset (Figure 2).

Negative-Going V_{CC} Transients

The MAX16072/MAX16073/MAX16074 family of devices is relatively immune to short-duration, negative-going V_{CC} transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Threshold Overdrive graph, for which reset pulses are not generated. The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have when issuing a reset signal. As the amplitude of the transient increases, the maximum allowable pulse width decreases.

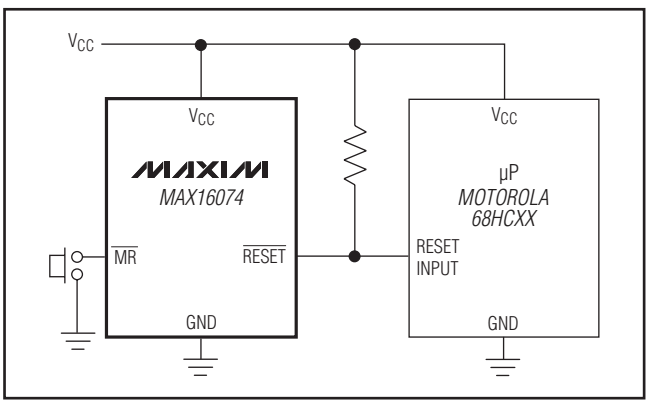


Figure 2. Interfacing to μP with Bidirectional Reset Pins

Table 1. Factory Trimmed Reset Thresholds

THRESHOLD SUFFIX	RESET TRIP THRESHOLD (V)		
	T_A = +25°C	T_A = -40°C to +85°C	
	TYP	MIN	MAX
15	1.58	1.54	1.61
16	1.63	1.60	1.66
17	1.67	1.62	1.71
18	1.80	1.76	1.85
19	1.90	1.85	1.95
20	2.00	1.95	2.05
21	2.10	2.05	2.15
22	2.20	2.145	2.25
23	2.32	2.262	2.375
24	2.40	2.34	2.46
25	2.50	2.437	2.562
26	2.63	2.564	2.69
27	2.70	2.633	2.768
28	2.80	2.63	2.87
29	2.93	2.857	3.0
30	3.00	2.925	3.075
31	3.08	3.003	3.15

Table 2. Reset Timeout Periods

RESET TIMEOUT PERIODS				
SUFFIX	MIN	TYP	MAX	UNITS
0	20	80	120	μs
1	8	13	17	ms
2	34	52	69	ms
3	140	210	280	ms

µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
4 UCSP	R41C1-1	21-0242