

### 3.3V SDRAM Buffer for Mobile PCS with 4 SO-DIMMs

#### Features

- One input to 10 output buffer/driver
- Supports up to four SDRAM SO-DIMMs
- Two additional outputs for feedback
- Serial interface for output control
- Low skew outputs
- Up to 133MHz operation
- Multiple  $V_{DD}$  and  $V_{SS}$  pins for noise reduction
- Dedicated OE pin for testing
- Space-saving 28 Pin SSOP package
- 3.3V operation

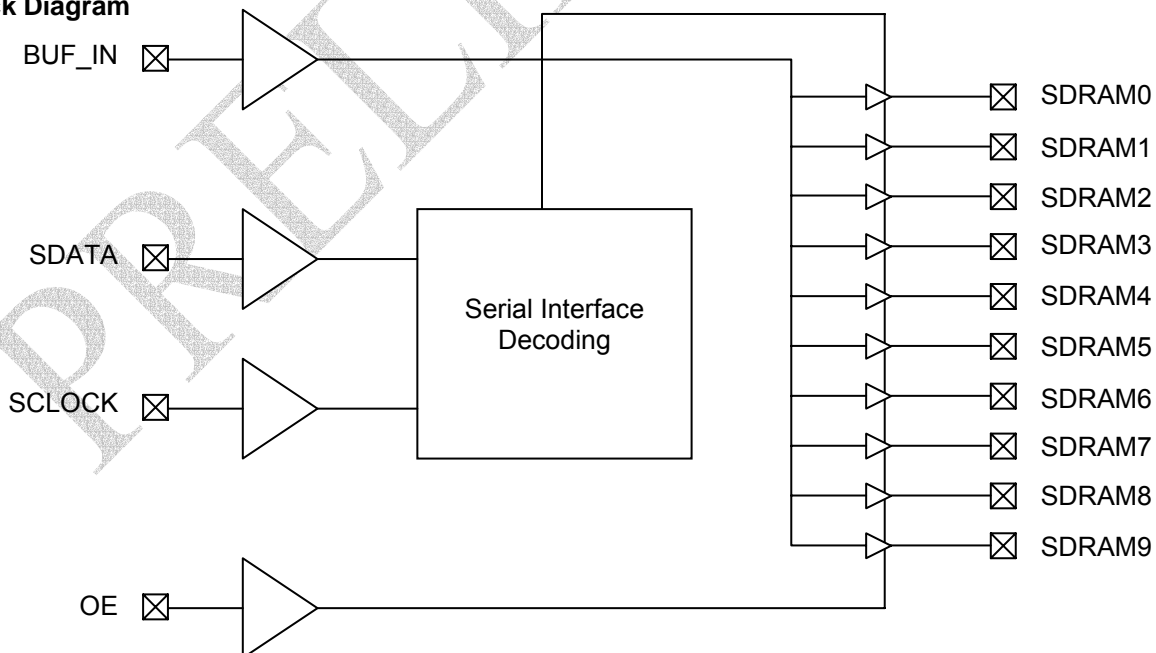
#### Functional Description

The PCS2I2310ANZ is a 3.3V buffer designed to distribute high-speed clocks in mobile PC applications. The part has 10 outputs, 8 of which can be used to drive up to four SDRAM SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 133MHz, thus making it compatible with Pentium II<sup>®</sup> processors.

The PCS2I2310ANZ also includes a serial interface (IIC), which can enable or disable each output clock. The IIC is Slave Receiver only and is Standard mode compliant. IIC Master can write into the IIC registers but cannot read back. The first two bytes after address should be ignored by IIC Block and data is valid after these two bytes as given in IIC Byte Flow Table. On power-up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

<sup>i</sup> Pentium II is a registered trademark of Intel Corporation

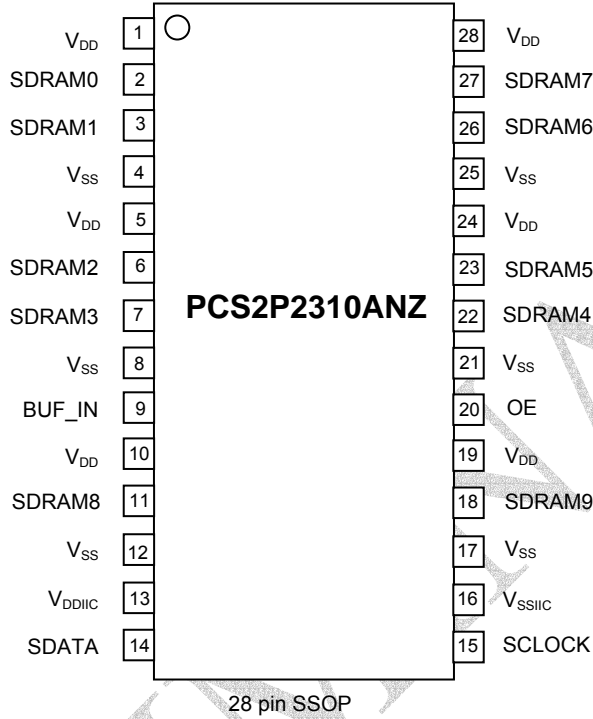
#### Block Diagram



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Pin Configuration

28 Pin SSOP Package-- Top View



Pin Description

Pins	Name	Type	Description
1, 5, 10, 19, 24, 28	V <sub>DD</sub>	P	3.3V Digital voltage supply
4, 8, 12, 17, 21, 25	V <sub>SS</sub>	P	Ground
13	V <sub>DDIIC</sub>	P	3.3V Serial interface voltage supply
16	V <sub>SSIIC</sub>	P	Ground for serial interface
9	BUF_IN	I	Input clock, 5V tolerant
20	OE	I	Output Enable, three-states outputs when LOW. Internal pull-up to V <sub>DD</sub>
14	SDATA	I/O	Bi-directional Serial data pin. Internal pull-up to V <sub>DD</sub> . 5V tolerant
15	SCLK	I	Serial clock input. Internal pull-up to V <sub>DD</sub> . 5V tolerant
2, 3, 6, 7	SDRAM [0-3]	O	SDRAM byte 0 Clock Outputs
22, 23, 26, 27	SDRAM [4-7]	O	SDRAM byte 1 Clock Outputs
11, 18	SDRAM [8-9]	O	SDRAM byte 2 Clock Outputs

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**Device Functionality**

OE	SDRAM [0-17]
0	High-Z
1	1 x BUF_IN

**Serial Configuration Map**

- The Serial bits will be read by the clock driver in the following order:
  - Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits can be programmed to either "0" or "1".
- Serial interface address for the PCS2I2310ANZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	---

**Byte 0: SDRAM Active/Inactive Register<sup>1</sup>  
(1 = Enable, 0 = Disable), Default = Enable**

Bit	Pin #	Description
Bit 7	--	Unused
Bit 6	--	Unused
Bit 5	--	Unused
Bit 4	--	Unused
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

Note 1: When the value of bit in these bytes is high, the output is enabled. When the value of the bit is low, the output is forced to low state. The default value of all the bits is high after chip is powered up.

**IIC Byte Flow**

Byte	Description
1	IIC Address
2	Command (dummy value, ignored)
3	Byte Count (dummy value, ignored)
4	IIC Data Byte 0
5	IIC Data Byte 1
6	IIC Data Byte 2

**Byte 1: SDRAM Active/Inactive Register<sup>1</sup>  
(1 = Enable, 0 = Disable), Default = Enable**

Bit	Pin #	Description
Bit 7	27	SDRAM7 (Active/Inactive)
Bit 6	26	SDRAM6 (Active/Inactive)
Bit 5	23	SDRAM5 (Active/Inactive)
Bit 4	22	SDRAM4 (Active/Inactive)
Bit 3	--	Unused
Bit 2	--	Unused
Bit 1	--	Unused
Bit 0	--	Unused

**Byte 2: SDRAM Active/Inactive Register<sup>1</sup>  
(1 = Enable, 0 = Disable), Default = Enable**

Bit	Pin #	Description
Bit 7	18	SDRAM9 (Active/Inactive)
Bit 6	11	SDRAM8 (Active/Inactive)
Bit 5	--	Reserved
Bit 4	--	Reserved
Bit 3	--	Reserved
Bit 2	--	Reserved
Bit 1	--	Reserved
Bit 0	--	Reserved

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Unit
V <sub>DD</sub>	Supply Voltage to Ground Potential	-0.5V to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Except BUF_IN)	-0.5V to V <sub>DD</sub> + 0.5	V
V <sub>INB</sub>	DC Input Voltage (BUF_IN)	-0.5V to +7.0	V
T <sub>STG</sub>	Storage Temperature	-65°C to +150	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2000	V

**Operating Conditions**

Parameter	Description	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	3.135	3.465	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	0	70	°C
C <sub>L</sub>	Load Capacitance	20	30	pF
C <sub>IN</sub>	Input Capacitance		7	pF
t <sub>PU</sub>	Power-up time for all V <sub>DD</sub> 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

**Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input LOW Voltage	Except serial interface pins			0.8	V
V <sub>ILIC</sub>	Input LOW Voltage	For serial interface pins only			0.7	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>OL</sub>	Output LOW Voltage <sup>1</sup>	I <sub>OL</sub> = 25 mA			0.4	V
V <sub>OH</sub>	Output HIGH Voltage <sup>1</sup>	I <sub>OH</sub> = -36 mA	2.4			V
I <sub>CC</sub>	Quiescent Supply Current	V <sub>DD</sub> = 3.465V, V <sub>i</sub> = V <sub>DD</sub> or GND I <sub>o</sub> = 0		50	100	µA
I <sub>OZ</sub>	High Impedance Output Current	V <sub>DD</sub> = 3.465V, V <sub>i</sub> = V <sub>DD</sub> or GND			±10	µA
I <sub>OFF</sub>	OffState Current (for SCL, SDATA)	V <sub>DD</sub> = 0V, V <sub>i</sub> = 0V or 5.5V			50	µA
ΔI <sub>CC</sub>	Change in Supply Current	V <sub>DD</sub> = 3.135V to 3.465V One Input at V <sub>DD</sub> -0.6, All other Inputs at V <sub>DD</sub> or GND			500	µA
I <sub>i</sub>	Input Leakage	V <sub>DD</sub> = 3.465V or GND (Applicable to all Input Pins)	-5		+5	µA
I <sub>DD</sub>	Supply Current <sup>1</sup>	Unloaded outputs, 133MHz			266	mA
I <sub>DD</sub>	Supply Current <sup>1</sup>	Loaded outputs, 30pF, 133MHz			360	mA
I <sub>DD</sub>	Supply Current <sup>1</sup>	Unloaded outputs, 100MHz			200	mA
I <sub>DD</sub>	Supply Current <sup>1</sup>	Loaded outputs, 30pF, 100MHz			290	mA
I <sub>DD</sub>	Supply Current <sup>1</sup>	Unloaded outputs, 66.67MHz			150	mA
I <sub>DD</sub>	Supply Current <sup>1</sup>	Loaded outputs, 30pF, 66.67MHz			185	mA
I <sub>DDS</sub>	Supply Current	BUF_IN = V <sub>DD</sub> or V <sub>SS</sub> , all other inputs at V <sub>DD</sub>			500	µA

Note: 1. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics<sup>1</sup>

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
$f_{max}$	Maximum Operating Frequency				133	MHz
$t_D$	Duty Cycle <sup>2,3</sup> = $t_2 \div t_1$	Measured at 1.5V	45.0	50.0	55.0	%
$t_3$	Rising Edge Rate <sup>3</sup>	Measured between 0.4V and 2.4V	1	2	4	V/nS
$t_4$	Falling Edge Rate <sup>3</sup>	Measured between 2.4V and 0.4V	1	2	4	V/nS
$t_5$	Output to Output Skew <sup>3</sup>	All outputs equally loaded		150	225	pS
$t_6$	SDRAM Buffer LH Prop. Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	2.7	3.5	nS
$t_7$	SDRAM Buffer HL Prop. Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	2.7	3.5	nS
$t_{PLZ}, t_{PHZ}$	SDRAM Buffer Enable Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	3	5	nS
$t_{PZL}, t_{PZH}$	SDRAM Buffer Disable Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	3	5	nS
$t_r$	Rise Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3	$C_L = 10pF$	6			nS
		$C_L = 400pF$			250	
$t_f$	Fall Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3	$C_L = 10pF$	20			nS
		$C_L = 400pF$			250	

Note: 1. All parameters specified with loaded outputs.  
 2. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/nS  
 3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Test Circuit for SDRAM Enable and Disable Times

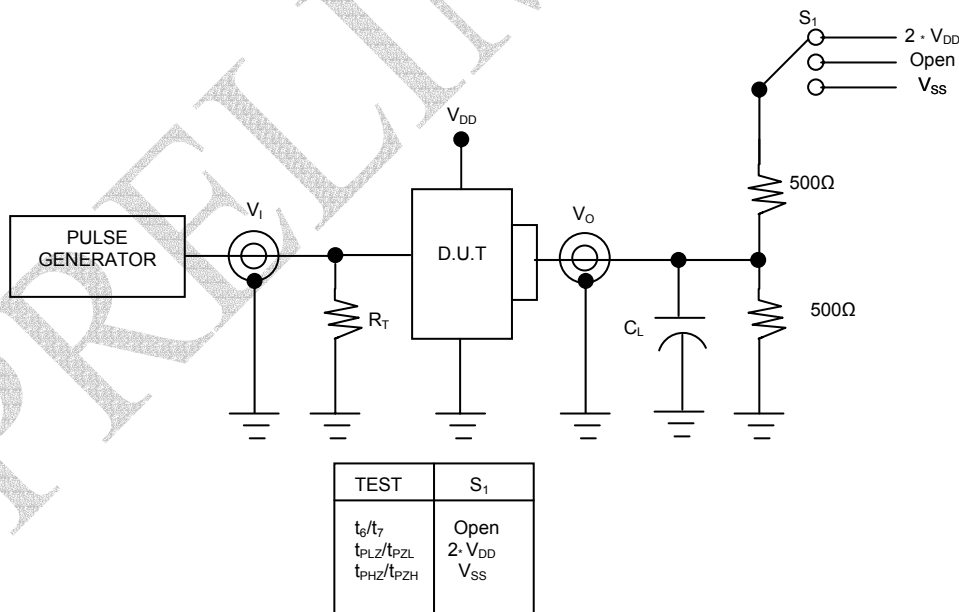


Figure 1. Load circuit for Switching times

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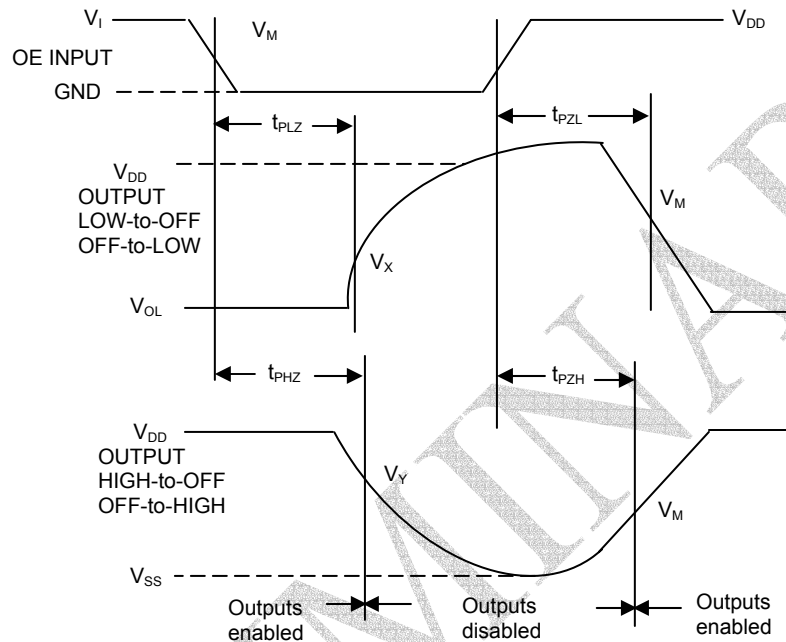
**SDRAM Enable and Disable Times**

$V_M = 1.5V$

$V_X = V_{OL} + 0.3V$

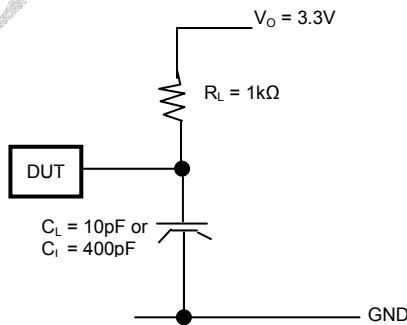
$V_Y = V_{OH} - 0.3V$

$V_{OH}$  and  $V_{OL}$  are the typical Output Voltage drop that occur with the output load



**Figure 2. 3-State Enable and Disable times**

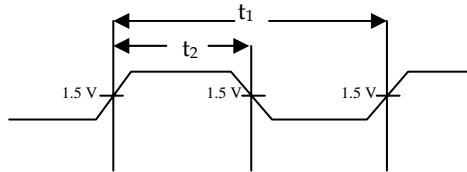
**Test Circuit for IIC Rise and Fall Times**



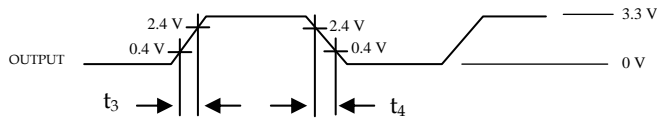
**Figure 3. Test Circuit for IIC**

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Switching Waveforms

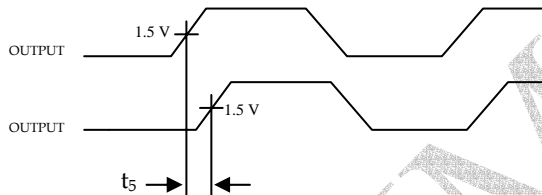
Duty Cycle Timing



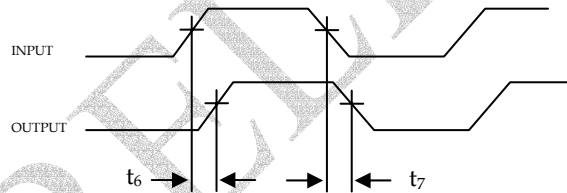
All Outputs Rise/Fall Time



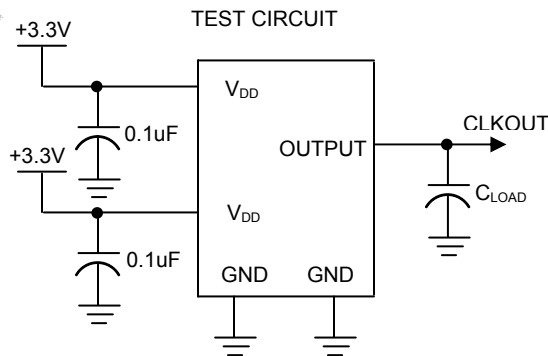
Output - Output Skew



SDRAM Buffer LH and HL Propagation Delay

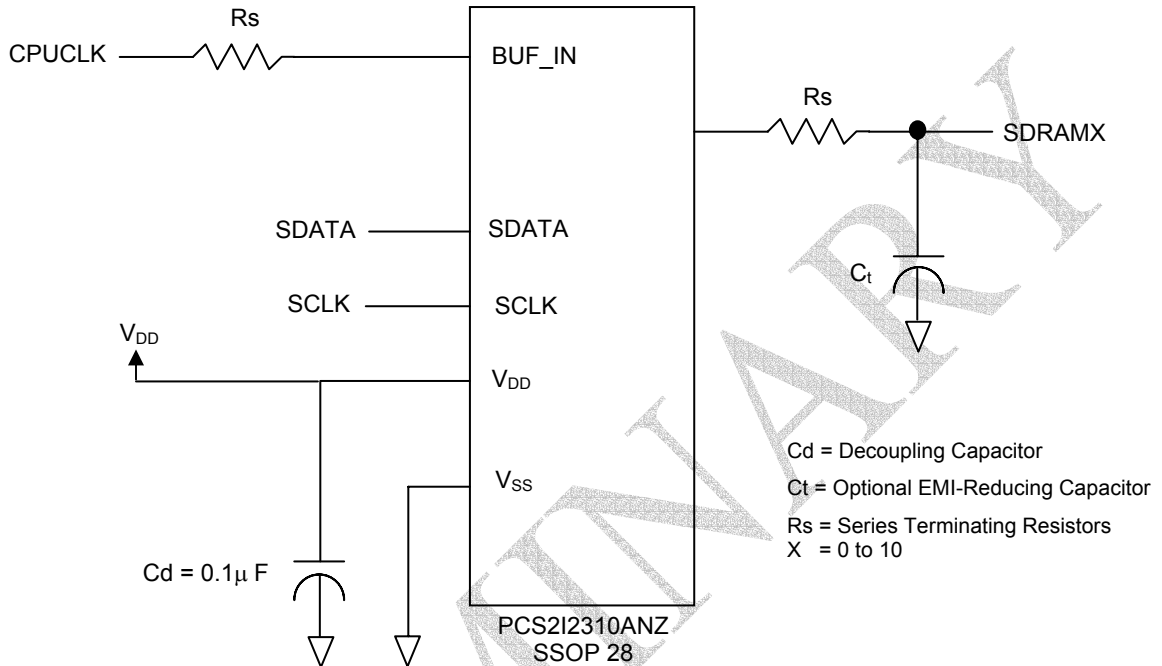


Test Circuits



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Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.



Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically 25Ω), and Rseries is the series terminating resistor.  
$$R_{series} > R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7pF to 22pF.
- A Ferrite Bead may be used to isolate the Board VDD from the clock generator VDD island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions.
- If a Ferrite Bead is used, a 10µF–22µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.



**IIC Serial Interface Information**

The information in this section assumes familiarity with IIC programming.

**How to program PCS2I2310ANZ through IIC:**

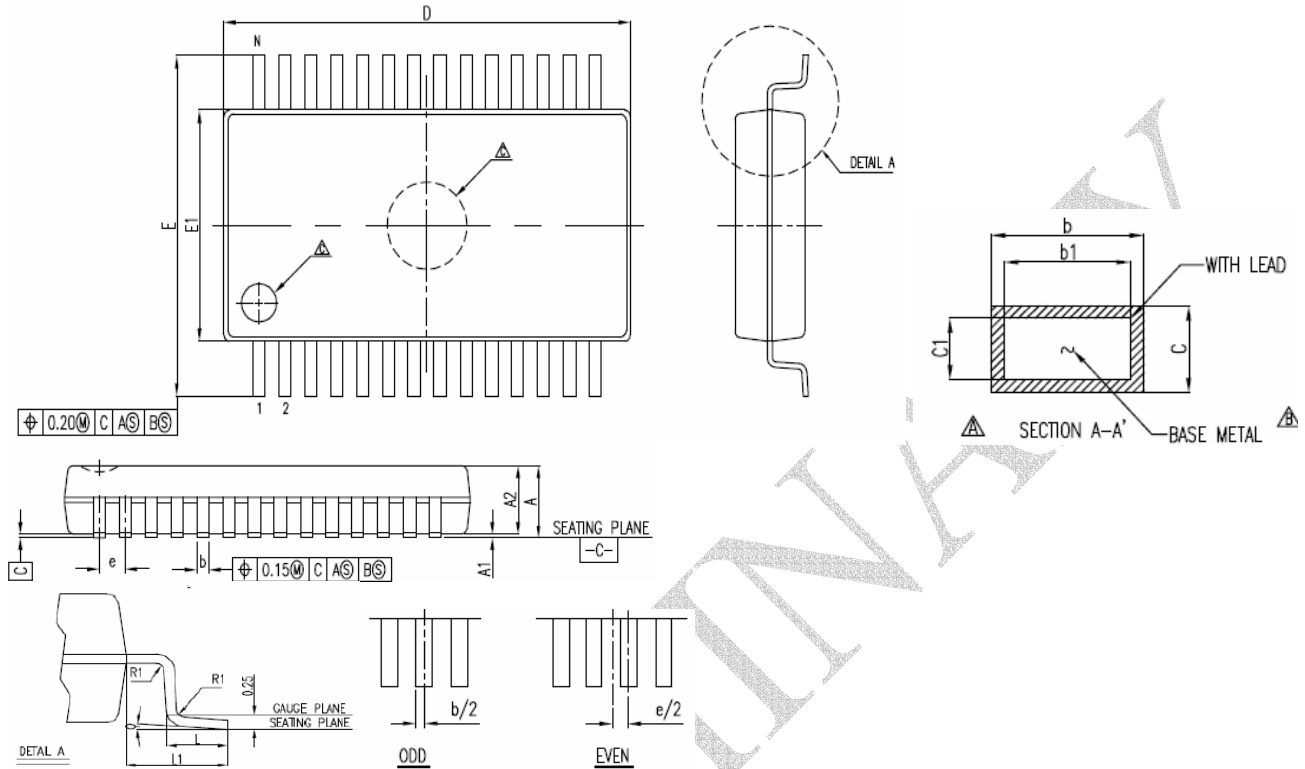
- Master (host) sends a start bit.
- Master (host) sends the write address D3 (H).
- PCS2I2310ANZ device will acknowledge.
- Master (host) sends the Command Byte.
- PCS2I2310ANZ device will acknowledge the Command Byte.
- Master (host) sends a Byte count
- PCS2I2310ANZ device will acknowledge the Byte count.
- Master (host) sends the Byte 0
- PCS2I2310ANZ device will acknowledge Byte 0
- Master (host) sends the Byte 1
- PCS2I2310ANZ device will acknowledge Byte 1
- Master (host) sends the Byte 2
- PCS2I2310ANZ device will acknowledge Byte 2
- Master (host) sends a Stop bit.

Controller (Host)	PCS2I2310ANZ (slave/receiver)
Start Bit	
Slave Address D3(H)	
	ACK
Command Byte	
	ACK
Byte count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Stop Bit	

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Package Information

28L SSOP (209 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.079	...	2.0
A1	0.002	...	0.05	...
A2	0.065	0.073	1.65	1.85
D	0.394	0.409	10.00	10.40
L	0.021	0.037	0.55	0.95
E	0.295	0.319	7.50	8.10
E1	0.197	0.220	5.00	5.60
R1	0.004	....	0.09	.....
b	0.009	0.015	0.22	0.38
b1	0.009	0.013	0.22	0.33
c	0.004	0.010	0.09	0.25
c1	0.004	0.008	0.09	0.21
L1	0.050REF		1.25 REF	
e	0.026 BSC		0.65 BSC	
θ	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS2P2310ANZG-28-AT	2P2310ANZG	28-pin SSOP –Tube, Green	Commercial
PCS2P2310ANZG-28-AR	2P2310ANZG	28-pin SSOP –Tape and Reel, Green	Commercial
PCS2I2310ANZG-28-AT	2I2310ANZG	28-pin SSOP –Tube, Green	Industrial
PCS2I2310ANZG-28-AR	2I2310ANZG	28-pin SSOP –Tape and Reel, Green	Industrial

Device Ordering Information

PCS2I2310ANZG-28-AR

R = Tape & Reel, T = Tube or Tray

O = SOT	U = MSOP
S = SOIC	E = TQFP
T = TSSOP	L = LQFP
A = SSOP	U = MSOP
V = TVSOP	P = PDIP
B = BGA	D = QSOP
Q = QFN	X = SC-70

DEVICE PIN COUNT

G = GREEN PACKAGE, LEAD FREE, and RoHS

PART NUMBER

X= Automotive (-40C to +125C)    I= Industrial (-40C to +85C)    P or n/c = Commercial (0C to +70C)

1 = Reserved	6 = Power Management
2 = Non PLL based	7 = Power Management
3 = EMI Reduction	8 = Power Management
4 = DDR support products	9 = Hi Performance
5 = STD Zero Delav Buffer	0 = Reserved

PulseCore Semiconductor Mixed Signal Product

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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