F72569

ACPI Controller IC for AMD K8/AM2 Platform

Release Date: Oct, 2006
Version: 0.26P

F72569 Datasheet Revision History

Version	Date	Page	Revision History
0.20P	Dec, 2005		Preliminary version
0.21P	Apr, 2006		Model name modification
0.22P	May, 2006		Re-compose
		1	Delete the description about Vref for overclock
		14	Description of linear controller correction
		23	Application circuit correction
0.23P	June, 2006	1	Delete the description about Vref in general description
0.24P	Aug, 2006	11	Add over current protection description
0.25P	Sep,2006	3	Pin description
		20	Application circuit correction
0.26P	Oct, 2006	20	Application circuit correction

Table of Contents

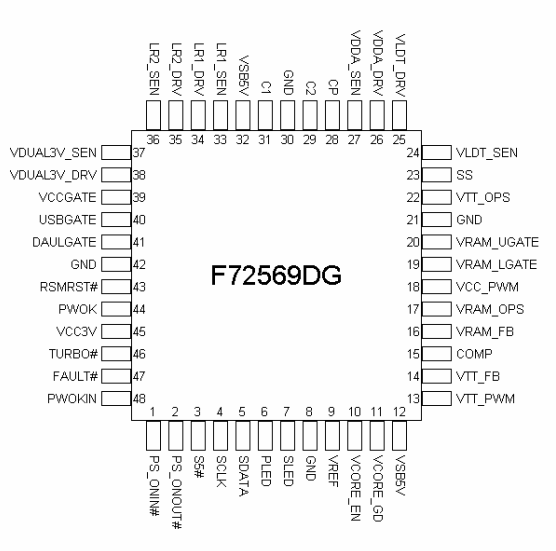
1 General Description

The F72569 is a fully compliant ACPI controller IC specific for AMD K8 CPU platform. The chip is used with an ATX power supply, and it integrates synchronous PWM controllers, regulators, several linear controllers, switching signals, monitoring and control function into a 48 pin LQFP package. Its operation mode (sleep or active) is selectable through some control signals. The F72569 provides 3 switch signals which can provide $5V_{DUAL}$, $5V_{USB}$ & $3.3V_{DUAL}$ etc. The F72569 can also provide 5 linear regulators for system requirements. This chip integrates a charge pump engine to provide higher driving voltage for appropriate gate during standby. Besides, this chip offers current limiting that protects each PWM outputs, and provides soft-start for a linear regulator to avoid rush current. The power LED is programmable and compliant with PC2001. Moreover, this high-performance chip integrates I^2C interface and provides adjustable linear controllers mechanism for dynamic over/under-voltage use. This chip is in a 48pin LQFP package and powered by 5VSB.

2 Feature

- Compliant with AMD K8 timing sequence
- Provide 3 switching controlled signals for $5V_{DUAL}$, $5V_{USB}$ and $3.3V_{DUAL}$
- Programmable $5V_{DUAL}$/$5V_{STR}$/$5V_{CC}$ for USB device wake up
- Provide 5 linear controller and typically use for –
  - -- 1 channel for DUAL3V power
  - -- 1 channel for VDDA power
  - -- 1 channel for VLDT power
  - -- 2 channels for 0.8~5V voltage requirement
- Provide one PWM controller for DDR V_{DDQ}
- Provide one PWM regulator for chipset power requirement
- 1 PWROK input signal(typically from ATXPWOKIN) and 1 PWROK output signal
- Provide resume reset signal(RSMRST#)
- Programmable power LED control
- Provide V_{REF} and VSB9V voltage for generating different voltage use
- Power up soft-start and under-voltage monitoring for the linear regulators
- Over current protection(OCP) on PWM controller and under-voltage monitoring of all linear regulators
- Integrate I^2C interface
- 48 pin LQFP package and 5VSB operation

3 Pin Configuration



4 Pin Description

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12ts} - TTL level and schmitt trigger

I/OD_{16} - TTL level bi-directional pin. Open-drain output with 16 mA sink capability

OUT_{12} - Output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{16} - Open-drain output pin with 16 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

O_{24V4} - Output pin with 24mA driving capability, output 4V

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

AOUT - Output pin(Analog)

P - Power

◆ ***Power Pins***

PIN NO	PIN NAME	TYPE	DESCRIPTION
8	GND	P	Power pins
12	VSB5V		
21	GND		
30	GND		
32	VSB5V		
42	GND		
45	VCC3V		
18	VCC_PWM		VRAM_UGATE and VRAM_LGATE signal power, recommend to connect to Vcc12V

◆ ***Reset & Power Good & Control signal***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
1	PS_ONIN#	IN_{ts}	VSB5V	Normal power control signal input.
2	PS_ONOUT#	OD_{12}	VSB5V	Power control signal output. Connected to ATX power ON/OFF pin, normally.
3	S5#	IN_{ts}	VSB5V	A low active ACPI control signal governs the S5 state. Typically, connected to chipset S5# signal.
10	VCORE_EN	OD_{12}	VSB5V	This pin is the open drain output to control CPU Vcore power enabled signal.
11	VCORE_GD	IN_{ts}	VSB5V	This pin is the CPU Vcore power ready signal input.
43	RSMRST#	OD_{12}	VSB5V	As VSB arrives at 3.3V, this pin will generate RSMRST# signal output after 66ms.
44	PWOK	OD_{16}	VSB5V	Power Good output signal.
46	TURBO#	IN_{ts}	VSB5V	Enable adjustable power signal.
47	FAULT#	IN_{ts}	VSB5V	Error input signal for power off.
48	PWOKIN	IN_{ts}	VSB5V	Power Good Schmitt Trigger input signal. Typically, connected to ATX power Good.

◆ ***Switching Signal & Linear/PWM Controller***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
13	VTT_PWM	OUT_5	VSB5V	External buffer PWM control output signal
14	VTT_FB	AIN	VSB5V	External buffer PWM feedback signal
15	COMP	AOUT	VSB5V	Output of the error amplifier used to compensate the feedback loop of the PWM controller.

16	VRAM_FB	AIN	VSB5V	VRAM PWM feedback signal
17	VRAM_OPS	AOUT/AIN	VSB5V	VRAM PWM current protection signal
19	VRAM_LGATE	O	VCC_PWM	VRAM PWM low gate control signal
20	VRAM_UGATE	O	VCC_PWM	VRAM PWM up gate control signal
22	VTT_OPS	AOUT/AIN	VSB9V	External buffer PWM current protection signal
24	VLDT_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. VLDT_SEN and VLDT_DRV act as a linear regulator and generate voltage for S0 state power.
25	VLDT_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. VLDT_SEN and VLDT_DRV act as a linear regulator and generate voltage for S0 state power.
26	VDDA_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. VDDA_SEN and VDDA_DRV act as a linear regulator and generate voltage and generate voltage for S0 sate power.
27	VDDA_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. VDDA_SEN and VDDA_DRV act as a linear regulator and generate voltage and generate voltage for S0 sate power.
33	LR1_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. LR1_SEN and LR1_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
34	LR1_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. LR1_SEN and LR1_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
35	LR2_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. LR2_SEN and LR2_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
36	LR2_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. LR2_SEN and LR2_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
37	DAUL3V_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. VDUAL3V_SEN and VDUAL3V_DRV act as an adjustable linear regulator and this regulator is typically incorporated with VCCGATE to generate dual voltage.
38	DUAL3V_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. VDUAL3V_SEN and VDUAL3V_DRV act as an adjustable linear regulator and this regulator is typically incorporated with VCCGATE to

				generate dual voltage.
39	VCCGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. Generate dual 3.3V voltage with VDUAL3V_DRV and VDUAL3V_SEN. Generate USB voltage with USBGATE. Generate dual 5V voltage with DUALGATE.
40	USBGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. Generate USB voltage with VCCGATE.
41	DUALGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. Generate dual 5V voltage with VCCGATE.

◆ ***Charge Pump***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
28	CP	P	VSB9V	Charge pump output (9V nominal). Decouple this pin with 1uF ceramic capacitor. VSB9V power output.
29	C2	AOUT	VSB9V	Positive end of charge pump capacitor
31	C1	AOUT	VSB5V	Negative end of charge pump capacitor. Connect a 1uF ceramic capacitor between C1 and C2

◆ ***Power LED***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
6	PLED	OD_{24}	VSB5V	Power LED. Can be programmed by setting register
7	SLED	OD_{24}	VSB5V	Suspend LED. Can be programmed by setting register

◆ ***Others***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
4	SCLK	IN_{ts}	VSB5V	I2C serial bus clock
5	SDATA	I/OD_{12ts}	VSB5V	I2C serial bus data
9	VREF	AOUT	VSB5V	Provide 1.25V reference voltage
23	SS	AIN	VSB5V	Soft-Start. Connect this pin to a small ceramic capacitor to determine the soft-start rate. The value of capacitor is bigger, and the slew rate is slower.

5 Electrical Characteristic

Absolute Maximum Ratings

PARAMETER	SYMBOL	RATINGS	UNIT
IC supply voltage	VCC		V
ESD classification	HBM		kV
※ Maximum junction temperature (plastic package)	T_j		°C
※ Maximum storage temperature	T_{STO}		°C
※ Maximum lead temperature (soldering 10s)			°C

Note: **If ICs are stressed beyond the limits listed in the "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.**

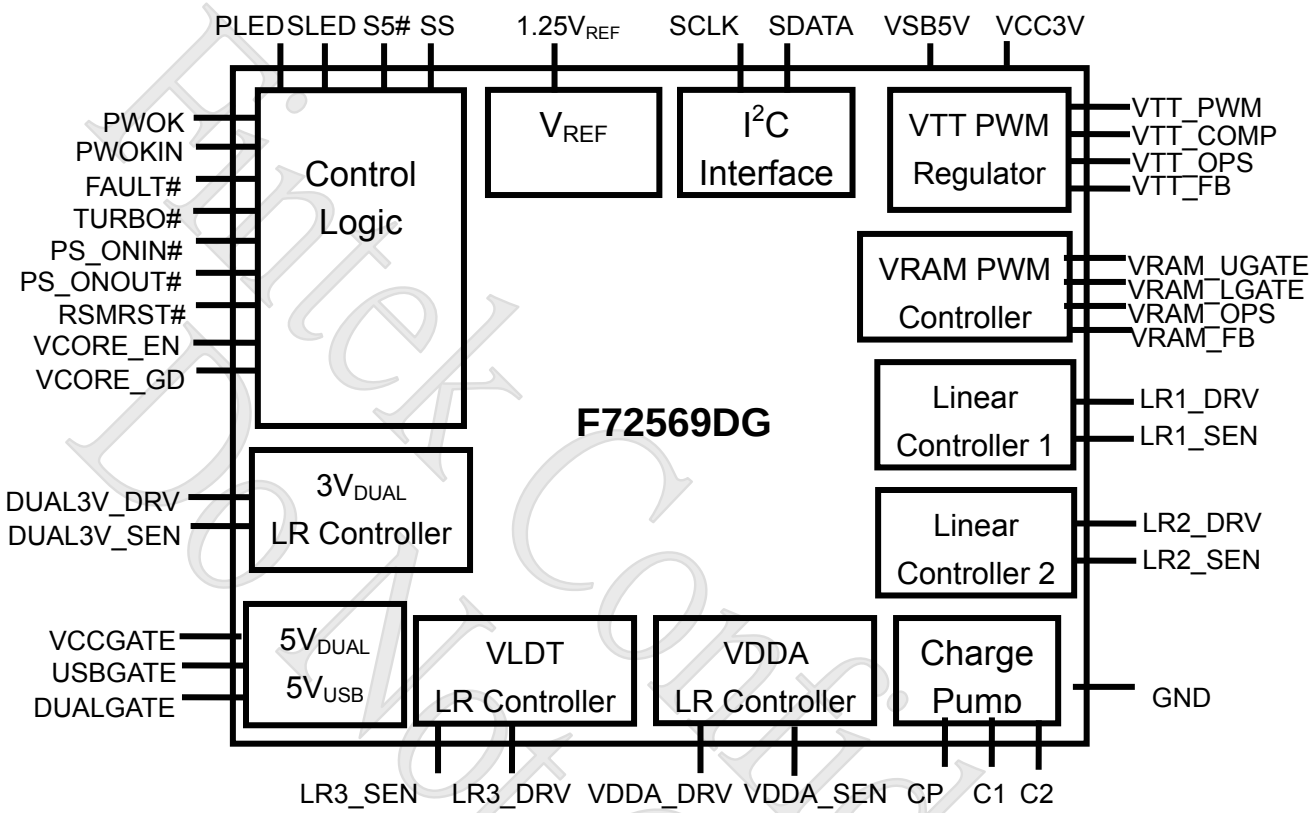
DC and AC electrical characteristics (VCC = 12V, TA = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCC SUPPLY CURRENT/Regulated Voltage						
Nominal supply current 5VCC	I_{CC}	UGATE, LGATE and DRIVE2 open		6	15	mA
POWER-ON RESET						
Rising VCC threshold			3.0	3.3	3.6	V
Falling VCC threshold			2.7	3.0	3.3	V
OSCILLATOR AND Soft-start						
Free running frequency	F_{OSC}		200	250	300	kHz
※ Ramp Amplitude	$\triangle V_{OSC}$			1.5		V_{P-P}
Soft-start interval	T_{SS}	Css=0.1u	8.4	12.4	17.4	ms
Dead time	T_{DT}	2V to 2V	20	30	50	ns
REFERENCE VOLTAGE						
Reference voltage	V_{REF}	VCC=5V, T= 25	0.784	0.8	0.816	V
PWM CONTROLLER GATE DRIVERS						
Upper Drive Source	R_{UGATE}	VDS = 1V, VGS = 12V,		7	14	Ω
Upper Drive Sink	R_{UGATE}	VDS = 1V, VGS = 12V		5	10	Ω
Lower Drive Source	R_{LGATE}	VDS = 1V, VGS = 12V		7	14	Ω
Lower Drive Sink	R_{LGATE}	VDS = 1V, VGS = 12V		5	10	Ω

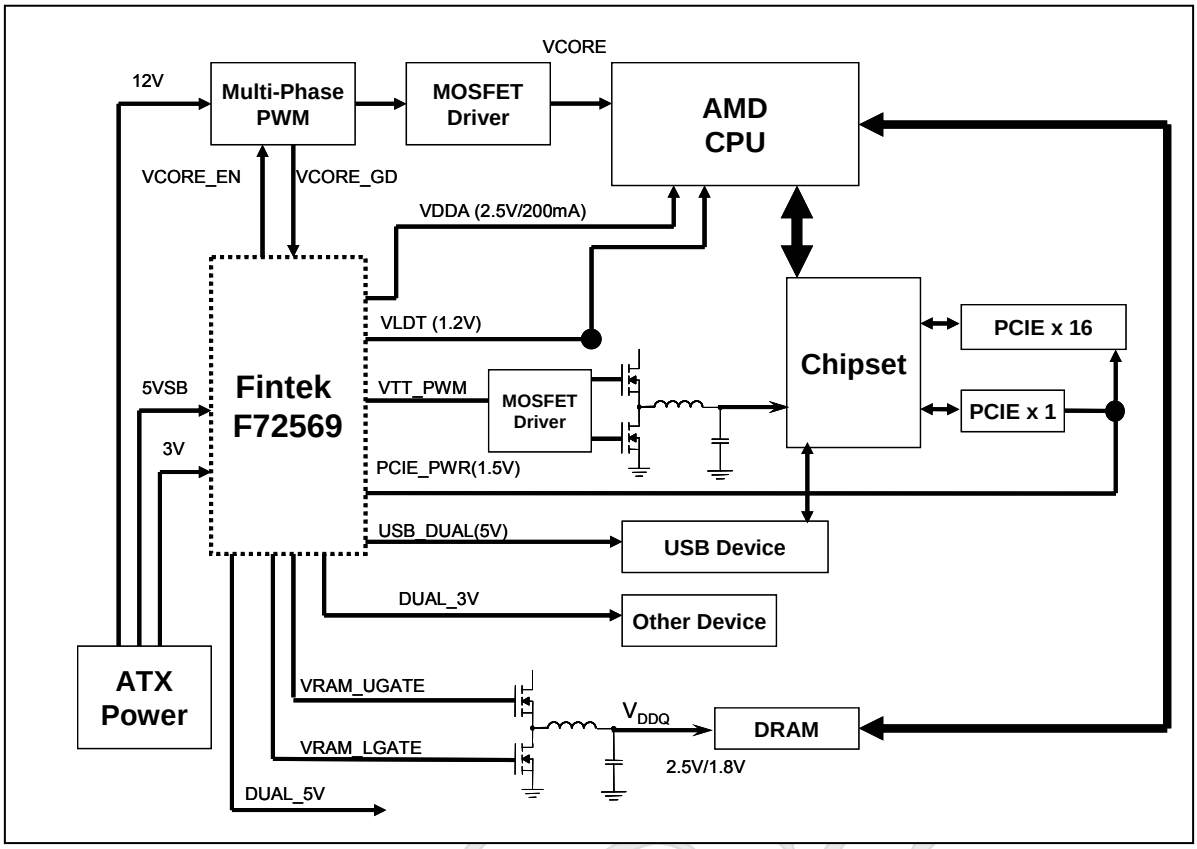
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Error Amplifier						
Slew Rate	SR			4.5		V/us
※ DC Gain	A0			34		dB
Linear Regulator						
DC Gain				70		dB
Gain Bandwidth Product				1.86		MHz
Slew Rate				38		V/us
Drive High Output Voltage				12		V
Drive Low Output Voltage				0		V
Drive High Output Source Current		Vo=9V; VDDA=10V			-0.54	mA
Drive Low Output Sink Current		Vo=1V; VDDA=10V		0.52		mA
Protection						
OCSET Current Source	I_{OCSET}			40		uA
FB Under Voltage Trip		FB Falling	0.4	0.5	0.6	V
VRAM(V_{DDQ}) UV Level			0.4	0.5	0.6	V
VTT_PWM (V_{GMCH}) UV Level			0.4	0.5	0.6	V
Charge Pump						
Charge Pump Frequency				250		KHz
Charge Pump Voltage				9.5		V
Switch Controller						
DUALGATE Output High Voltage				9.5		V
VCCGATE Output High Voltage			10.8	12	13.2	V
USBGATE SS Source Current			10.8	12	13.2	V

※: **Design Guarantee**

6 Block Diagram



7 Simplified Power System Diagram



8 Functional Description

8.1 ACPI state

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the usage of power in a computer. It lets computer manufacturers and users to determine the power usage of computer dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state and the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state the processor is powered down but the last state is being stored in memory which is still active. S5 is a state that memory is off and the last state of the

processor has been stored to the hard disk. Take S3 and S5 as a comparison, the computer can come back more quickly to full-power state in S3 than S5 due to data restored from the memory is faster than from the hard disk. However, S5 draws the minimal power compared to S0 and S3 because of powering off the memory.

It is anticipated that only the following state transitions may happen: S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5. Among them, S3→S5 is an illegal transition and won't be allowed by state machine. In order to enter to S5 from S3, it is necessary to come back to S0 first. The transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

8.2 Charge pump

The F72569 is incorporated with an embedded charge pump to provide higher driving voltage. Pin 29(CP) supports 10mA driving current and ensures 9V output voltage or above. In main operation, the VSB9V signals of the F72569 are run from the +12V supplied by ATX power which also supplies to other MOSFET gates. However, during standby state, the +12V will be off and it needs to provide power to the chip and the appropriate gates. Therefore, the F72567 is incorporated with a free running charge pump. As shown in the schematic, there is a capacitor connected between C1 and C2 of the F72569 act as a charge pump with internal diodes. There must be a serial diode in the 12V input to prevent back-feeding the charge pump to the +12V main in standby. It also needs a bypass capacitor connected with 12V input line to filter high-frequency noise.

8.3 Soft-start

SS of the F72569 acts as a soft-start function. As shown in the schematic, a ceramic capacitor is attached between this pin and the ground. When power is first applied to the chip, a constant current is applied from the pin into an external capacitor, linearly ramping up the voltage. This ramp in turn controls the internal reference of the F72569 which provides a soft-start for the linear regulator. Switches must be either on or off in the system to avoid the effect on them from the soft-start. It is important to know soft-start is not an enable signal, pulling it low will not be sure to turn off all outputs. If there are appropriate signals asserted, the switches will be turned on at once. The actual state of the F72569 in power up will be determined by the controlled input signal and the soft-start is effective only during power on.

8.4 Reference voltage

The pin10 (VREF) is an output pin that is driven by a small output buffer to provide the 1.25V reference voltage to other devices

in the system.

8.5 Over-current Protection

To sense the low-side MOSFET's RDS (ON) to set over-current trip point. Connecting a resistor (ROCSET) from this pin to PHASE to set the over-current trip point, ROCSET, an internal 40μA current source, and the lower MOSFET on resistance, RDS (ON), sets the converter over-current trip point (IOCSET) according to the following equation:

$$I_{OCSET} = \frac{40uA \times R_{OCSET} - 0.4V}{R_{DS(ON)} \text{ of the lower MOSFET}}$$

8.6 Access interface

The F72569 can be connected to a compatible 2-wire serial system Management Bus (SMBus) as a slave device under the control of the master device, using two device terminals SCL and SDA. The controller can provide a clock signal to the device SCL pin and read/write data from/to the device through the device SDA pin. The default address is 0x5E(0101_1110) and the operation of the device to the bus is described with details in the following sections.

(a) SMBus write to internal address register followed by the data byte

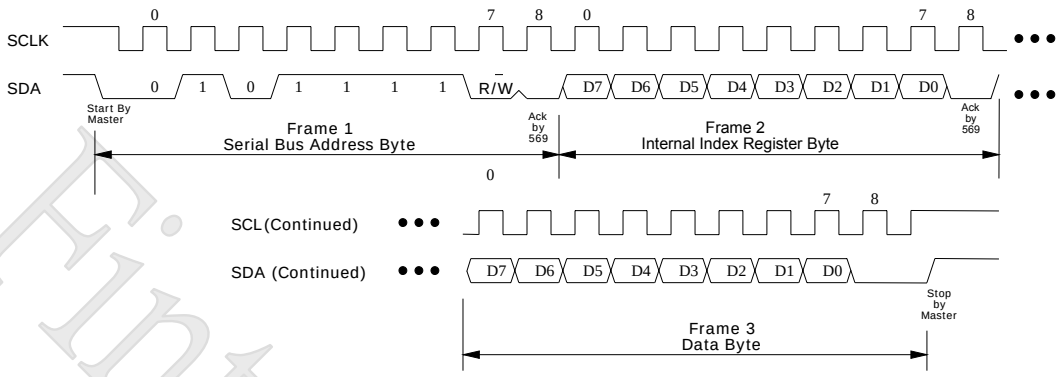


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

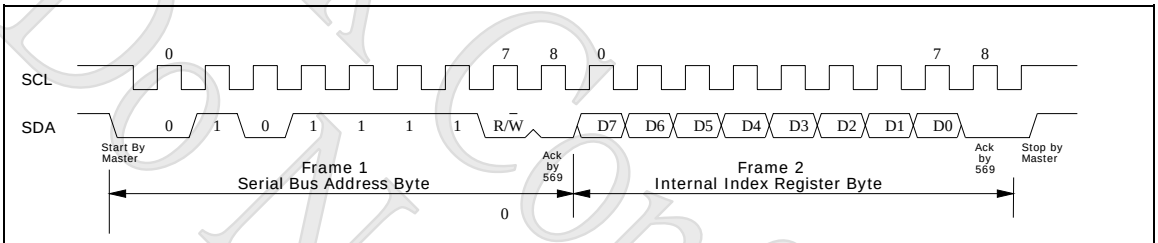


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

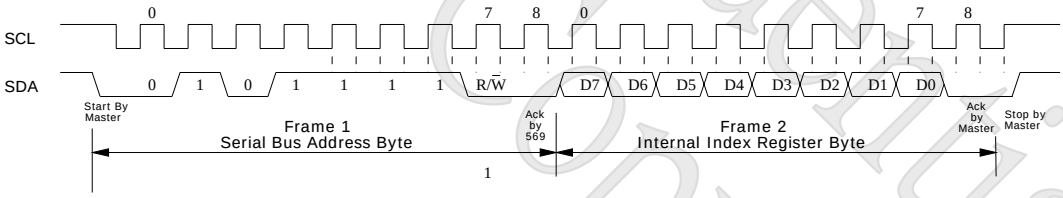


Figure 3. Serial Bus Read from Internal Address Register

9 Register Description

9.1 Register — Index 01h

Reserved register. Do not write the reserved register to avoid the mis-action, please.

9.2 PWM_VRAM_11, PWM_VRAM_10 Fine Tune Voltage Register — Index 02h

Bit	Name	R/W	Default	Description
7:4	PWMVRAM_11	R/W	3	According to Turbo hardware pin setting, to fine tune PWM_VRAM reference voltage. If Turbo = 1, the PWM_VRAM Voltage table is set by Register 02h bit 7:4. 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3
3:0	PWMVRAM_10	R/W	3	According to Turbo hardware pin setting to fine tune PWM_VRAM reference voltage. If Turbo = 0, the PWM_VRAM Voltage table is set by Register 02h bit 3:0. 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3

9.3 Register — Index 03h

Reserved register. Do not write the reserved register to avoid the mis-action, please.

9.4 PWM_VTT_10, PWM_VTT_11 Fine Tune Voltage Register — Index 04h

Bit	Name	R/W	Default	Description
7:4	PWMVTT_11	R/W	3	According to Turbo hardware pin setting to fine tune PWM_VTT reference voltage. If Turbo = 1, the PWM_VTT Voltage table is set by Register 04h bit 7:4. 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3
3:0	PWMVTT_10	R/W	3	According to Turbo hardware pin setting to fine tune PWM_VTT reference voltage. If Turbo = 0, the PWM_VTT Voltage table is set by Register 04h bit 3:0 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3

9.5 Register — Index 05h

Reserved register. Do not write the reserved register to avoid the mis-action, please.

9.6 LR_VDDA_10, LR_VDDA_11 Fine Tune Voltage Register — Index 06h

Bit	Name	R/W	Default	Description
7:4	LRVDDA_11	R/W	3	According to Turbo hardware pin setting to fine tune LR_VDDA reference voltage. If Turbo = 1, the LR_VDDA Voltage table is set by Register 06h bit 7:4. 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3

3:0	LR_VDDA_10	R/W	3	According to Turbo hardware pin setting to fine tune LR_VDDA reference voltage. If Turbo = 0, the LR_VDDA Voltage table is set by Register 06h bit 3:0 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3

9.7 Register — Index 07h

Reserved register. Do not write the reserved register to avoid the mis-action, please.

9.8 LRVLDT_10, LRVLDT_11 Fine Tune Voltage Register — Index 08h

Bit	Name	R/W	Default	Description
7:4	LRVLDT_11	R/W	3	According to Turbo hardware pin setting to fine tune LRVLDT reference voltage. If Turbo = 1, the LRVLDT Voltage table is set by Register 08h bit 7:4. 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3
3:0	LRVLDT_10	R/W	3	According to Turbo hardware pin setting to fine tune LRVLDT reference voltage. If Turbo = 0, the LRVLDT Voltage table is set by Register 08h bit 3:0 0000 : 0.74V 1000 : 0.90V 0001 : 0.76V 1001 : 0.92V 0010 : 0.78V 1010 : 0.94V 0011 : 0.80V 1011 : 0.96V 0100 : 0.82V 1100 : 0.98V 0101 : 0.84V 1101 : 1.00V 0110 : 0.86V 1110 : 1.02V 0111 : 0.88V 1111 : 1.04V The function must be enable by Register 09 Bit3 and Register 0A bit 3

9.9 LRVDDA, LRVLDT Fine Tune Voltage Register — Index 09h

Bit	Name	R/W	Default	Description
7-6	USBMODE	R/W	1	USB Power mode select, 00:DUAL 01:STR 10:OFF 11:OFF
5	Reserved	R/W	1	Reserved
4	Reserved	R/W	0	Reserved
3	TURBO_EN	R/W	0	TURBO function Enable, if set to 1 the register 01~08h will enable fine tune function when the fine tune setting is Turbo mode (Register 0A bit 3)

2	TURBO_INV	R/W	0	TURBO function sequence inverter. TURBO_INV=0: If TURBO value changes from 0 to 1, it will fine tune directly, Otherwise, it will delay 20ms to fine tune reference voltage. TURBO_INV=1: If TURBO value changes from 1 to 0, it will fine tune directly. Otherwise, it will delay 20ms to fine tune reference voltage
1	Reserved	R/W	0	Reserved
0	FAULT_EN	R/W	0	When register 09H bit 1 is set to FAULT_N mode, Set this bit to 1 to enable FAULT Function, When FAULT_N is low in S0 State, it will Shut down PWM_VRAM, PWM_VTT, LR_PCIE, LR_VID directly,.

9.10 LED ACPI Frequency setting Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-6	PLED_SET[9:8]	R/W	0	PLED frequency setting, When PLED_SET[9:8] set equal to S3_N, S5_N, the PLED pin will be tri-state (OD) *note : {1,1} represent S0 State, {0,1} represent S3 State, {00} represent S5 State, {1,0} the state is reserved
5-4	SLED_SET[9:8]	R/W	3	SLED frequency setting, When SLED_SET[9:8] set equal to S3_N, S5_N, the PLED pin will be tri-state (OD) *note : {1,1} represent S0 State, {0,1} represent S3 State, {00} represent S5 State, {1,0} the state is reserved
3	VFB_SEL	R/W	0	Manual mode or Turbo mode selection, 0:turbo 1:Manual If the setting is Turbo mode, set register 09H bit 3 to enable the fine tune function. If the setting is Manual mode, Write Register 02/04/06/08 Bit [7:4] to fine tune voltage.
2	LED_INV	R/W	1	Set to 1 , the PLED and SLED CLK is inverted
1	VRAM_OCEN	R/W	1	PWM_VRAM Over current enable
0	VTT_OCEN	R/W	1	PWM_VTT Over current enable

9.11 PLED ACPI Frequency setting Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-0	PLED_SET[7:0]	R/W	9B	PLED frequency setting, When the PLED_SET[7:6] = S3_N, S5_N, PLED will be 1HZ toggle pulse with 50 duty cycle PLED_SET[5:4] = S3_N, S5_N, PLED will be 1/2 HZ toggle pulse with 50 duty cycle PLED_SET[3:2] = S3_N, S5_N, PLED will be 1/4HZ toggle pulse with 50 duty cycle PLED_SET[1:0] = S3_N, S5_N, PLED will drive low *note : {1,1} represent S0 State, {0,1} represent S3 State, {00} represent S5 State, {1,0} the state is reserved

9.12 SLED ACPI Frequency setting Register — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	SLED_SET[7:0]	R/W	98	SLED frequency setting, When the SLED_SET[7:6] = S3_N, S5_N, SLED will be 1HZ toggle pulse with 50 duty cycle SLED_SET[5:4] = S3_N, S5_N, SLED will be 1/2 HZ toggle pulse with 50 duty cycle SLED_SET[3:2] = S3_N, S5_N, SLED will be 1/4HZ toggle pulse with 50 duty cycle SLED_SET[1:0] = S3_N, S5_N, SLED will drive low *note : {1,1} represent S0 State, {0,1} represent S3 State, {00} represent S5 State, {1,0} the state is reserved

9.13 Under Voltage, Over Current Enable Protection Register — Index 10h

Bit	Name	R/W	Default	Description
7	VDDA_UVEN	R/W	1	VDDA Under voltage enable
6	VLDT_UVEN	R/W	1	VLDT Under voltage enable
5	VDUAL3V_UVEN	R/W	1	VDUAL3V Under voltage enable
4	LR1_UVEN	R/W	1	LR1 Under voltage enable
3	LR2_UVEN	R/W	1	LR2 Under voltage enable
2	Reserved	R/W	1	Reserved
1	PWM_VTT_UVEN	R/W	1	PWM_VTT Under voltage enable
0	PWM_VRAM_UVEN	R/W	1	PWM_VRAM Under voltage enable

9.14 Register — Index 11h

Bit	Name	R/W	Default	Description
7	DUAL[1:0]	R/W	0	DUAL3V selection 00:3.21V, 01 : 3.3V, 10 :3.38V, 11: 3.456v,
6		R/W	1	
5	Delay[1:0]	R/W	1	V3VOK delay timer, 00: 100ms, 01: 200ms, 10 : 300ms, 11 : 400ms
4		R/W	1	
3	Reserved	R/W	0	Reserved
2	Reserved	R/W	0	Reserved
1	DEC_VFB	R/W	0	Reserved Function: when set to 1, it can decrease regulators VFB voltage, it must fix the related fine tune register bit2, bit 3 to zero, for example 100XX, It provide 4 kinds decrease voltage 10000 : 0.72V 10001 : 0.70V 10010 : 0.68V 10011 : 0.66V
0	PROTECTION_SEL	R/W	0	Set to 1 can toggle S5_N to recovery, if VRAM, VTT, LR_PCIE, LR_VID Shut down by Over current or Under voltage or Fault_N SD , Set to 0, must power off to recovery.

9.15 Register — Index 12h

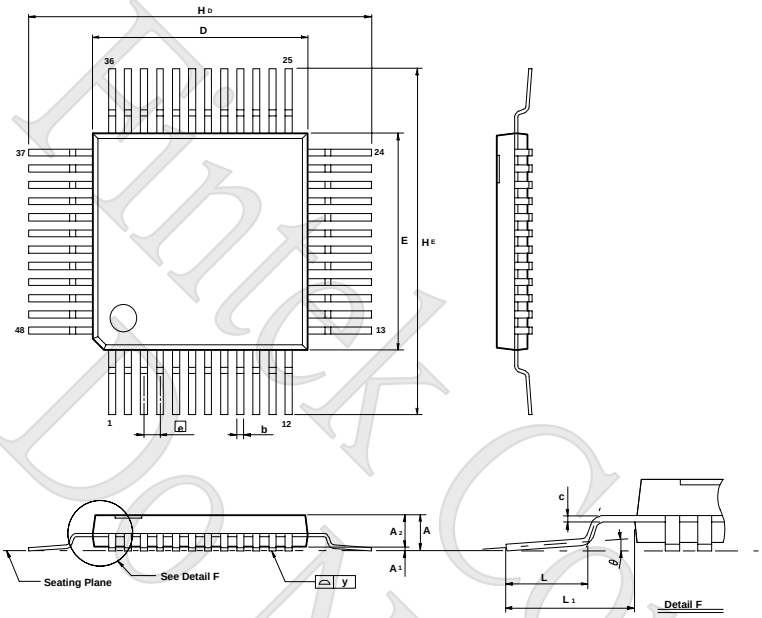
Bit	Name	R/W	Default	Description
7	PROG_PSN_OUT_SET	R/W	0	If Register 12H bit 4 set to 1, write this bit to1 can set PSON_OUT to high.

6	SAME_UV	R/W	1	Set to 1 will Set the VRAM, VDDA, VTT, VLDT Shut down when each power occurs fault event
5	PSON_OUT_UV	R/W	0	Set to 1 will Set the PSON_OUT to high when VRAM, VDDA, VTT, VLDT power fault event occurs
4	SOFT_PSON_OUT	R/W	0	Set to 1 can program PSON_OUT to HIGH
3	Reserved	R/W	0	Reserved
2	Reserved	R/W	0	Reserved
1	Reserved	R/W	0	Reserved
0	Reserved	R/W	0	Reserved

10 Ordering Information

Part Number	Package Type	Production Flow
F72569DG	48-LQFP (Green Package)	Commercial, 0°C to +70°C

11 Package Dimensions (48LQFP)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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12 Application Circuit