# 74LVC245A; 74LVCH245A

## Octal bus transceiver; 3-state

Rev. 05 — 25 August 2009 Product data sheet

## 1. General description

The 74LVC245A; 74LVCH245A are 8-bit transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH245A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{CC}$ = 0 V
- Bushold on all data inputs (74LVCH245A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC245AD | –40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74LVCH245AD | | | | |
| 74LVC245ADB | –40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74LVCH245ADB | | | | |
| 74LVC245APW | –40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74LVCH245APW | | | | |
| 74LVC245ABQ | –40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |
| 74LVCH245ABQ | | | | |
| 74LVC245ABX | –40 °C to +125 °C | DHXQFN20U | plastic dual in-line compatible thermal enhanced extremely thin quad flat package; no leads; 20 terminals; UTLP based; body 2.5 x 4.5 x 0.5 mm | SOT1045-1 |
| 74LVCH245ABX | | | | |

## 4. Functional diagram

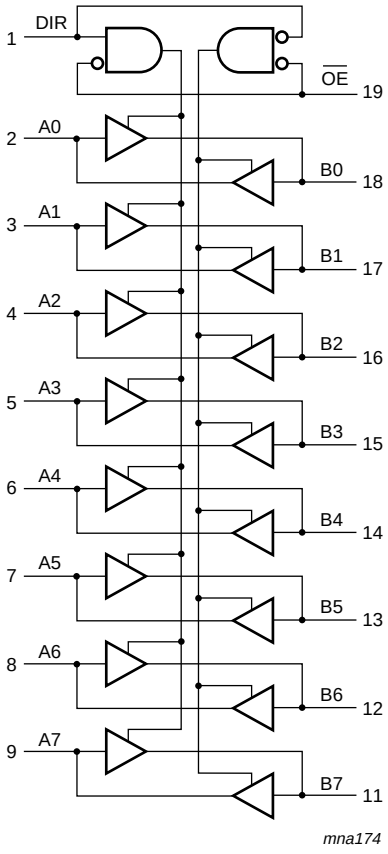



**Fig 1. Logic diagram**

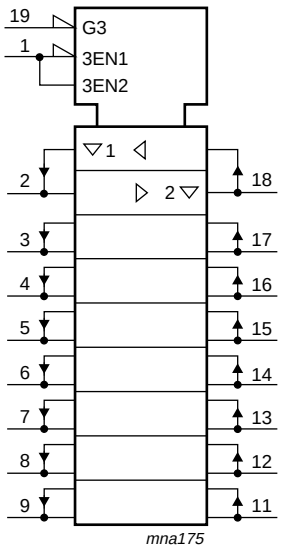



**Fig 2. IEC logic symbol**

# 5. Pinning information

## 5.1 Pinning

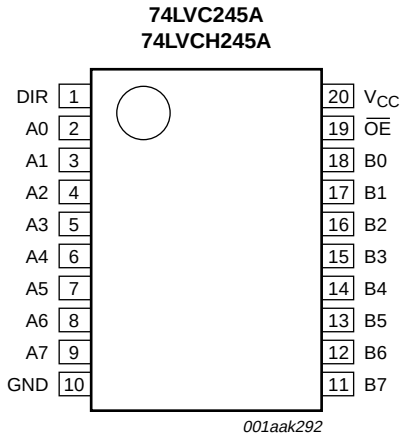
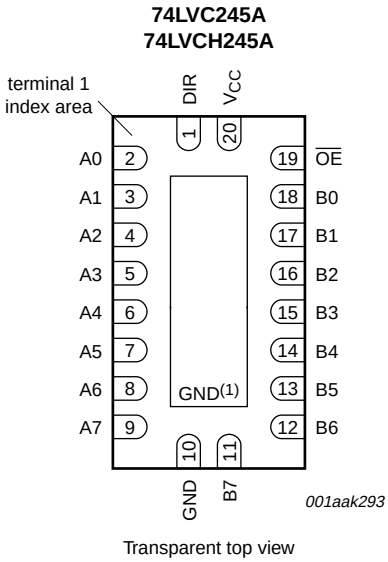



**Fig 3. Pin configuration for SO20 and (T)SSOP20**




Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

**Fig 4. Pin configuration for DHVQFN20 and DHXQFN20U**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| DIR | 1 | direction control |
| A0 to A7 | 2, 3, 4, 5, 6, 7, 8, 9 | data input/output |
| GND | 10 | ground (0 V) |
| B0 to B7 | 18, 17, 16, 15, 14, 13, 12, 11 | data input/output |
| $\overline{OE}$ | 19 | output enable input (active LOW) |
| $V_{CC}$ | 20 | supply voltage |

## 6. Functional description

**Table 3. Function selection[1]**

| Inputs | | Inputs/outputs | |
|---|---|---|---|
| $\overline{OE}$ | DIR | An | Bn |
| L | L | An = Bn | inputs |
| L | H | inputs | Bn = An |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –50 | - | mA |
| $V_I$ | input voltage | | [1] | –0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | output HIGH or LOW | [2] | –0.5 | $V_{CC}$ + 0.5 | V |
| | | output 3-state | [2] | –0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | –100 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C | [3] | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN20 and DHXQFN20U packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | maximum speed performance | 2.7 | - | 3.6 | V |
| | | functional | 1.2 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | output HIGH or LOW | 0 | - | $V_{CC}$ | V |
| | | output 3-state | 0 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.2 V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | $V_{CC}$ | - | - | $V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0 | - | 0 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = –100 µA; $V_{CC}$ = 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | $V_{CC}$ | - | $V_{CC}$ – 0.3 | - | V |
| | | $I_O$ = –12 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | $I_O$ = –18 mA; $V_{CC}$ = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | $I_O$ = –24 mA; $V_{CC}$ = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 2.7 V to 3.6 V | - | 0 | 0.20 | - | 0.3 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.40 | - | 0.6 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 3.6 V [2] | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = 5.5 V or GND; $V_{CC}$ = 3.6 V [2][3] | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 5.5 V; $V_{CC}$ = 0.0 V | - | ±0.1 | ±10 | - | ±20 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 3.6 V | - | 0.1 | 10 | - | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = $V_{CC}$ – 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 2.7 V to 3.6 V | - | 5 | 500 | - | 5000 | µA |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $C_I$ | input capacitance | | | - | 4.0 | - | - | - | pF |
| $C_{I/O}$ | input/output capacitance | | | - | 10 | - | - | - | pF |
| $I_{BHL}$ | bus hold LOW current | $V_{CC}$ = 3.0 V; $V_I$ = 0.8 V | [4][5] | 75 | - | - | 60 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | $V_{CC}$ = 3.0 V; $V_I$ = 2.0 V | [4][5] | –75 | - | - | –60 | - | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_{CC}$ = 3.6 V | [4][6] | 500 | - | - | 500 | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_{CC}$ = 3.6 V | [4][6] | –500 | - | - | –500 | - | µA |

[1] All typical values are measured at $V_{CC}$ = 3.3 V (unless stated otherwise) and $T_{amb}$ = 25 °C.

[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.

[3] For I/O ports the parameter $I_{OZ}$ includes the input leakage current.

[4] Valid for data inputs of bus hold parts only (74LVCH245A). Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified $V_I$ level.

[6] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | An to Bn; see Figure 5 | [1] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 17.0 | - | - | - | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | 3.4 | 7.3 | 1.5 | 9.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 1.5 | 2.9 | 6.3 | 1.5 | 8.0 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to An or Bn; see Figure 6 | [1] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 22.0 | - | - | - | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | 5.0 | 9.5 | 1.5 | 12.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 1.5 | 4.0 | 8.5 | 1.5 | 11.0 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to An or Bn; see Figure 6 | [1] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 12.0 | - | - | - | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | 3.6 | 8.0 | 1.5 | 10.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 1.7 | 3.4 | 7.0 | 1.7 | 9.0 | ns |
| $t_{sk(o)}$ | output skew time | | [4] | - | - | 1.0 | - | 1.5 | ns |

**Table 7. Dynamic characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | Min | Max | |
| $C_{PD}$ | power dissipation capacitance | per buffer; $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.3 V [5] | - | 15 | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

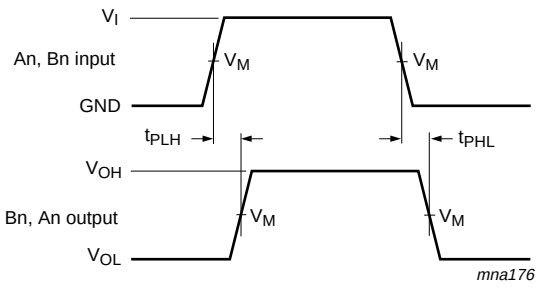
[2] Typical values are measured at $T_{amb}$ = 25 °C.

[3] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 3.3 V.

[4] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

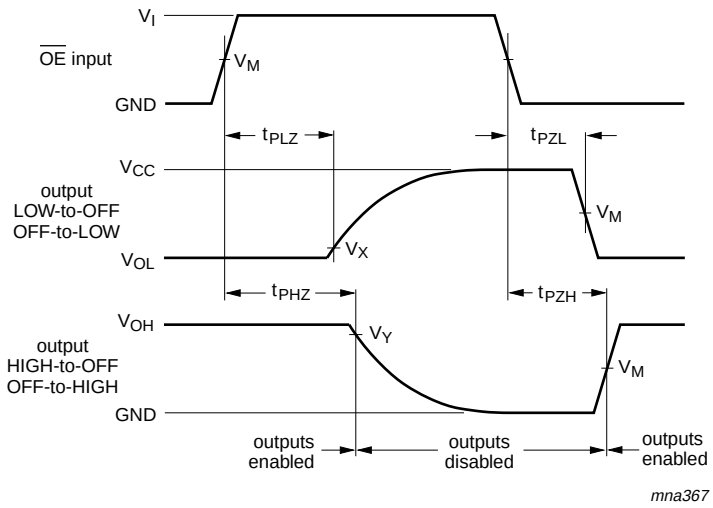
## 11. AC waveforms




See Table 8 for measurement points

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 5. Input (An, Bn) to output (Bn, An) propagation delays and output transition times**



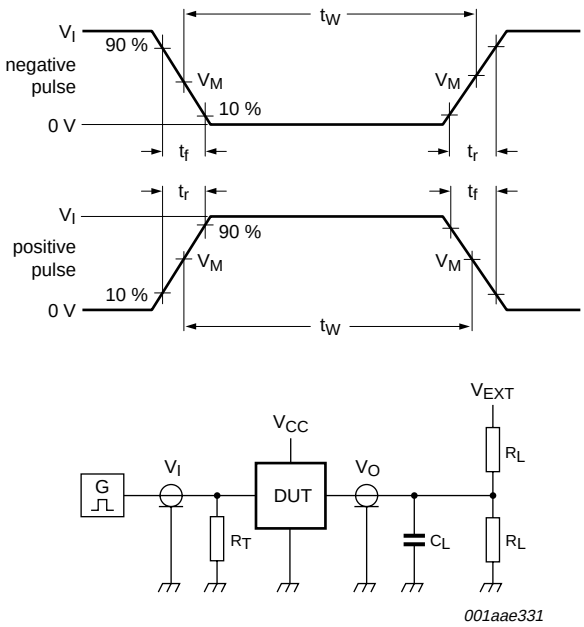

See Table 8 for measurement points

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 6. Enable and disable times**

**Table 8. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.2 V | $V_{CC}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.1 V | $V_{OH}$ − 0.1 V |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 9.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 7. Test circuit for measuring switching times**

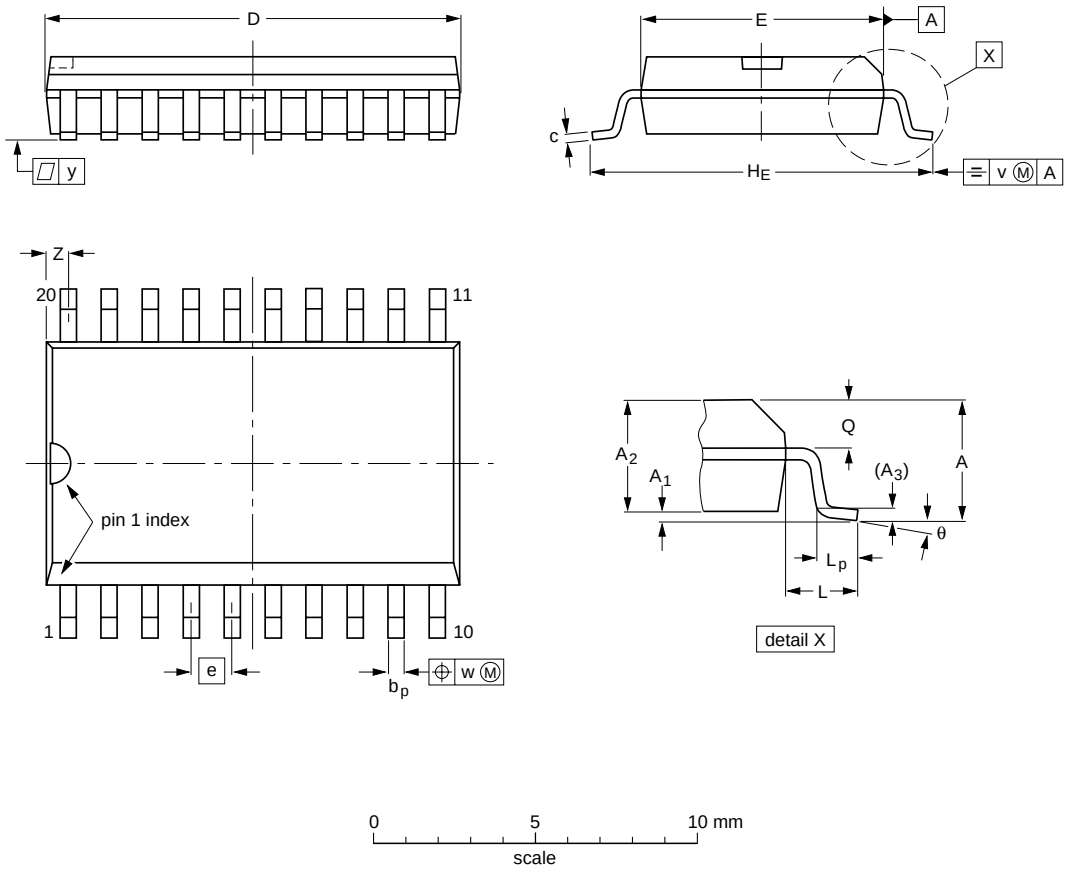
**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 1.2 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω[1] | open | $2 \times V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

[1] The circuit performs better when $R_L$ = 1 kΩ.

## 12. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

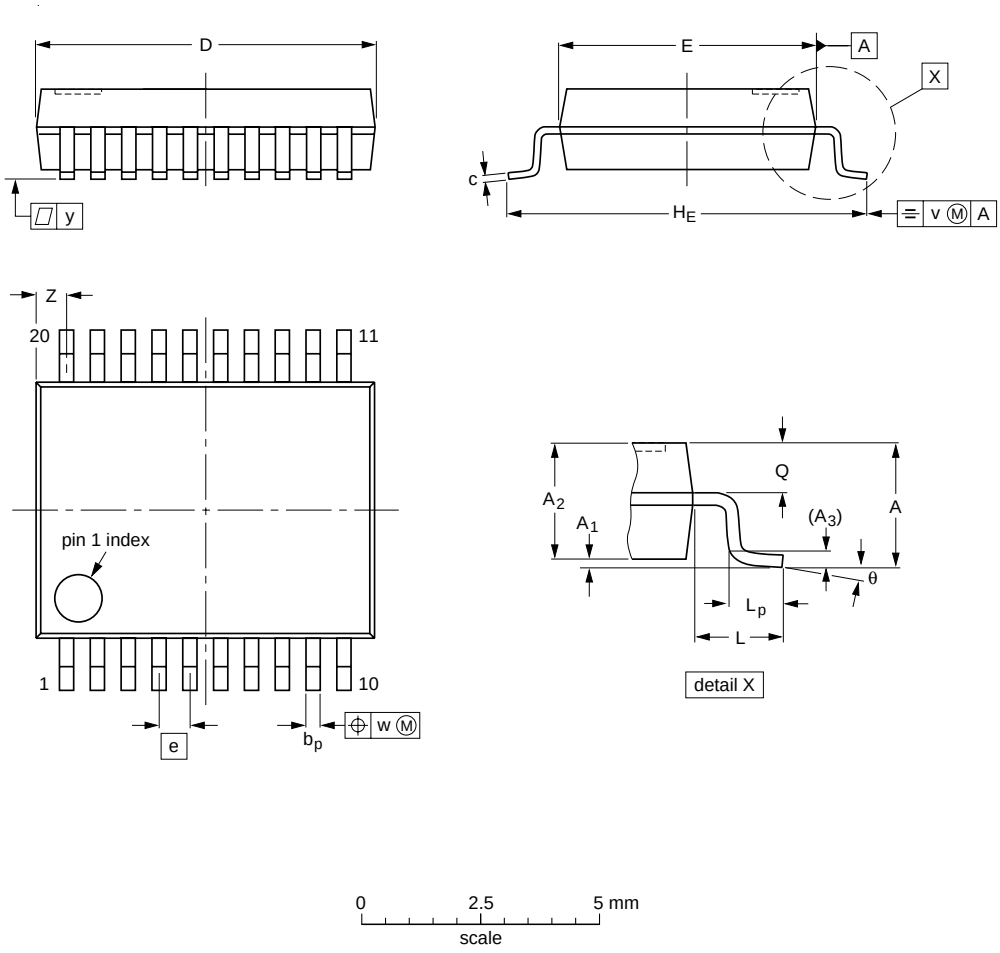
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT163-1 (SO20)**

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm** **SOT339-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 7.4<br>7.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.9<br>0.5 | $8^o$<br>$0^o$ |

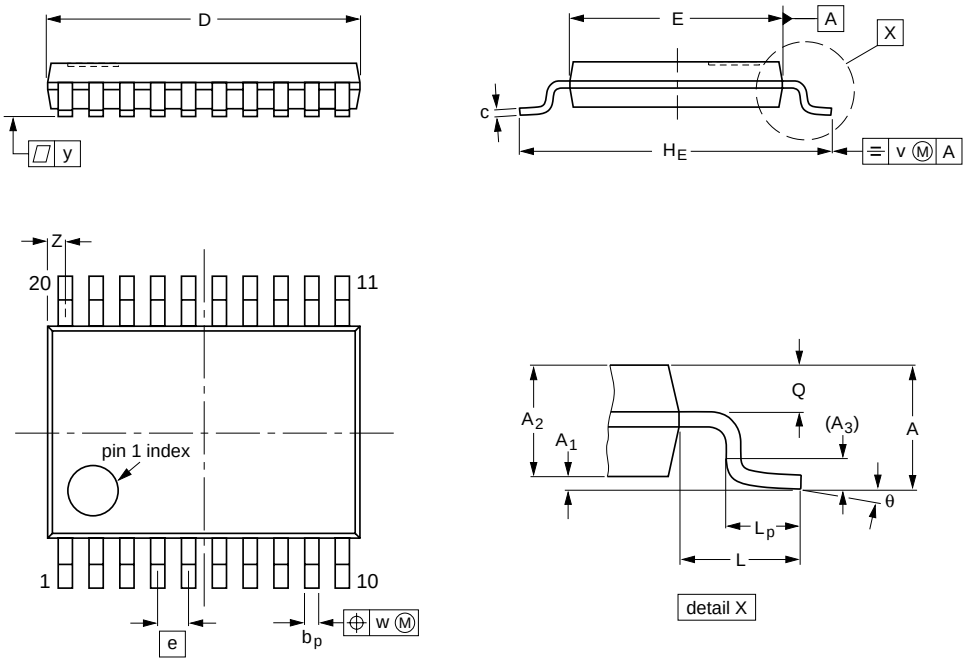
**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT339-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT339-1 (SSOP20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | $8^o$<br>$0^o$ |

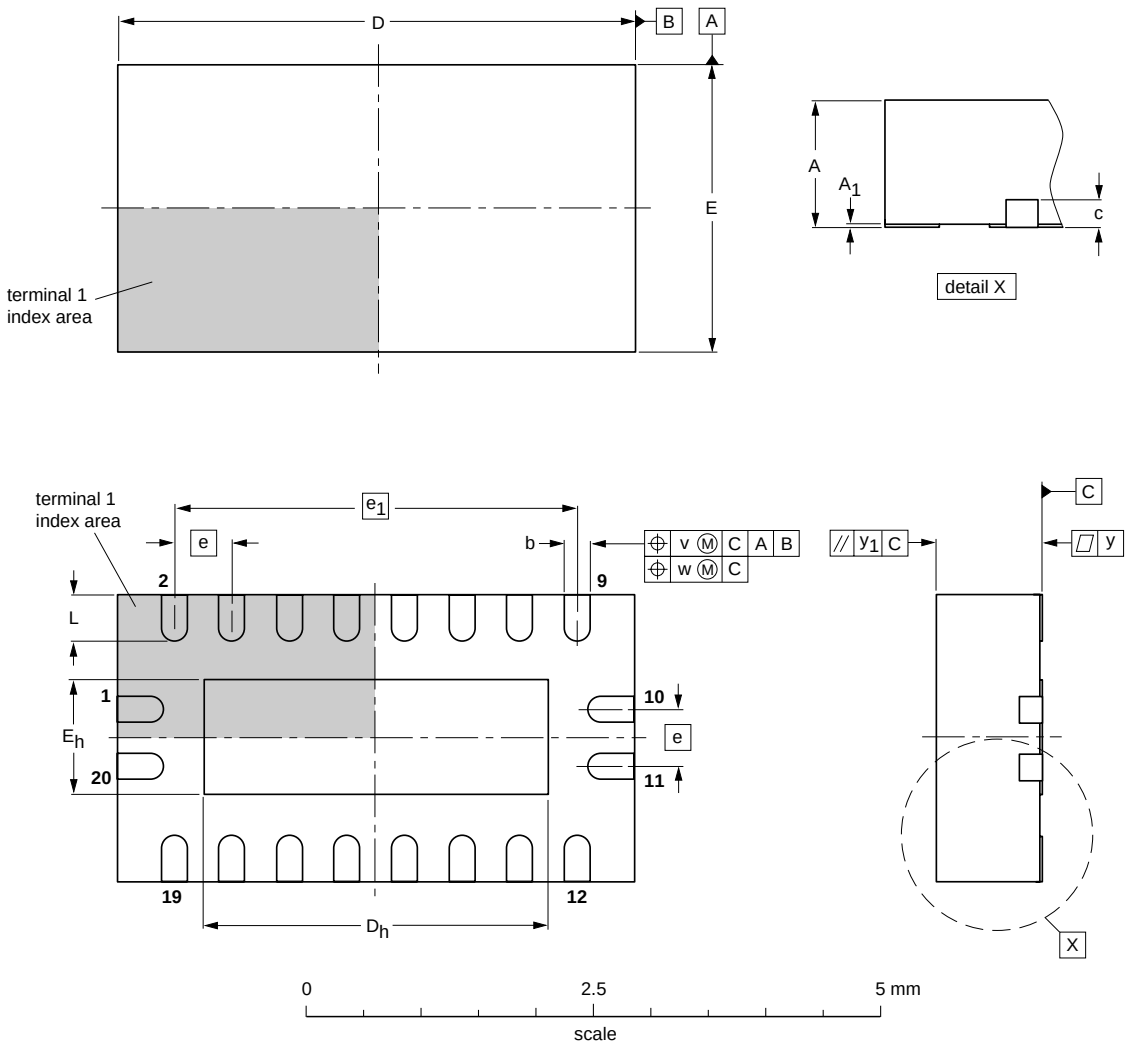
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT360-1 (TSSOP20)**

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm** **SOT764-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 4.6<br>4.4 | 3.15<br>2.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 3.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

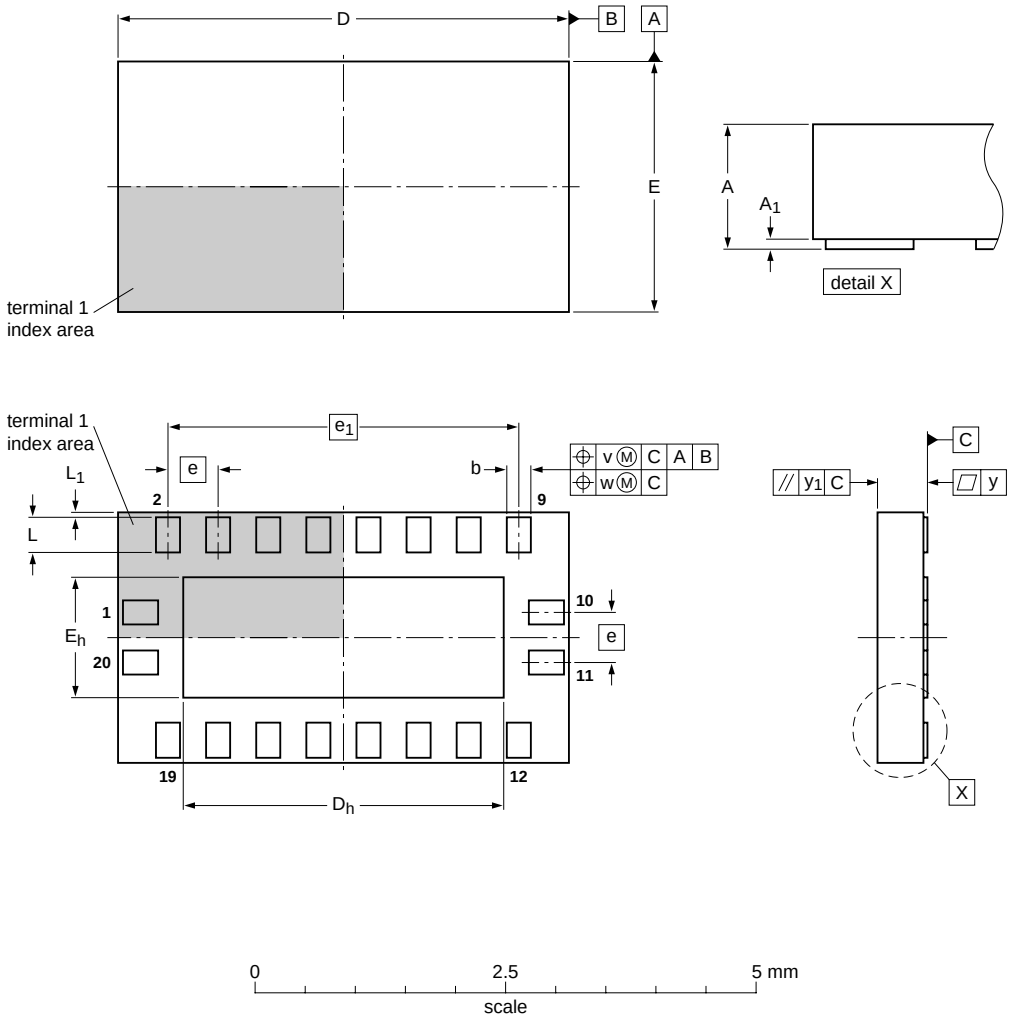
**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT764-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 11. Package outline SOT764-1 (DHVQFN20)**

**DHXQFN20U: plastic dual in-line compatible thermal enhanced extremely thin quad flat package; no leads; 20 terminals; UTLP based; body 2.5 x 4.5 x 0.5 mm** **SOT1045-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | b | D | $D_h$ | E | $E_h$ | e | $e_1$ | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.05<br>0.00 | 0.30<br>0.18 | 4.6<br>4.4 | 3.35<br>3.05 | 2.6<br>2.4 | 1.35<br>1.05 | 0.5 | 3.5 | 0.45<br>0.25 | 0.13<br>0.05 | 0.1 | 0.05 | 0.05 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1045-1 | - - - | | - - - | | | ~~07-12-01~~<br>09-08-04 |

**Fig 12. Package outline SOT1045-1 (DHXQFN20U)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC_LVCH245A_5 | 20090825 | Product data sheet | - | 74LVC_LVCH245A_4 |
| Modifications: | • New SOT1045-1 package outline drawing (DHXQFN20U package). | | | |
| 74LVC_LVCH245A_4 | 20090703 | Product data sheet | - | 74LVC_LVCH245A_3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Added type number 74LVC245ABX and 74LVCH245ABX (DHXQFN20U package) | | | |
| 74LVC_LVCH245A_3 | 20030507 | Product specification | - | 74LVC245A_74LVCH245A_2 |
| 74LVC245A_74LVCH245A_2 | 20020620 | Product specification | - | 74LVC245A_74LVCH245A_1 |
| 74LVC245A_74LVCH245A_1 | 19971219 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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**Date of release: 25 August 2009**

**Document identifier: 74LVC_LVCH245A_5**