

eorex

64MB/128MB/256MB/512MB MultiMediaCard™

Description

ESMMC64 / ESMMC128 / ESMMC256 / ESMMC512 are 64MB up to 512MB MultiMediaCard™. These are the highly integrated flash memory with serial and random accessible via a dedicated serial interface optimized for fast and reliable data transmission. They are fully compatible to a new consumer standard, called the MultiMediaCard™ system standard defined in the MultiMediaCard™ system specification. The MultiMediaCard™ system is a new mass-storage system based on innovations in semiconductor technology. It has been designed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications and mobile devices (handheld PCs, digital cameras, MP3 players, etc.) to store, copy, and move information like a small hard drive.

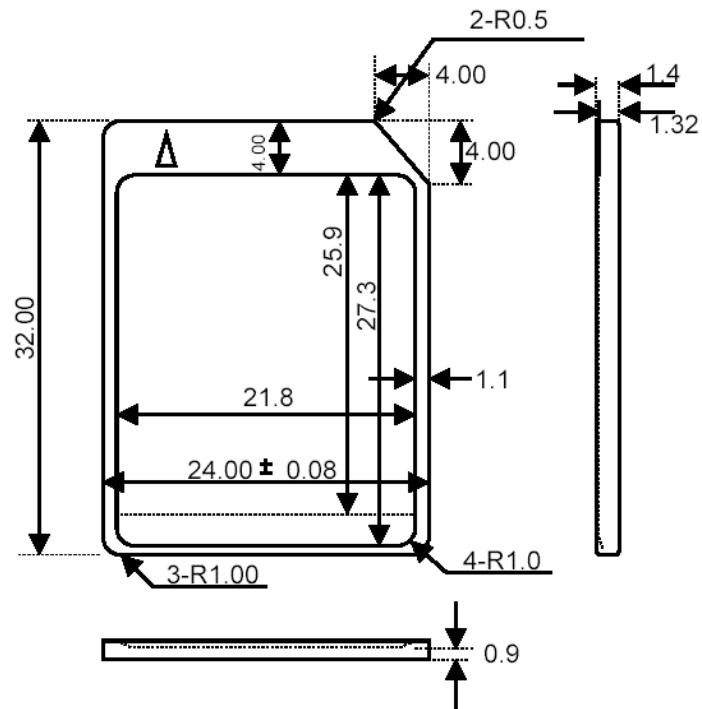
Features

- Operating Voltage: 2.7V ~ 3.6V
- Password data access protection
- Small erase block size of 512 bytes, tagged erase supported.
- Read block size programmable between 1 and 2048 bytes
- Damage free powered card insertion and removal
- 4KV ESD protection
- Read speed
 - Sustained: 13.7Mbits/s
 - Burst(one block): 20Mbit/s
- Write speed
 - Sustained: 2.8Mbits/s
 - Burst(one block): 20Mbit/s
- Up to 10 stacked card (at 20MHz, Vcc = 2.7V to 3.6V)
- Access time: 300μs
- Low power dissipation

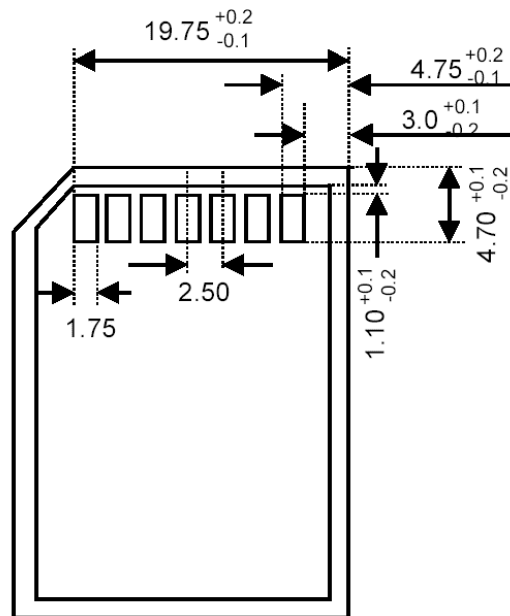
Pin Definition

Pin No.	Name	Type	Description
1	RSV	NC	No connection
2	CMD	I/O/PP/OD	Command/Response
3	VSS1	S	Ground
4	VCC	S	Power Supply
5	CLK	I	Clock
6	VSS2	S	Ground
7	DAT	I/O/PP	Data

Physical Outline

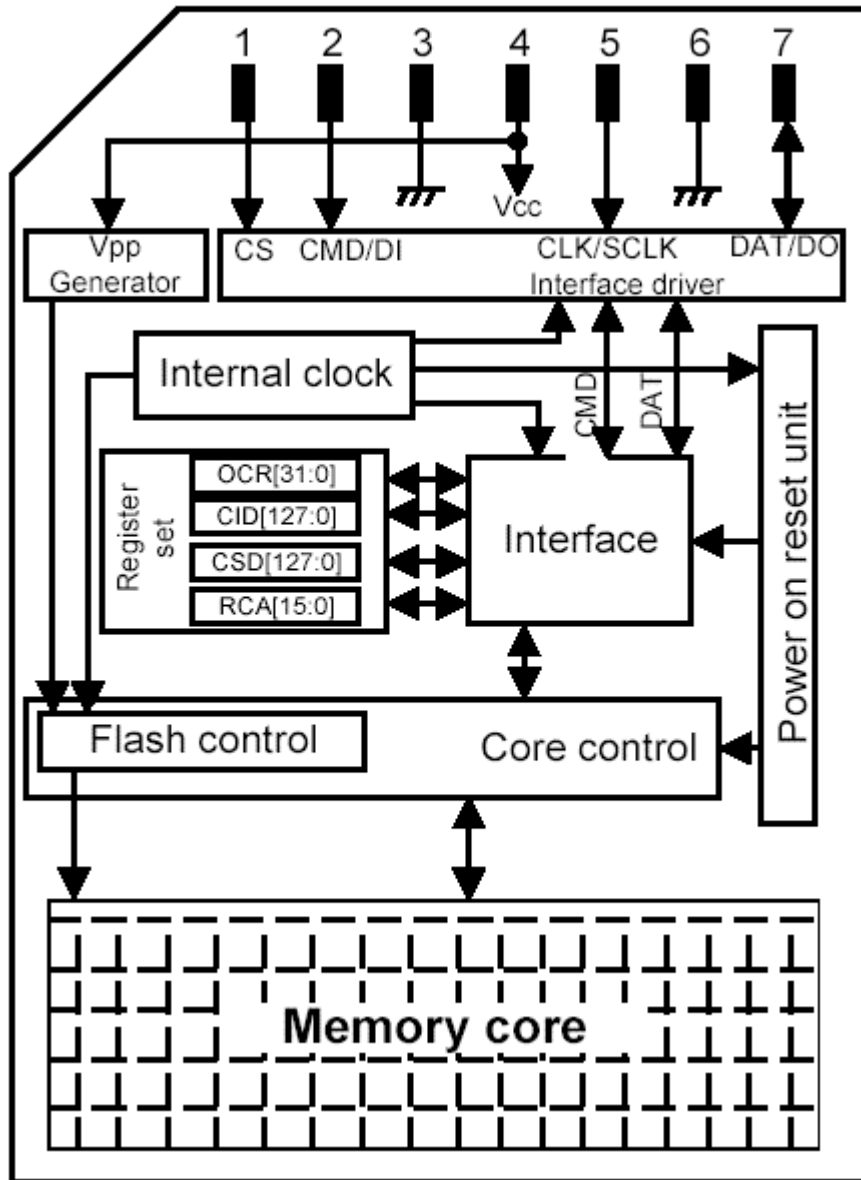


Front



Back

Architecture



Temperature Characteristic

Parameter	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-25	85	°C
Junction temperature	-20	95	°C

Electrical Characteristics

1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	Vcc	-0.5	4.6	V	
Total power dissipation			0.2	W	
ESD protection		-4	4	KV	Human body model
Input voltage	VImax	-0.5	Vcc+0.5	V	≤ max(Vcc)
Output voltage	VOmax	-0.5	Vcc+0.5	V	≤ max(Vcc)
High-level output current	VOHmax	-100		mA	Short cut protected
Low-level output current	IOHmax		150	mA	Short cut protected

2. Bus Signal Line Load

The total capacitance CL of each line of the MultiMediaCard™ bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line:

$$CL = CHOST + CBUS + N * CCARD$$

Where N is the number of connected cards. Requiring the sum of the host and bus capacitance's not to exceed 30pF for up to 10 cards, and 40pF up to 30 cards, the following values must not be exceeded:

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7	100	KΩ	To prevent bus floating
Pull-up resistance for DAT	RDAT	50	100	KΩ	To prevent bus floating
Bus signal line capacitance	CL		250	pF	fpp ≤ 5MHz, 30 cards
Bus signal line capacitance	CL		100	pF	fpp ≤ 20MHz, 10 cards
Signal card capacitance	CCARD		7	pF	
Maximum signal line inductance			16	nH	fpp ≤ 20MHz

3. Recommend Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit	Remark
Supply voltage		VCC	2.7	3.0	3.6	V	
Inputs	Low-level input current	VIL	VSS-0.3		0.25VCC	V	
	High-level input current	VIH	0.625VCC		VCC+0.3	V	
Outputs	High-level output current	IOH	-2			mA	
	Low-level output current	IOL			6	mA	
Clock	Clock frequency data transfer mode (pp)	fpp	0		20	MHz	CL<100pF,(10 cards)
Input clk	Clock frequency ident. Mode (od)	fOD	0		400	KHz	
	Clock cycle time data transfer mode (pp)	Tpp = 1/fpp	50			ns	
	Clock cycle time ident. Mode (od)	tOD = 1/fOD	2.5			μs	
	Clock low time	tWL	10			ns	CL<100pF,(10 cards)
	Clock high time	tWH	10			ns	CL<100pF,(10 cards)
	Clock input rise time	tLH			10	ns	CL<100pF,(10 cards)
	Clock input fall time	tHL			10	ns	CL<100pF,(10 cards)
	Clock low time	tWL	50			ns	CL<250pF,(30 cards)
	Clock high time	tWH	50			ns	CL<250pF,(30 cards)
	Clock input rise time	tLH			50	ns	CL<250pF,(30 cards)
	Clock input fall time	tHL			50	ns	CL<250pF,(30 cards)

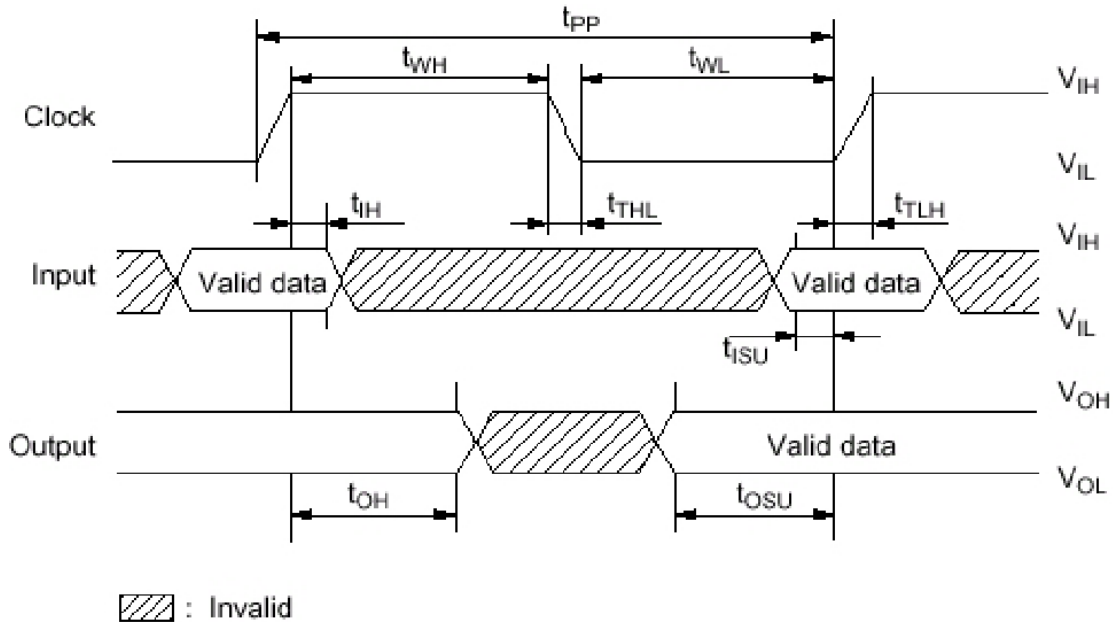
4. Recommend Bus Conditions

Parameter		Symbol	Min	Typ	Max	Unit	Remark
Clock	Pull-up resistance for CMD	RCMD	4.7		100	KΩ	To prevent bus floating
Input clk	Pull-up resistance for DAT	RDAT	50		100	KΩ	To prevent bus floating
	Bus signal line capacitance	CL			250	pF	fpp ≤ 5MHz, 30 cards
					100	pF	fpp ≤ 20MHz, 10 cards
Maximum signal line inductance				16	nH	fpp ≤ 20MHz	

5. Operating Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Remark
High speed supply current					45	mA	At 20MHz, 3.6V
Minimal supply current					150	μA	At 0Hz, 3.6V standby state
All digital inputs (including I/O current)	Input leakage current		-10		10	μA	
All outputs	High-level output voltage	VOH	0.75VCC			V	At min IOH
	Low-level output voltage	VOL			0.125VCC	V	At max IOL
Inputs: CMD, DAT(Referred to CLK), DI(Referred to SCLK), CS	Input set-up time	tISU	3			ns	
	Input hold time	VOL	3			ns	
Outputs: CMD, DAT(Referred to CLK), DO(Referred to SCLK)	Output set-up time	tOSU	5			ns	
	Output hold time	tOH	5			ns	At tLH = 10ns

Timing Diagram of Data Input and Output



The access time (t_{AT}) is divided into two parts:

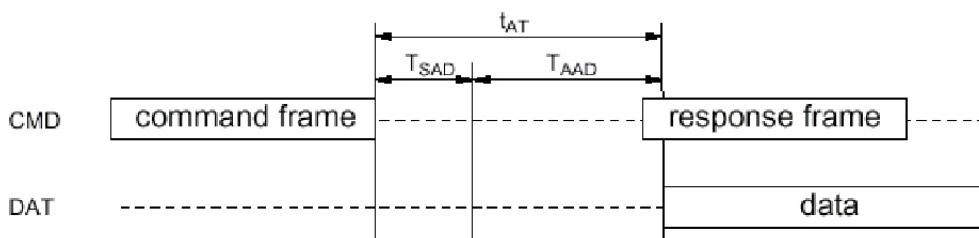
T_{SAD} : The synchronous access time. This time defines the time of the maximum number of cycles which are required to access a byte of the memory field.

T_{AAD} : The asynchronous access time to read a byte out of the memory field.

The synchronous part of the access time is sum of the command frame length and some additional internal cycles ($N_{SAD} = 16$ cycles). At 20MHz one cycle is 50ns ($1/f_{CLK}$), multiplied with N_{SAD} the resulting frame time is $T_{SAD} = 0.8\mu s$. The asynchronous access delay $T_{AAD} = 600\mu s$ maximum.

The resulting memory access time t_{AT} is the sum of both parts:

$$t_{AT} = T_{SAD} + T_{AAD} \quad \text{with } T_{SAD} = N_{SAD} / f_{CLK}$$





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Access Time

Parameter	Symbol	Typ	Max	Unit	Remark
Synchronous access delay cycles	N_{SAD}		16	cycles	
Synchronous access delay	T_{SAD}		0.8	μs	At 20MHz clock frequency
Asynchronous access delay	T_{AAD}	600		μs	
Memory access time	T_{AT}	600.8		μs	At 20MHz clock frequency

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