

HT1620

RAM Mapping 32×4 LCD Controller for I/O MCU

PATENTED PAT No. : 099352

Technical Document

- FAQs
- Application Note

Features

- Logic operating voltage: 2.4V~3.3V
- LCD voltage: 3.6V~4.9V
- Low operating current <3µA at 3V
- External 32.768kHz crystal oscillator
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Built-in capacitor type bias charge pump
- Time base or WDT overflow output

- 8 kinds of time base/WDT clock source
- 32×4 LCD driver
- Built-in 32×4-bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- R/Wy address auto increment
- Data mode and command mode instructions
- Three data accessing modes
- HT1620: 64pin LQFP package HT1620G: Gold bumped chip

General Description

The HT1620 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the HT1620 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the in-

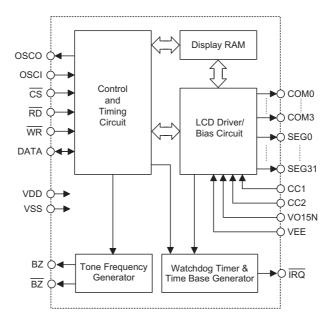
terface between the host controller and the HT1620. The HT1620 consumes low operating current owing to adopting capacitor type bias charge pump. The HT162X series have many kinds of products that match various applications.

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626
СОМ	4	4	8	8	8	8	16
SEG	32	32	32	32	48	64	48
Built-in Osc.	_	\checkmark	\checkmark			\checkmark	\checkmark
Crystal Osc.	√	\checkmark		\checkmark		\checkmark	\checkmark

Selection Table



Block Diagram



Note: CS: Chip selection

BZ, BZ: Tone outputs

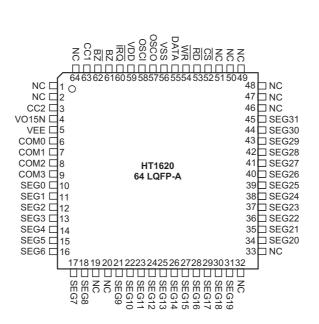
WR, RD, DATA: Serial interface

COM0~COM3, SEG0~SEG31: LCD outputs

IRQ: Time base or WDT overflow output VO15N: Half voltage circuit output pin VEE: Double voltage circuit output pin

CC1/CC2: External capacitor pin, for double voltage and half voltage circuit use

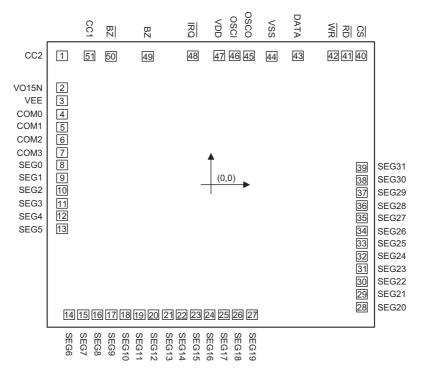
Pin Assignment





HT1620

Pad Assignment



Chip size: $92 \times 89 \text{ (mil)}^2$ Bump height: $18\mu\text{m} \pm 3\mu\text{m}$ Min. Bump spacing: $23.102\mu\text{m}$

Bump size: $76 \times 76 \mu m^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.



HT1620

Pad Coordinates

Pad Coordinat	tes				Unit: μm
Pad No.	Х	Y	Pad No.	Х	Y
1	-1047.550	1003.190	27	288.954	-1017.875
2	-1047.675	751.820	28	1066.345	-956.690
3	-1047.589	653.370	29	1066.345	-857.591
4	-1047.675	546.716	30	1066.345	-758.569
5	-1047.675	447.615	31	1066.345	-659.470
6	-1047.675	348.594	32	1066.345	-560.449
7	-1047.675	249.495	33	1066.345	-461.351
8	-1047.675	150.475	34	1066.345	-362.330
9	-1047.675	51.375	35	1066.345	-263.230
10	-1047.675	-47.646	36	1066.345	-164.210
11	-1047.675	-146.745	37	1066.345	-65.110
12	-1047.675	-245.766	38	1066.345	33.910
13	-1047.675	-344.865	39	1066.345	133.010
14	-998.865	-1017.875	40	1061.255	1003.190
15	-899.766	-1017.875	41	962.234	1003.190
16	-800.745	-1017.875	42	863.135	1003.190
17	-701.646	-1017.875	43	612.943	1003.190
18	-602.625	-1017.875	44	430.677	999.625
19	-503.526	-1017.875	45	267.974	1003.190
20	-404.505	-1017.875	46	168.952	1003.190
21	-305.406	-1017.875	47	59.692	1003.715
22	-206.385	-1017.875	48	-126.910	1003.190
23	-107.285	-1017.875	49	-445.130	999.100
24	-8.264	-1017.875	50	-704.419	999.100
25	90.835	-1017.875	51	-855.819	1003.190
26	189.855	-1017.875			



Pad Description

Pad No.	Pad Name	I/O	Description	
51, 1	CC1, CC2	I	External capacitor pin, for double voltage and half voltage circuit use	
2	VO15N	0	Half voltage circuit output pin	
3	VEE	_	Double voltage circuit output pin	
4~7	COM0~COM3	0	LCD common outputs	
8~39	SEG0~SEG31	0	LCD segment outputs	
40	cs	I	Chip selection input with pull-high resistor. When the \overline{CS} is logic high, the data and command, read from or written to the HT1620 are disabled. The serial interface circuit is also reset. But if the \overline{CS} is at logic low level and is input to the \overline{CS} pad, the data and command transmission between the host controller and the HT1620 are all enabled.	
41	RD	I	READ clock input with pull-high resistor. Data in the RAM of the HT1620 are clocked out on the falling edge of the $\overline{\text{RD}}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next raising edge to latch the clocked out data.	
42	WR	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1620 on the rising edge of the $\overline{\rm WR}$ signal.	
43	DATA	I/O	Serial data input/output with pull-high resistor	
44	VSS	_	Negative power supply, Ground	
45	OSCO	0	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to	
46	OSCI	I	generate a system clock.	
47	VDD	_	Positive power supply	
48	ĪRQ	0	Time base or WDT overflow flag, NMOS open drain output	
49, 50	BZ, BZ	0	2kHz or 4kHz tone frequency output pair (tri-state output buffer)	

Absolute Maximum Ratings

Supply VoltageV_SS=0.3V to V_SS+3.6V	Storage Temperature50°C to 125°C
Input VoltageV_SS=0.3V to V_DD+0.3V	Operating Temperature25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

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D.C. Characteristics

Council of	Demonster		Test Conditions	Min	Turn	Maria	Unit
Symbol	Parameter	V _{DD}	Conditions	Min.	Тур.	Max.	
V _{DD}	Operating Voltage	_		2.4	_	3.3	V
I _{DD}	Operating Current	3V	See note 1	_	2	3	μA
I _{STB}	Standby Current	3V	See note 2	_	_	1	μA
VIL	Input Low Voltage	3V	DATA, WR, CS, RD		_	0.6	V
VIH	Input High Voltage	3V	DATA, WR, CS, RD	2.4		3.0	V
I _{OL1}	DATA, BZ, BZ, IRQ	3V	V _{OL} =0.3V	0.8	1.6		mA
I _{OH1}	DATA, BZ, BZ	3V	V _{OH} =2.7V	-0.6	-1.2		mA
I _{OL2}	LCD Common Sink Current	3V	V _{OL} =0.3V	80	150	_	μA
I _{OH2}	LCD Common Source Current	3V	V _{OH} =2.7V	-70	-120		μA
I _{OL3}	LCD Segment Sink Current	3V	V _{OL} =0.3V	70	140		μA
I _{OH3}	LCD Segment Source Current	3V	V _{OH} =2.7V	-30	-60	_	μA
R _{PH}	Pull-high Resister	3V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	100	200	300	kΩ

Note: 1. No load, Buzzer Off, LCD On, system enable and $\overline{CS}=\overline{WR}=\overline{RD}=High$ 2. No load, Buzzer Off, LCD Off, system disable and $\overline{CS}=\overline{WR}=\overline{RD}=High$

A.C. Characteristics

Test Conditions Symbol Parameter Min. Тур. Max. Unit Conditions V_{DD} System Clock 3V Crystal 32kHz 32768 Hz f_{SYS} ____ LCD Frame Frequency ____ 64 Hz ____ LCD Frame Frequency 1/2 Duty 64 Ηz ____ ____ ____ fLCD Crystal 32kHz LCD Frame Frequency 1/3 Duty 56 Hz ____ ____ ____ LCD Frame Frequency 1/4 Duty 64 Ηz ____ ____ ____ LCD Common Period n: Number of COM t_{COM} ____ n/f_{LCD} s ____ Write mode 4 150 kHz ____ Serial Data Clock 3V f_{CLK} Read mode 75 kHz ____ Tone Frequency (2kHz) 2.0 kHz **f**TONE 3V Crystal 32kHz Tone Frequency (4kHz) 4.0 kHz ____ ____ Serial Interface Reset Pulse CS tcs 500 600 ns Width (Figure 3) Write mode 3.34 125 WR, RD Input Pulse Width ____ t_{CLK} 3V μS (Figure 1) Read mode 6.67 ____ **Rise/Fall Time Serial Data Clock** t_r, t_f 3V 120 160 ns ____ Width (Figure 1) Setup Time for DATA to WR, RD 3V 60 120 t_{SU} ns ____ Clock Width (Figure 2) Hold Time for DATA to \overline{WR} , \overline{RD} 3V 500 600 t_H ns ____ Clock Width (Figure 2)

Ta=25°C

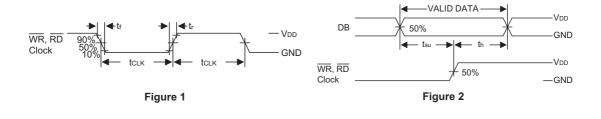
Ta=25°C

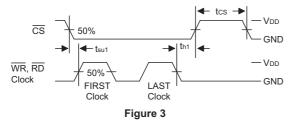


Symbol	Parameter		Test Conditions	Min.	Тур.	Max.	Unit
Symbol	Farameter	V _{DD}	Conditions				
t _{SU1}	Setup Time for $\overline{\text{CS}}$ to $\overline{\text{WR}}, \overline{\text{RD}}$ Clock Width (Figure 3)	3V		500	600	_	ns
t _{H1}	Hold Time for $\overline{\text{CS}}$ to $\overline{\text{WR}}$, $\overline{\text{RD}}$ Clock Width (Figure 3)	3V		50	100		ns
t _{OFF}	V _{DD} OFF Times (Figure 4)	_	VDD drop down to 0V	20	_	_	ms
t _{SR}	V _{DD} Rising Slew Rate (Figure 4)	_		0.05	_	_	V/ms

Note: 1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.

2. If the VDD drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the VDD must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.





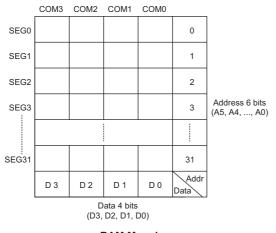




Functional Description

Display Memory – RAM structure

The static display RAM is organized into 32×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MOD IFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.



Time Base and Watchdog Timer - WDT

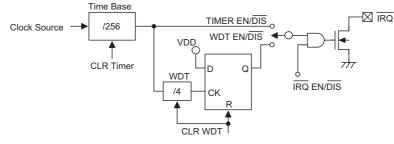
The time base generator and WDT share the same divided (\div 256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and \overline{IRQ} EN/DIS are independent from each other. Once the WDT time-out occurs, the \overline{IRQ} pin will stay at a logic low level until the CLR WDT or the \overline{IRQ} DIS command is issued.

Buzzer Tone Output

A simple tone generator is implemented in the HT1620. The tone generator can output a pair of differential driving signals on the BZ and $\overline{\text{BZ}}$ which are used to generate a single tone.

LCD Driver

The HT1620 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1620 suitable for multiple LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency. The LCD corresponding commands are summarized in the table.



Timer and WDT Configurations

Name	Command Code	Function
LCD OFF	100 0000010X	Turn off LCD outputs
LCD ON	100 0000011X	Turn on LCD outputs
BIAS and COM	100 0010abXcX	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option



The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID will be omitted, except for the first command. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. With the use of the LCD related commands, the HT1620 can be compatible with most types of LCD panels.

Command Format

The HT1620 can be configured by the S/W setting. There are two mode commands to configure the HT1620 resources and to transfer the LCD display data. The configuration mode of the HT1620 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, **100**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the \overline{CS} pin should be set to "1" and the previous operation mode will be reset also. Once the \overline{CS} pin returns to "0", a new operation mode ID should be issued first.

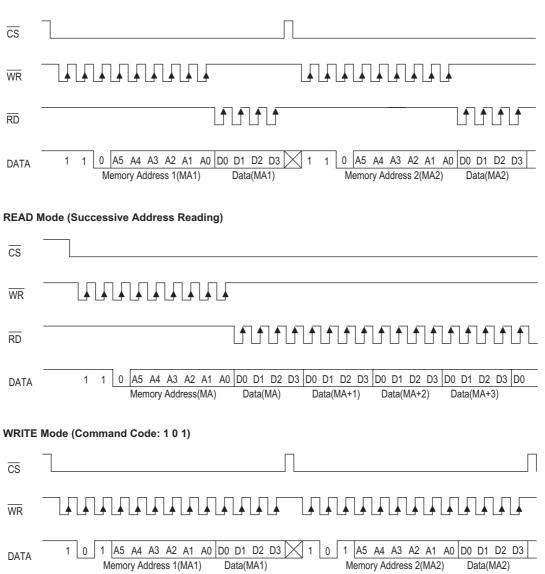
Interfacing

Only four lines are required to interface with the HT1620. The \overline{CS} line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1620. If the \overline{CS} pin is set to 1, the data and command issued between the host controller and the HT1620 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1620. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the RD signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the RD signal. The WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1620 on the rising edge of the WR signal. There is an optional IRQ line to be used as an interface between the host controller and the HT1620. The IRQ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by connecting with the IRQ pin of the HT1620.



Timing Diagrams

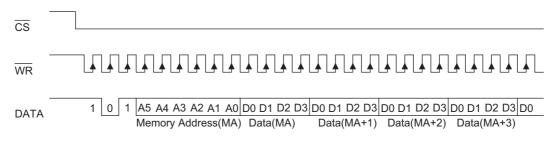
READ Mode (Command Code: 1 1 0)





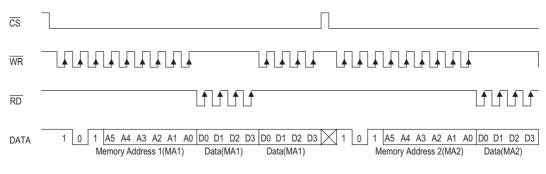
HT1620

WRITE Mode (Successive Address Writing)

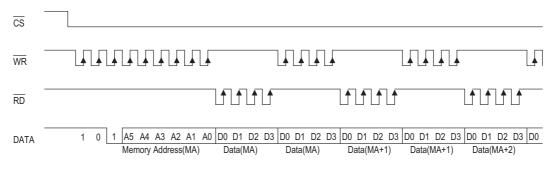


Note: It is recommended that the host controller should read with the data from the DATA line between the raising edge of the $\overline{\text{RD}}$ line and the falling edge of the next $\overline{\text{RD}}$ line.

READ-MODIFY-WRITE Mode (Command Code: 1 0 1)



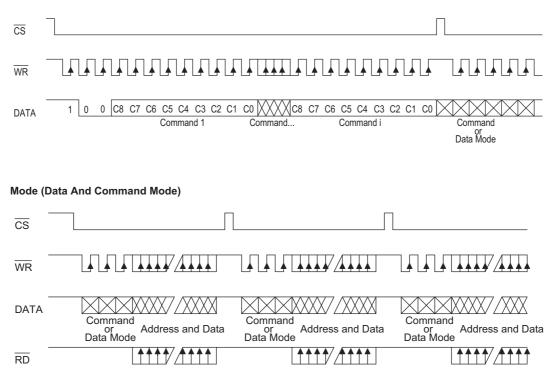
READ-MODIFY-WRITE Mode (Successive Address Accessing)





HT1620

Command Mode (Command Code: 1 0 0)

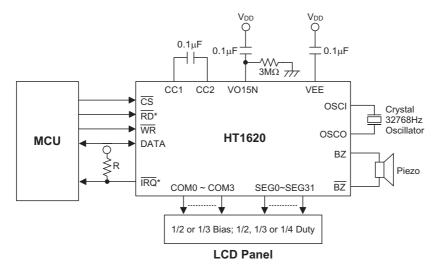






HT1620

Application Circuits



Note: * The connection of the IRQ and RD pin is selectable depending on the requirement of the MCU. V_{DD}=2.4V~3.3V, V_{EE}=-1/2 V_{DD}, V_{LCD} (LCD voltage)=V_{DD}-V_{EE}=3/2 V_{DD}=3.6V~4.9V. Adjust R (external pull-high resistance) to fit user's time base clock.

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ MODIFY WRITE	101	A5A4A3A2A1A0D0D D2D3	D Read and write to the RAM		
SYS DIS	100	0000-0000-X	С	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	100	0000-0001-X	С	Turn on system oscillator	
LCD OFF	100	0000-0010-X	С	Turn off LCD bias generator	Yes
LCD ON	100	0000-0011-X	С	Turn on LCD bias generator	
TIMER DIS	100	0000-0100-X	С	Disable time base output	Yes
WDT DIS	100	0000-0101-X	С	Disable WDT time-out flag output	Yes
TIMER EN	100	0000-0110-X	С	Enable time base output	
WDT EN	100	0000-0111-X	С	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	С	Turn off tone outputs	Yes
CLR TIMER	100	0000-1101-X	с	Clear the contents of the time base generator	
CLR WDT	100	0000-111X-X	С	Clear the contents of the WDT stage	
BIAS 1/2	100	0010-abX0-X	С	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	

Command Summary



Name	ID	Command Code	D/C	Function	Def.
BIAS 1/3	100	0010-abX1-X	с	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	100	010X-XXXX-X	С	Tone frequency, 4kHz	
TONE 2K	100	0110-XXXX-X	С	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	С	Disable IRQ output	Yes
IRQ EN	100	100X-1XXX-X	С	Enable IRQ output	
F1	100	101X-0000-X	С	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	100	101X-0001-X	С	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-0010-X	С	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	100	101X-0011-X	С	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-0100-X	С	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-0101-X	С	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-0110-X	С	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-0111-X	с	Time base clock output: 128Hz The WDT time-out flag after:1/32s	
TEST	100	1110-0000-X	С	Test mode, user don't use.	
NORMAL	100	1110-0011-X	С	Normal mode	Yes

Note: X: Don't care

A5~A0: RAM addresses

D3~D0: RAM data

D/C: Data/command mode

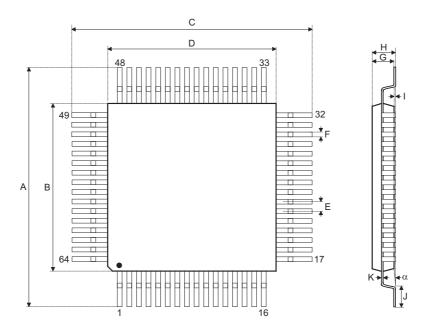
Def.: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from a 32.768kHz crystal oscillator. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1620 after power on reset, for power on reset may fail, which in turn leads to malfunctioning of the HT1620.



Package Information

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol		Dimensions in mm	
Symbol	Min.	Nom.	Max.
A	8.9	—	9.1
В	6.9	_	7.1
С	8.9		9.1
D	6.9		7.1
E		0.4	_
F	0.13		0.23
G	1.35		1.45
Н		_	1.6
I	0.05		0.15
J	0.45		0.75
К	0.09		0.20
α	0°		7 °



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