secos
Elektronische Bauelemente

STT6601

(N-Ch) 2.8 A, 30 V, RDS(ON) 68 mΩ
(P-Ch) -2.8 A, -30 V, RDS(ON) 120 mΩ
N & P-Channel Enhancement Mode Mos.FET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

The STT6601 is the N and P Channel enhancement mode power FET produced using high cell-density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery-powered circuits where high-side switching, low in-line power loss and resistance to transients are needed.

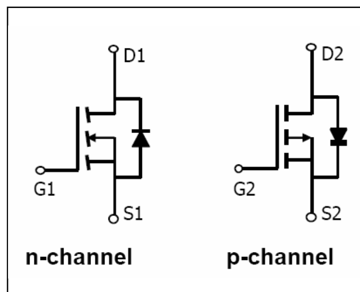
FEATURES

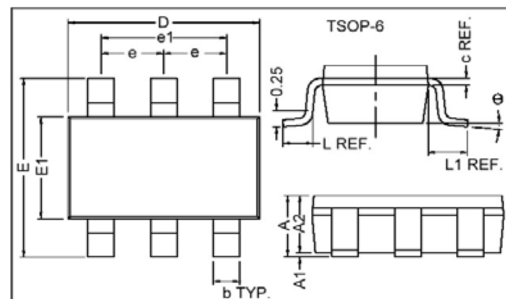
- N-Channel
  30V/2.8A, $R_{DS(ON)}$ = 68mΩ@VGS = 10 V
  30V/2.3A, $R_{DS(ON)}$ = 78mΩ@VGS = 4.5 V
  30V/1.5A, $R_{DS(ON)}$ = 108mΩ@VGS = 2.5 V
- P-Channel
  -30V/-2.8A, $R_{DS(ON)}$ = 105mΩ@VGS = 10 V
  -30V/-2.5A, $R_{DS(ON)}$ = 120mΩ@VGS = 4.5 V
  -30V/-1.5A, $R_{DS(ON)}$ = 150mΩ@VGS = 2.5 V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TSOP-6P package design

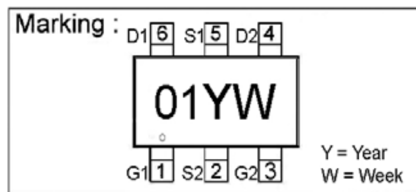
APPLICATIONS

- Battery powered systems
- Portable devices
- Power management in NB
- DC to DC converter, load switch, DSC, LCD display inverter

PACKAGE DIMENSIONS







Week code: A~Z (1~26); a ~ z (27 ~ 52)

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.10 Max		L	0.45 Ref	
A1	0	0.10	L1	0.60 Ref	
A2	0.70	1.00		0°	10°
c	0.12 Ref		b	0.30	0.50
D	2.70	3.10	e	0.95 Ref	
E	2.60	3.00	e1	1.90 Ref	
E1	1.40	1.80			

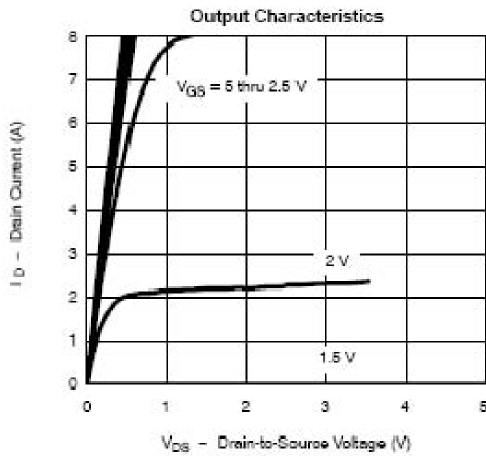
ABSOLUTE MAXIMUM RATINGS

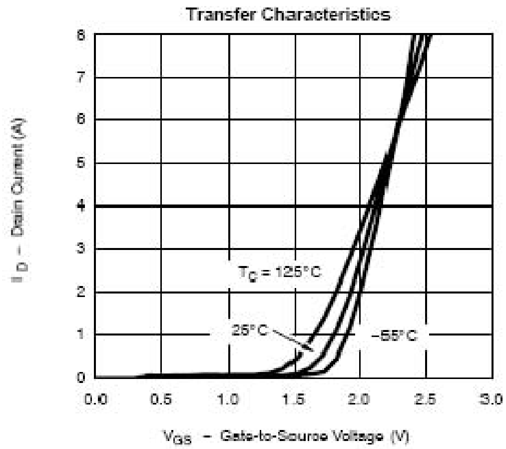
Parameter		Symbol	Ratings		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current (TJ=150℃)		I_D @TA=25℃	2.8	-2.8	A
		I_D @TA=70℃	2.3	-2.1	
Pulsed Drain Current		I_{DM}	10	-8	A
Power Dissipation		P_D @TA=25℃	1.15		W
		P_D @TA=70℃	0.75		
Continuous Source Current (Diode Conduction)		I_S	1.25	-1.4	A
Thermal Resistance- Junction to Ambient	T ≦ 10 sec	RθJA	50	52	℃/W
	Steady State		90	90	
Operating Junction and Storage Temperature Range		Tj, Tstg	-55 ~ +150		℃

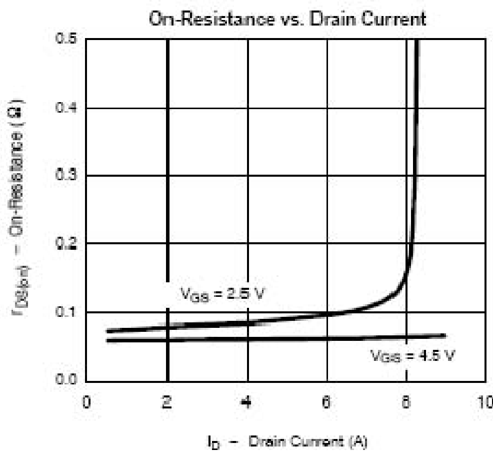
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

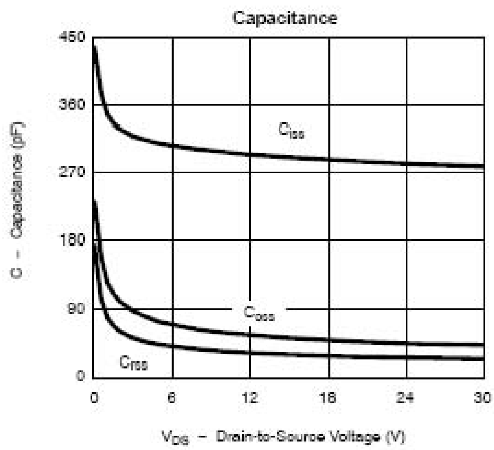
Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	N-Ch	BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250uA
	P-Ch		-30	-	-		V_{GS}=0, I_D=-250uA
Gate Threshold Voltage	N-Ch	$V_{GS(th)}$	0.8	-	1.6	V	V_{DS}=V_{GS}, I_D=250uA
	P-Ch		-0.4		-1.0		V_{DS}=V_{GS}, I_D=-250uA
Forward Transconductance	N-Ch	g_{fs}	-	4.6	-	S	V_{DS}=4.5V, I_D=-6.0A
	P-Ch		-	4	-		V_{DS}=-10V, I_D=-2.8A
Gate Leakage Current	N-Ch	I_{GSS}	-	-	±100	nA	V_{DS}= 0 V, V_{GS}=±12 V
	P-Ch		-	-	±100		V_{DS}= 0 V, V_{GS}=±12 V
Zero Gate Voltage Drain Current (Tj=25℃)	N-Ch	I_{DSS}	-	-	1	uA	V_{DS}=24 V, V_{GS}=0 V
	P-Ch		-	-	-1		V_{DS}=-24V, V_{GS}=0 V
	N-Ch		-	-	10		V_{DS}=24V, V_{GS}=0 V, T_J=55℃
	P-Ch		-	-	-10		V_{DS}=-24V, V_{GS}=0 V, T_J=55℃
On-State Drain Current	N-Ch	$I_{D(on)}$	6	-	-	A	$V_{DS} \geqq$ 5V, V_{GS}=10 V
	P-Ch		-6	-	-		$V_{DS} \leqq$ -5V, V_{GS}= -10 V
Drain-Source On-Resistance	N-Ch	$R_{DS(ON)}$	-	0.048	0.068	Ω	V_{GS}=10V, I_D=2.8A
	P-Ch		-	0.077	0.105		V_{GS}=-10V, I_D=-2.8A
	N-Ch		-	0.054	0.078		V_{GS}=4.5V, I_D=2.3A
	P-Ch		-	0.092	0.120		V_{GS}=-4.5V, I_D=-2.5A
	N-Ch		-	0.079	0.108		V_{GS}=2.5V, I_D=1.5A
	P-Ch		-	0.118	0.150		V_{GS}=-2.5V, I_D=-1.5A
Total Gate Charge	N-Ch	Q_g	-	4.2	6	nC	N-Channel V_{DS}=15V, V_{GS}=4.5V , I_D=2.0A P-Channel V_{DS}=-15V, V_{GS}=-4.5V ,I_D=-2.0A
	P-Ch		-	5.8	-		
Gate-Source Charge	N-Ch	Q_{gs}	-	0.6	-		
	P-Ch		-	0.8	-		
Gate-Drain Charge	N-Ch	Q_{gd}	-	1.5	-		
	P-Ch		-	1.5	-		
Turn-on Time	N-Ch	$T_{d(on)}$	-	2.5	-	ns	N-Channel V_{DD}=15V R_L=10Ω V_{GEN}=10V R_G=3Ω P-Channel V_{DD}=-15V R_L=15Ω V_{GEN}=-10V R_G=3Ω
	P-Ch		-	6	-		
	N-Ch	T_r	-	2.5	-		
	P-Ch		-	3.9	-		
Turn-off Time	N-Ch	$T_{d(off)}$	-	20	-		
	P-Ch		-	40	-		
	N-Ch	T_f	-	4	-		
	P-Ch		-	15	-		

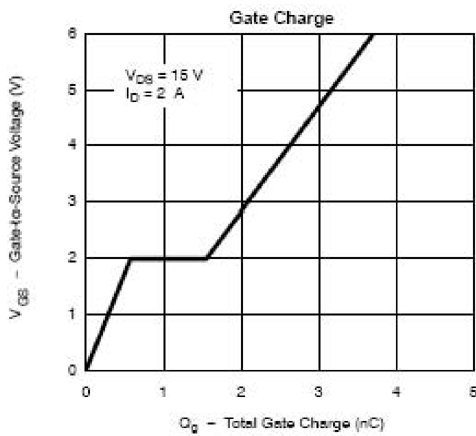
CHARACTERISTIC CURVES (N-Channel)

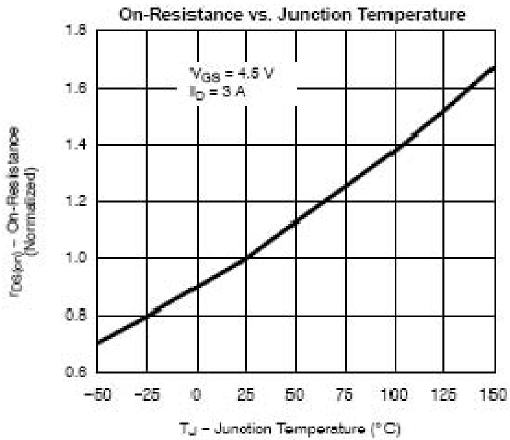


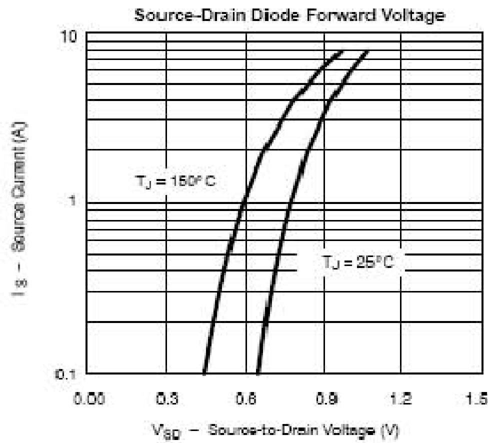


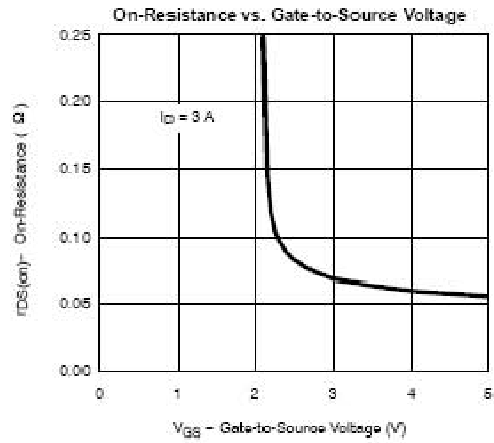


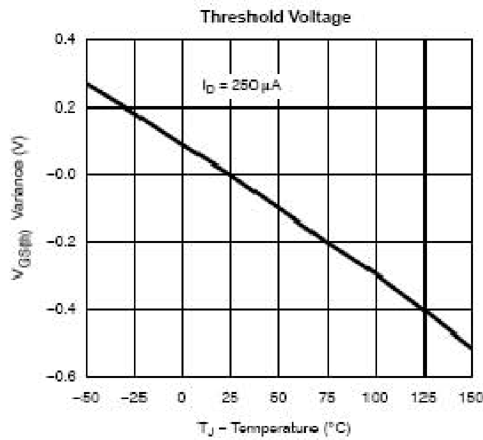


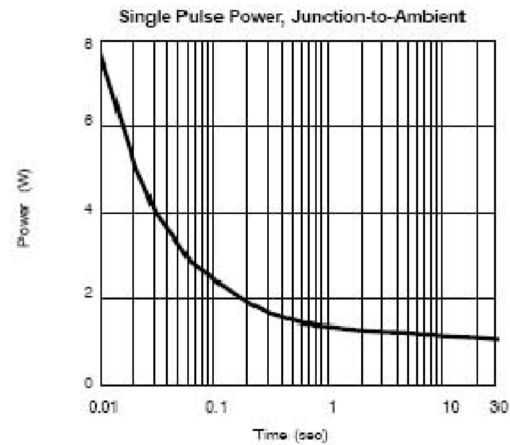


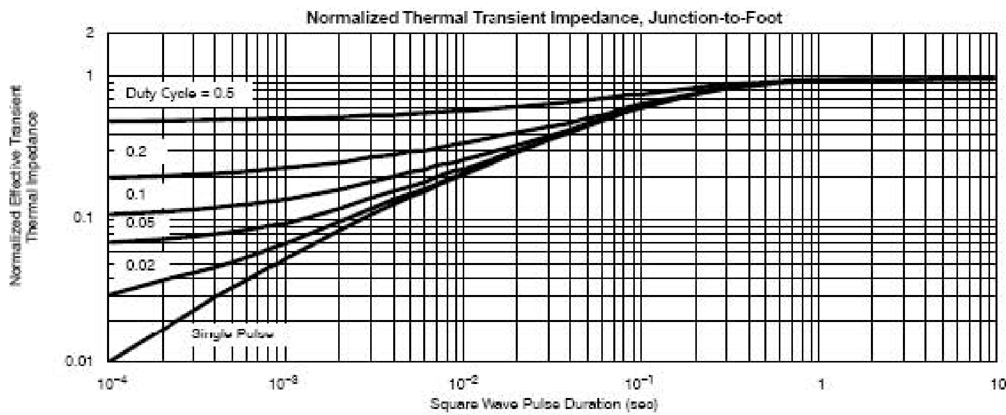



Source-Drain Diode Forward Voltage
I_S – Source Current (A)
T_J = 150° C
T_J = 25° C
V_{SD} – Source-to-Drain Voltage (V)

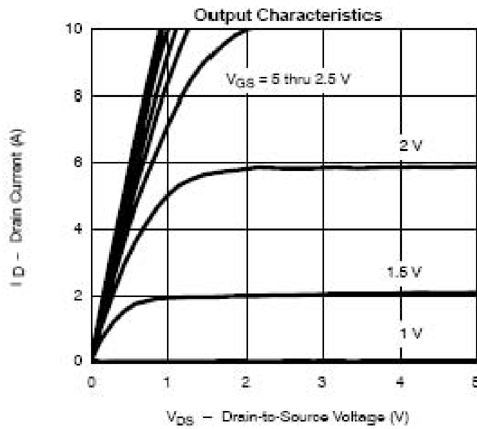

On-Resistance vs. Gate-to-Source Voltage
rDS(on)– On-Resistance (Ω)
I_D = 3 A
V_{GS} – Gate-to-Source Voltage (V)

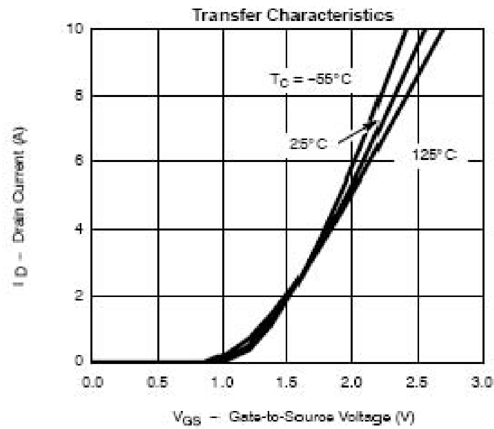

Threshold Voltage
$V_{GS(th)}$ Variance (V)
I_D = 250 µA
T_J – Temperature (°C)

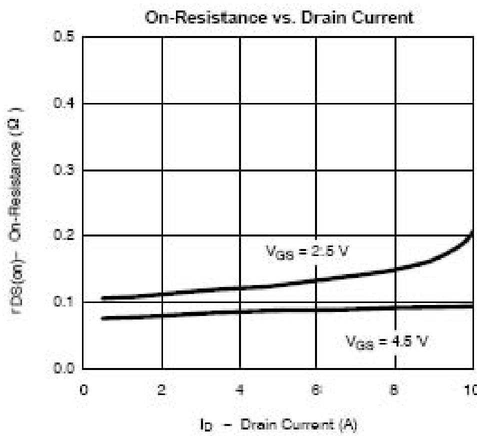

Single Pulse Power, Junction-to-Ambient
Power (W)
Time (sec)

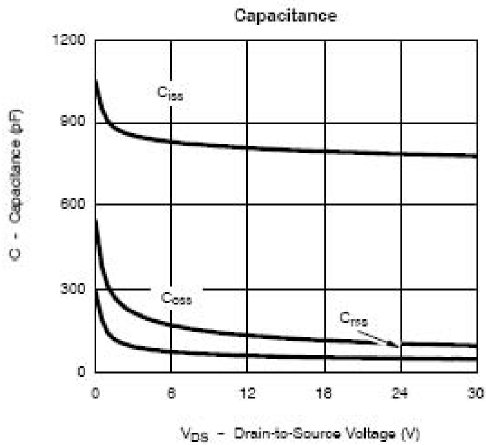

Normalized Thermal Transient Impedance, Junction-to-Foot
Normalized Effective Transient Thermal Impedance
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
Single Pulse
Square Wave Pulse Duration (sec)

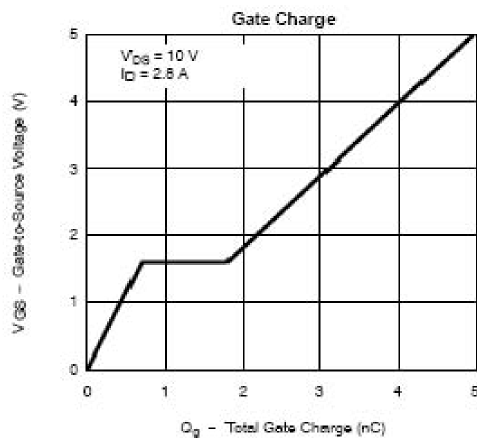
CHARACTERISTIC CURVES (N-Channel)

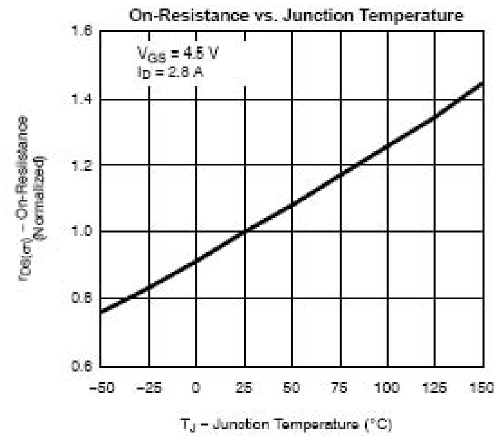


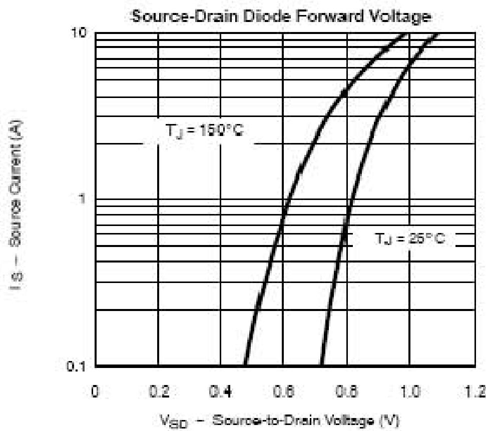




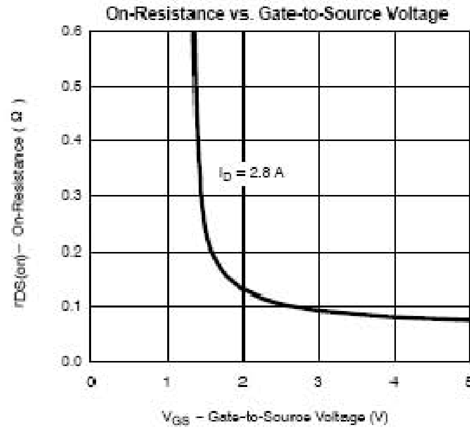




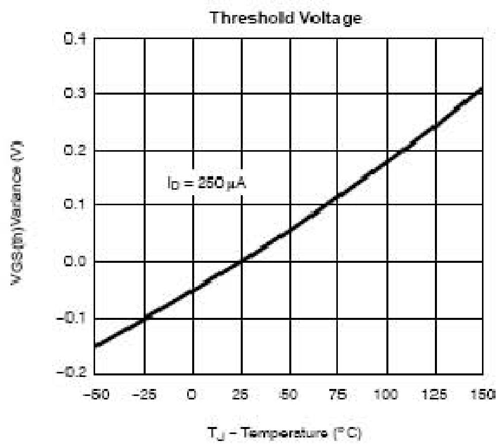




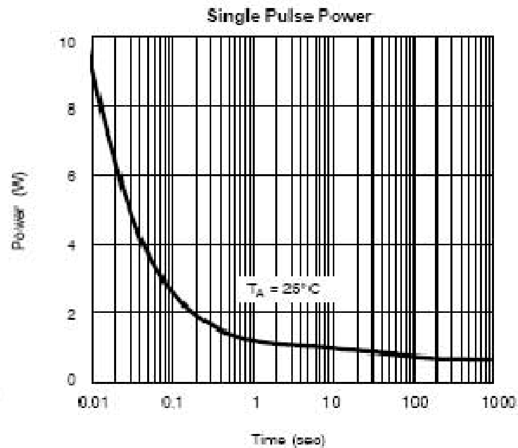
Source-Drain Diode Forward Voltage
I S – Source Current (A)
10
1
0.1
TJ = 150°C
TJ = 25°C
0
0.2
0.4
0.6
0.8
1.0
1.2
VSD – Source-to-Drain Voltage (V)



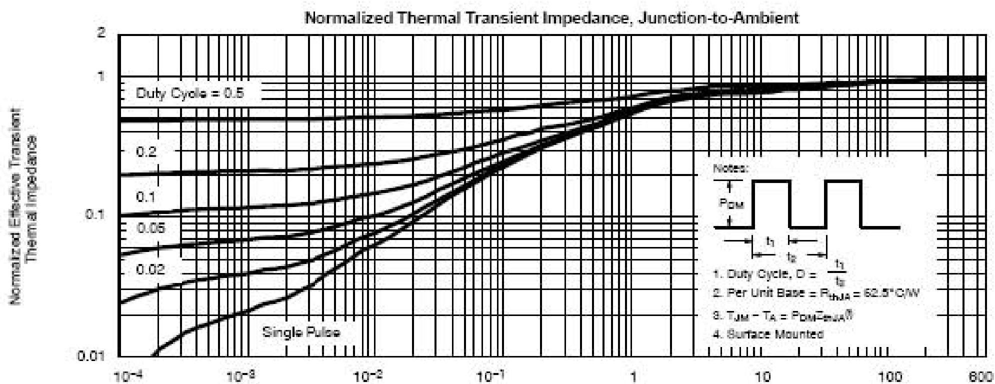
On-Resistance vs. Gate-to-Source Voltage
rDS(on) – On-Resistance (Ω)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
ID = 2.8 A
0
1
2
3
4
5
VGS – Gate-to-Source Voltage (V)



Threshold Voltage
VGS(th) Variance (V)
0.4
0.3
0.2
0.1
0.0
–0.1
–0.2
ID = 250 μA
–50
–25
0
25
50
75
100
125
150
TJ – Temperature (°C)



Single Pulse Power
Power (W)
10
8
6
4
2
0
TA = 25°C
0.01
0.1
1
10
100
1000
Time (sec)



Normalized Thermal Transient Impedance, Junction-to-Ambient
Normalized Effective Transient Thermal Impedance
2
1
0.1
0.01
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
Single Pulse
Notes:
PDM
t1
t2
1. Duty Cycle, D = t1/t2
2. Per Unit Base = RthJA = 62.5°C/W
3. TJM – TA = PDMZthJA(t)
4. Surface Mounted
10⁻⁴
10⁻³
10⁻²
10⁻¹
1
10
100
600