Complete Isolated RS485/RS422 µModule Transceiver + Power

FEATURES

- **Isolator µModule Technology**
- **Isolated RS485/RS422 Transceiver: 2500V_{RMS}**
- **Integrated Isolated DC/DC Converter: 1W, 62% Efficiency**
- **No External Components Required**
- **20Mbps or Low EMI 250kbps Data Rate**
- **High ESD: ±15kV HBM on Transceiver Interface**
- **High Common Mode Transient Immunity: 30kV/µs**
- **Integrated Selectable 120Ω Termination**
- 3.3V (LTM2881-3) or 5.0V (LTM2881-5) Operation
- 1.62V to 5.5V Logic Supply Pin for Flexible Digital Interface
- Common Mode Working Voltage: 560V_{PEAK}
- High Input Impedance Failsafe RS485 Receiver
- Current Limited Drivers and Thermal Shutdown
- Compatible with TIA/EIA-485-A Specification
- High Impedance Output During Internal Fault Condition
- Low Current Shutdown Mode (< 10µA)
- General Purpose CMOS Isolated Channel
- Small, Low Profile (15mm × 11.25mm × 2.8mm) Surface Mount LGA Package

APPLICATIONS

- Isolated RS485/RS422 Interface
- Industrial Networks
- Breaking RS485 Ground Loops

DESCRIPTION

The LTM®2881 is a complete galvanically isolated full-duplex RS485/RS422 µModule® transceiver. No external components are required. A single supply powers both sides of the interface through an integrated, isolated, low noise, efficient 5V output DC/DC converter.

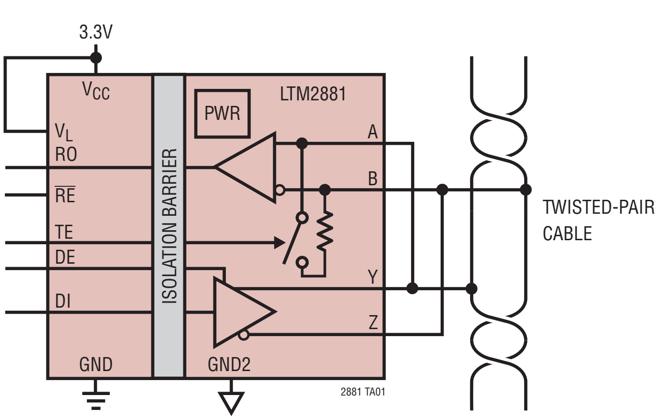
Coupled inductors and an isolation power transformer provide 2500V_{RMS} of isolation between the line transceiver and the logic interface. This device is ideal for systems where the ground loop is broken allowing for large common mode voltage variation. Uninterrupted communication is guaranteed for common mode transients greater than 30kV/µs.

Maximum data rates are 20Mbps or 250kbps in slew limited mode. Transmit data, DI and receive data, RO, are implemented with event driven low jitter processing. The receiver has a one-eighth unit load supporting up to 256 nodes per bus. A logic supply pin allows easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

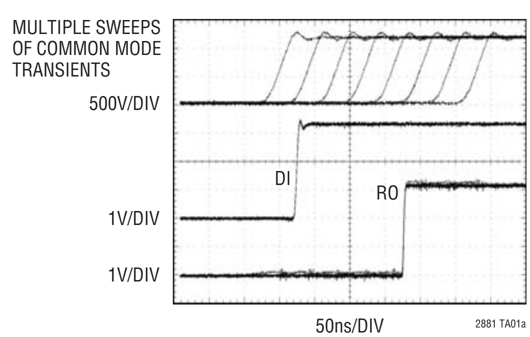
Enhanced ESD protection allows this part to withstand up to ±15kV (human body model) on the transceiver interface pins to isolated supplies and ±10kV through the isolation barrier to logic supplies without latch-up or damage.

TYPICAL APPLICATION

Isolated Half-Duplex RS485 µModule Transceiver



LTM2881 Operating Through 35kV/µs CM Transient

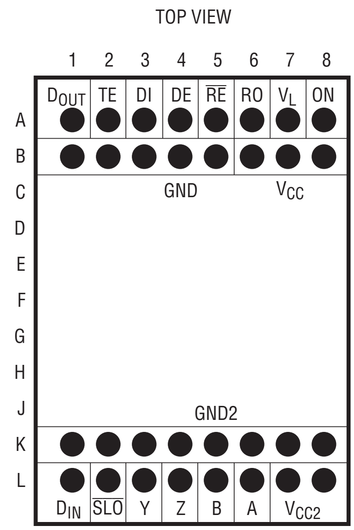


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND .... –0.3V to 6V
V_{CC2} to GND2 .... –0.3V to 6V
V_L to GND .... –0.3V to 6V
Interface Voltages
(A, B, Y, Z) to GND2 .... V_{CC2} –15V to 15V
Signal Voltages ON, RO, DI, DE,
$\overline{RE}$, TE, D_{OUT} to GND .... –0.3V to V_L +0.3V
Signal Voltages $\overline{SLO}$,
D_{IN} to GND2 .... –0.3V to V_{CC2} +0.3V
Operating Temperature Range
LTM2881C .... 0°C to 70°C
LTM2881I .... –40°C to 85°C
Storage Temperature Range .... –55°C to 125°C
Peak Reflow Temperature (Soldering, 10 sec) ...... 245°C

PIN CONFIGURATION



LGA PACKAGE
32-PIN (15mm × 11.25mm × 2.8mm)
T_{JMAX} = 125°C, θ_{JA} = 32°C/W WEIGHT = 1_g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM2881CV-3#PBF	LTM2881CV-3#PBF	LTM2881V-3	32-Pin (15mm × 11.25mm × 2.8mm) LGA	0°C to 70°C
LTM2881IV-3#PBF	LTM2881IV-3#PBF	LTM2881V-3	32-Pin (15mm × 11.25mm × 2.8mm) LGA	–40°C to 85°C
LTM2881CV-5#PBF	LTM2881CV-5#PBF	LTM2881V-5	32-Pin (15mm × 11.25mm × 2.8mm) LGA	0°C to 70°C
LTM2881IV-5#PBF	LTM2881IV-5#PBF	LTM2881V-5	32-Pin (15mm × 11.25mm × 2.8mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	V_{CC} Supply Voltage	LTM2881-3 LTM2881-5	● ●	3.0 4.5	3.3 5.0	3.6 5.5	V V
V_L	V_L Supply Voltage		●	1.62		5.5	V
I_{CCPOFF}	V_{CC} Supply Current in Off Mode	ON = 0V	●		0	10	µA
I_{CCS}	V_{CC} Supply Current in On Mode	LTM2881-3 DE = 0V, $\overline{RE}$ = V_L, No Load LTM2881-5 DE = 0V, $\overline{RE}$ = V_L, No Load	● ●		20 15	25 19	mA mA
V_{CC2}	Regulated V_{CC2} Output Voltage, Loaded	LTM2881-3 DE = 0V, $\overline{RE}$ = V_L, I_{LOAD} = 100mA LTM2881-5 DE = 0V, $\overline{RE}$ = V_L, I_{LOAD} = 180mA	●	4.7 4.7	5.0 5.0		V V
$V_{CC2NOLOAD}$	Regulated V_{CC2} Output Voltage, No Load	DE = 0V, $\overline{RE}$ = V_L, No Load		4.8	5.0	5.35	V
	Efficiency	I_{CC2} = 100mA (Note 2)			50		%
I_{CC2S}	V_{CC2} Short-Circuit Current	DE = 0V, $\overline{RE}$ = V_L, V_{CC2} = 0V	●			250	mA
Driver							
$\|V_{OD}\|$	Differential Driver Output Voltage	R = ∞ (Figure 1) R = 27Ω (RS485) (Figure 1) R = 50Ω (RS422) (Figure 1)	● ● ●	 1.5 2		V_{CC2} V_{CC2} V_{CC2}	V V V
$\Delta\|V_{OD}\|$	Difference in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Driver Common Mode Output Voltage	R = 27Ω or R = 50Ω (Figure 1)	●			3	V
$\Delta\|V_{OC}\|$	Difference in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)	●			0.2	V
I_{OZD}	Driver Three-State (High Impedance) Output Current on Y and Z	DE = 0V, (Y or Z) = –7V, +12V	●			±10	µA
I_{OSD}	Maximum Driver Short-Circuit Current	–7V ≤ (Y or Z) ≤ 12V (Figure 2)	●	–250		250	mA
Receiver							
R_{IN}	Receiver Input Resistance	$\overline{RE}$ = 0V or V_L, V_{IN} = –7V, –3V, 3V, 7V, 12V (Figure 3)	●	96	125		kΩ
R_{TE}	Receiver Termination Resistance Enabled	TE = V_L, V_{AB} = 2V, V_B = –7V, 0V, 10V (Figure 8)	●	108	120	156	Ω
I_{IN}	Receiver Input Current (A, B)	ON = 0V V_{CC2} = 0V or 5V, V_{IN} = 12V (Figure 3)	●			125	µA
		ON = 0V V_{CC2} = 0V or 5V, V_{IN} = –7V (Figure 3)	●	–100			µA
V_{TH}	Receiver Differential Input Threshold Voltage (A-B)	–7V ≤ B ≤ 12V	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Failsafe Hysteresis	B = 0V			25		mV
	Receiver Input Failsafe Threshold	B = 0V		–0.2	–0.05	0	V
Logic							
V_{IL}	Logic Input Low Voltage	1.62V ≤ V_L ≤ 5.5V	●			0.4	V
V_{IH}	Logic Input High Voltage	D_{IN} $\overline{SLO}$ DI, TE, DE, ON, $\overline{RE}$: V_L ≥ 2.35V 1.62V ≤ V_L < 2.35V	● ● ● ●	0.67•V_{CC2} 2 0.67•V_L 0.75•V_L			V V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{INL}	Logic Input Current		●		0	±1	µA
V_{HYS}	Logic Input Hysteresis	(Note 2)			150		mV
V_{OH}	Output High Voltage	Output High, I_{LOAD} = –4mA (Sourcing), 5.5V ≥ V_L ≥ 3V Output High, I_{LOAD} = –1mA (Sourcing), 1.62V ≤ V_L < 3V	● ●	V_L –0.4 V_L –0.4			V V
V_{OL}	Output Low Voltage	Output Low, I_{LOAD} = 4mA (Sinking), 5.5V ≥ V_L ≥ 3V Output High, I_{LOAD} = 1mA (Sinking), 1.62V ≤ V_L < 3V	● ●			0.4 0.4	V V
I_{OZR}	Three-State (High Impedance) Output Current on RO	$\overline{RE}$ = V_L, 0V ≤ RO ≤ V_L	●			±1	µA
I_{OSR}	Short-Circuit Current	0V ≤ (RO or D_{OUT}) ≤ V_L	●			±85	mA

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Driver $\overline{SLO}$ = V_{CC2}							
f_{MAX}	Maximum Data Rate	(Note 3)		20			Mbps
t_{PLHD} t_{PHLD}	Driver Input to Output	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		60	85	ns
Δt_{PD}	Driver Input to Output Difference $\|t_{PLHD} – t_{PHLD}\|$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		1	8	ns
t_{SKEWD}	Driver Output Y to Output Z	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		1	±8	ns
t_{RD} t_{FD}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		4	12.5	ns
t_{ZLD}, t_{ZHD}, t_{LZD}, t_{HZD}	Driver Output Enable or Disable Time	R_L = 500Ω, C_L = 50pF (Figure 5)	●			170	ns
Driver $\overline{SLO}$ = GND2							
f_{MAX}	Maximum Data Rate	(Note 3)		250			kbps
t_{PLHD} t_{PHLD}	Driver Input to Output	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)			1	1.55	µs
Δt_{PD}	Driver Input to Output Difference $\|t_{PLHD} – t_{PHLD}\|$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)			50	500	ns
t_{SKEWD}	Driver Output Y to Output Z	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)			±200	±500	ns
t_{RD} t_{FD}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		0.9	1.5	µs
t_{ZLD}, t_{ZHD}, t_{LZD}, t_{HZD}	Driver Output Enable or Disable Time	R_L = 500Ω, C_L = 50pF (Figure 5)	●			400	ns

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver							
t_{PLHR} t_{PHLR}	Receiver Input to Output	C_L = 15pF, V_{CM} = 2.5V, $\|V_{AB}\|$ = 1.4V, t_R and t_F < 4ns, (Figure 6)	●		100	140	ns
t_{SKEWR}	Differential Receiver Skew $\|t_{PLHR} - t_{PHLR}\|$	C_L = 15pF (Figure 6)	●		1	8	ns
t_{RR} t_{FR}	Receiver Output Rise or Fall Time	C_L = 15pF (Figure 6)	●		3	12.5	ns
t_{ZLR}, t_{ZHR}, t_{LZR}, t_{HZR}	Receiver Output Enable Time	R_L =1kΩ, C_L = 15pF (Figure 7)	●			50	ns
t_{RTEN}, t_{RTZ}	Termination Enable or Disable Time	$\overline{RE}$ = 0V, DE = 0V, V_{AB} = 2V, V_B = 0V (Figure 8)	●			100	µs
Generic Logic Input							
t_{PLHL1} t_{PHLL1}	D_{IN} to D_{OUT} Input to Output	C_L = 15pF, t_R and t_F < 4ns	●		60	100	ns
Power Supply Generator							
	V_{CC2}–GND2 Supply Start-Up Time (0V to 4.5V)	ON ⮥ V_L, No Load	●		325	800	µs

ISOLATION CHARACTERISTICS

T_A = 25°C, LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Minute (Derived from 1 Second Test)	2500			V_{RMS}
		1 Second	±4400			V_{DC}
	Common Mode Transient Immunity	(Note 2)	30			kV/µs
V_{IORM}	Maximum Working Insulation Voltage	(Note 2)	560			V_{PEAK}
	Partial Discharge	V_{PR} = 1050 V_{PEAK} (Note 2)			<5	pC
	Input to Output Resistance	(Note 2)	>10^9			Ω
	Input to Output Capacitance	(Note 2)		6		pF
	Creepage Distance	(Note 2)		9.48		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

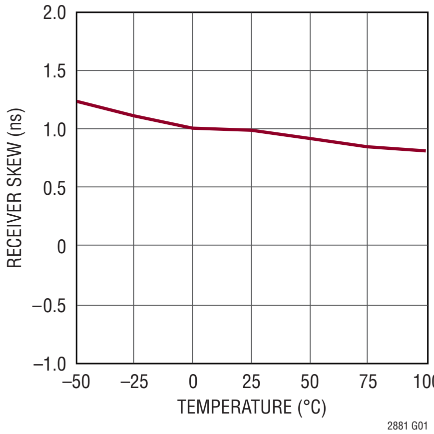
Note 3: Maximum Data rate is guaranteed by other measured parameters and is not tested directly.

Note 4: This µModule transceiver includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

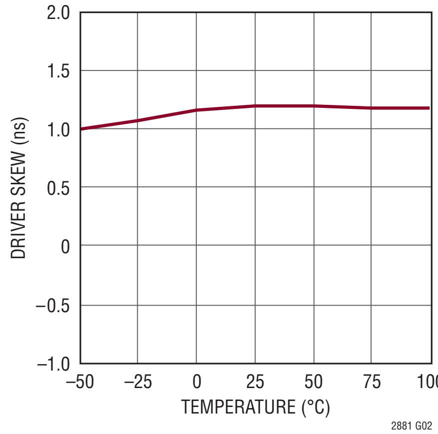
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V unless otherwise noted.

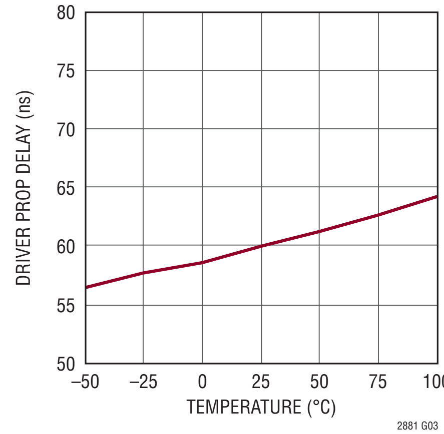
Receiver Skew vs Temperature



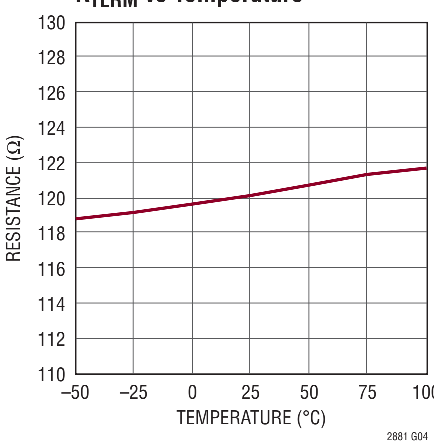
Driver Skew vs Temperature



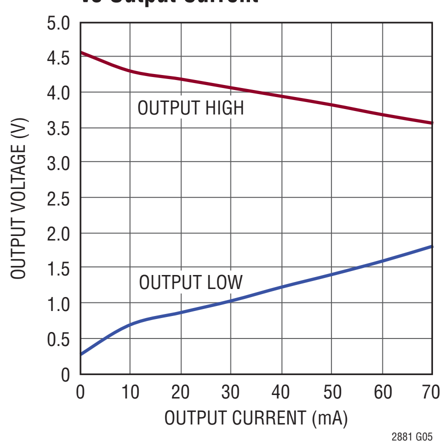
Driver Propagation Delay vs Temperature



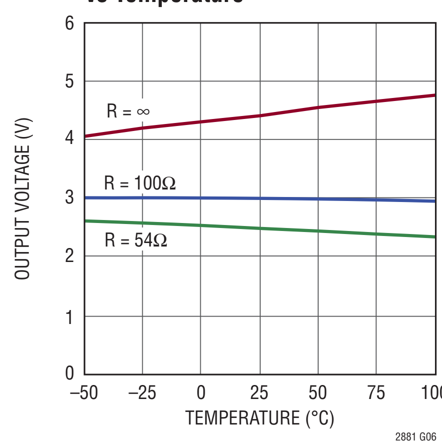
R_{TERM} vs Temperature



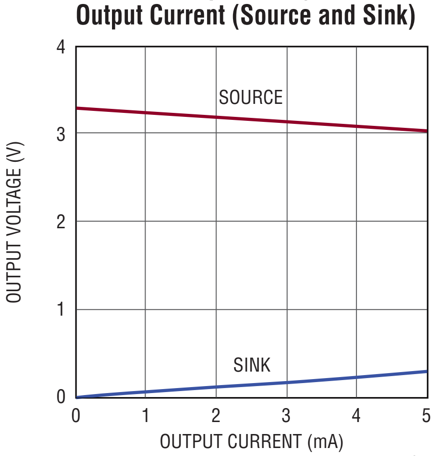
Driver Output Low/High Voltage vs Output Current



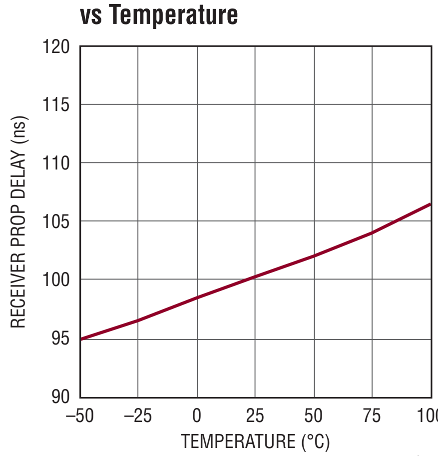
Driver Differential Output Voltage vs Temperature



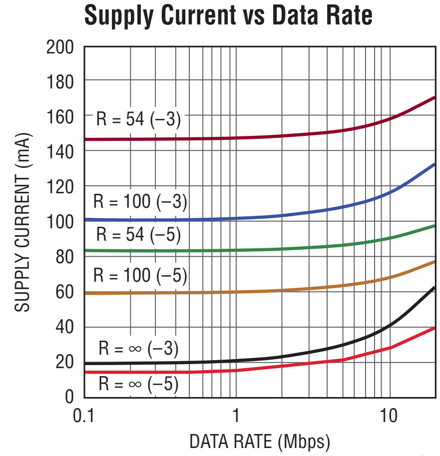
Receiver Output Voltage vs Output Current (Source and Sink)



Receiver Propagation Delay vs Temperature



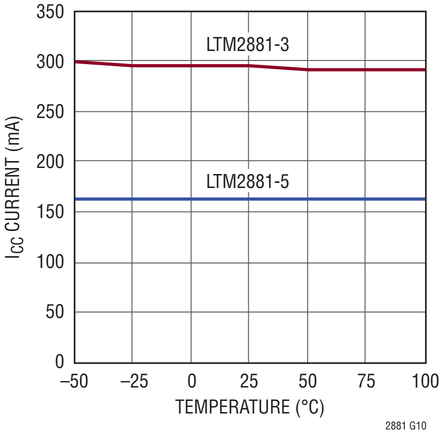
Supply Current vs Data Rate



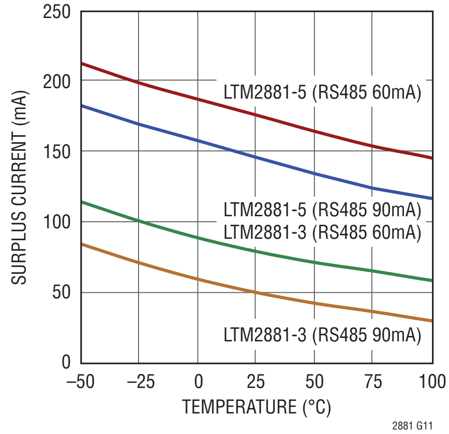
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V unless otherwise noted.

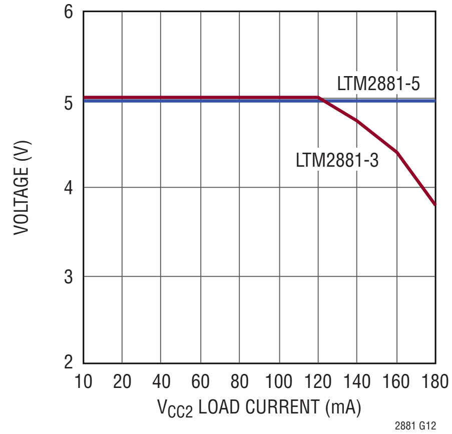
V_{CC} Supply Current vs Temperature at I_{LOAD} = 100mA on V_{CC2}



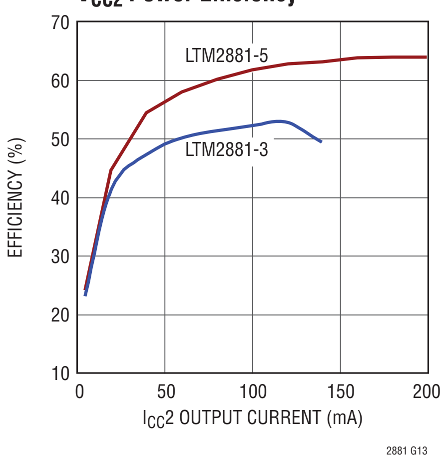
V_{CC2} Surplus Current vs Temperature



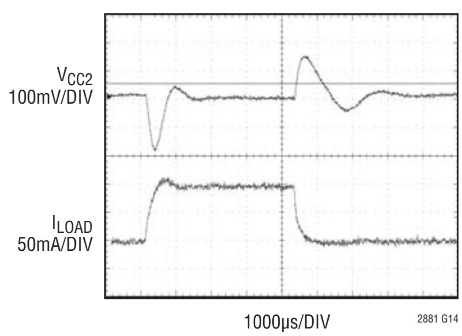
V_{CC2} vs Load Current



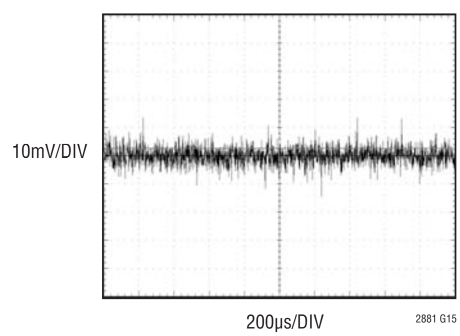
V_{CC2} Power Efficiency



V_{CC2} Load Step (100mA)



V_{CC2} Noise



PIN FUNCTIONS

LOGIC SIDE (V_{CC}, V_L, GND)

D_{OUT} (Pin A1): General Purpose Logic Output. Logic output connected through isolation path to D_{IN}. Under the condition of an isolation communication failure D_{OUT} is in a high impedance state.

TE (Pin A2): Terminator Enable. A logic high enables a termination resistor (typically 120Ω) between pins A and B.

DI (Pin A3): Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the driver noninverting output (Y) low and the inverting output (Z) high. A high on DI, with the driver outputs enabled, forces the driver noninverting output (Y) high and inverting output (Z) low.

DE (Pin A4): Driver Enable. A logic low disables the driver leaving the outputs Y and Z in a high impedance state. A logic high enables the driver.

$\overline{RE}$ (Pin A5): Receiver Enable. A logic low enables the receiver output. A logic high disables RO to a high impedance state.

RO (Pin A6): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low) and if A – B is > 200mV, RO is a logic high, if A – B is < 200mV RO is a logic low. If the receiver inputs are open, shorted, or terminated without a valid signal, RO will be high. Under the condition of an isolation communication failure RO is in a high impedance state.

V_L (Pin A7): Logic Supply. Interface supply voltage for pins RO, $\overline{RE}$, TE, DI, DE, D_{OUT}, and ON. Recommended operating voltage is 1.62V to 5.5V.

ON (Pin A8): Enable. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset and the isolated side is unpowered.

GND (Pins B1-B5): Circuit Ground.

V_{CC} (Pins B6-B8): Supply Voltage. Recommended operating voltage is 3V to 3.6V for LTM2881-3 and 4.5V to 5.5V for LTM2881-5.

ISOLATED SIDE (V_{CC2}, GND2)

D_{IN} (Pin L1): General Purpose Isolated Logic Input. Logic input on the isolated side relative to V_{CC2} and GND2. A logic high on D_{IN} will generate a logic high on D_{OUT}. A logic low on D_{IN} will generate a logic low on D_{OUT}.

$\overline{SLO}$ (Pin L2): Driver Slew Rate Control. A low input, relative to GND2, will force the driver into a reduced slew rate mode for reduced EMI. A high input, relative to GND2, puts the driver into full speed mode to support maximum data rates.

Y (Pin L3): Non Inverting Driver Output. High impedance when the driver is disabled.

Z (Pin L4): Inverting Driver Output. High impedance when the driver is disabled.

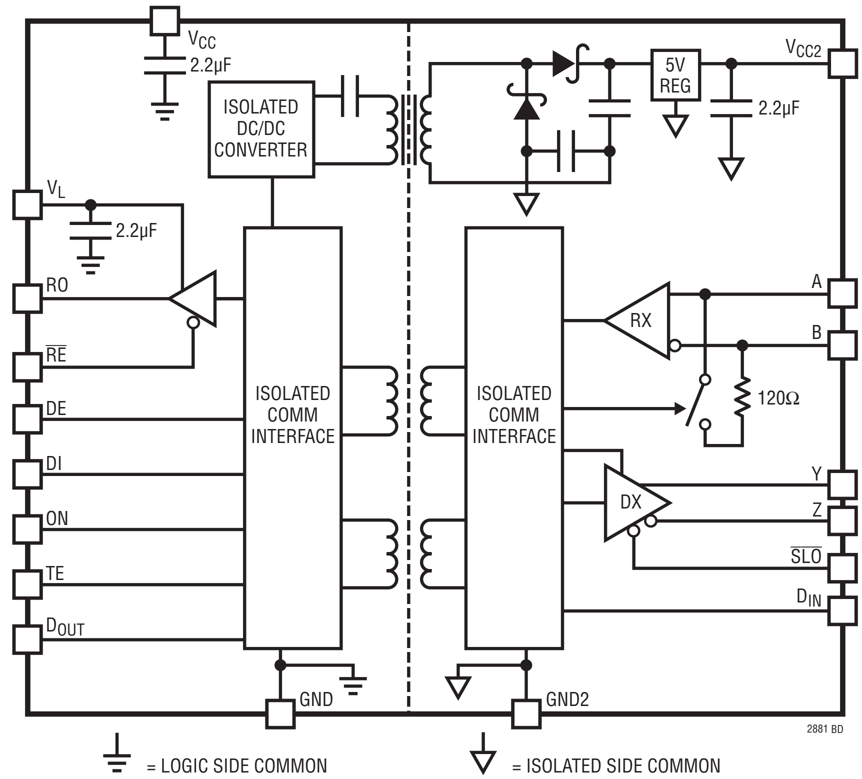
B (Pin L5): Inverting Receiver Input. Impedance is > 96kΩ in receive mode with TE low or unpowered.

A (Pin L6): Non Inverting Receiver Input. Impedance is > 96kΩ in receive mode with TE low or unpowered.

V_{CC2} (Pins L7-L8): Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 5V.

GND2 (Pins K1-K8): Isolated Side Circuit Ground. The pads should be connected to the isolated ground and/or cable shield.

BLOCK DIAGRAM



TEST CIRCUITS

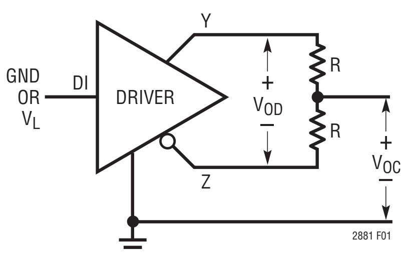


Figure 1. Driver DC Characteristics

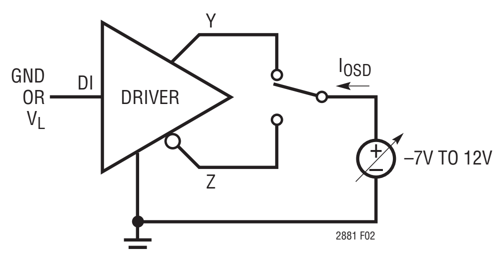
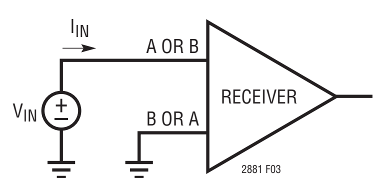


Figure 2. Driver Output Short-Circuit Current



$R_{IN} = \frac{V_{IN}}{I_{IN}}$

Figure 3. Receiver Input Current and Input Resistance

TEST CIRCUITS

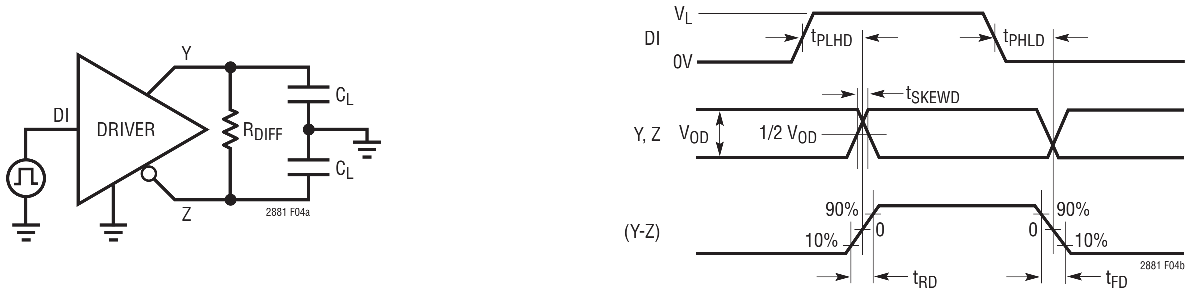


Figure 4. Driver Timing Measurement

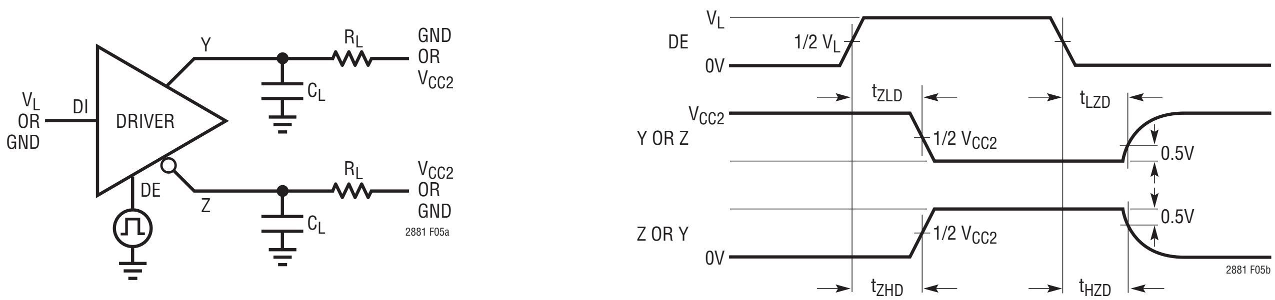


Figure 5. Driver Enable and Disable Timing Measurements

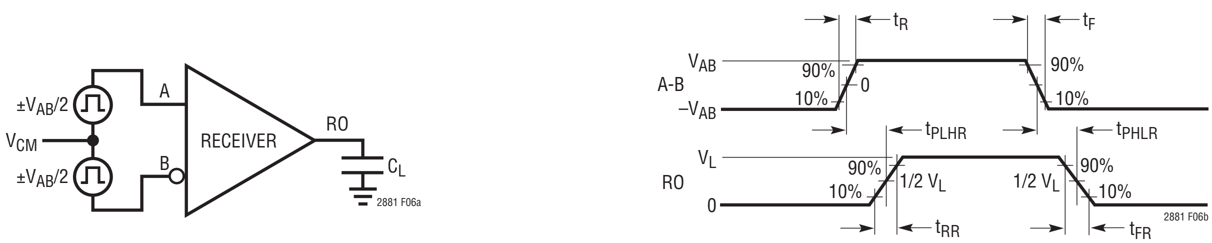


Figure 6. Receiver Propagation Delay Measurements

TEST CIRCUITS

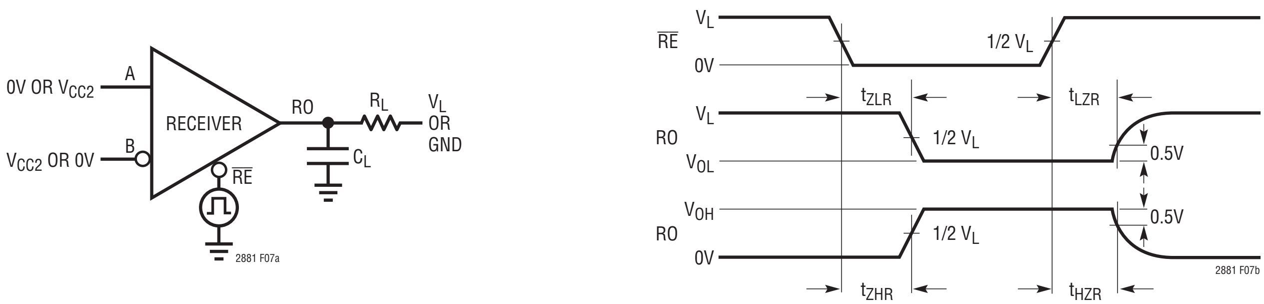


Figure 7. Receiver Enable/Disable Time Measurements

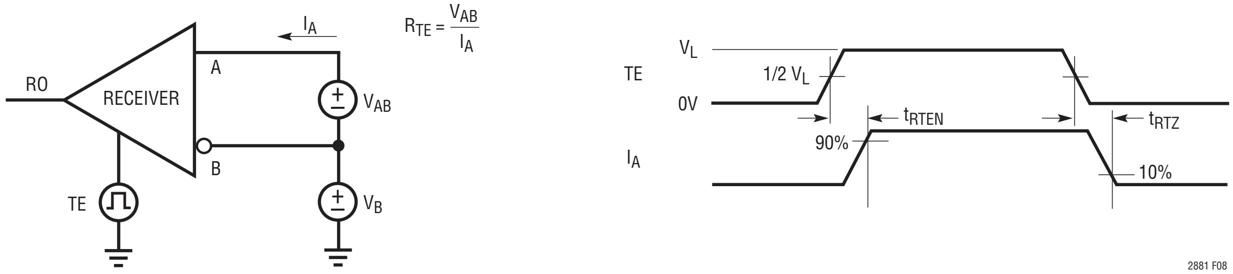


Figure 8. Termination Resistance and Timing Measurements

FUNCTIONAL TABLE

LOGIC INPUTS				MODE	A, B	Y, Z	RO	DC/DC CONVERTER	TERMINATOR
ON	$\overline{RE}$	TE	DE						
1	0	0	0	Receive	R_{IN}	Hi-Z	Enabled	On	Off
1	0	0	1	Transceiver	R_{IN}	Driven	Enabled	On	Off
1	1	0	1	Transmit	R_{IN}	Driven	Hi-Z	On	Off
1	0	1	0	Receive + Term On	R_{TE}	Hi-Z	Enabled	On	On
0	X	X	X	Off	R_{IN}	Hi-Z	Hi-Z	Off	Off

APPLICATIONS INFORMATION

Overview

The LTM2881 μModule transceiver provides a galvanically-isolated robust RS485/RS422 interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. A switchable termination resistor is integrated at the receiver input to provide proper termination to the RS485 bus. The LTM2881 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2881 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground potentials. Error free operation is maintained through common mode events greater than 30kV/μs providing excellent noise isolation.

DC/DC Converter

The LTM2881 contains a fully integrated isolated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running about 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a full-wave voltage doubler. This topology eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated low noise 5V output.

The internal power solution is sufficient to support the transceiver interface at its maximum specified load and data rate, and external pins are supplied for extra decoupling (optional) and heat dissipation. The logic supplies, V_{CC} and V_L have a 2.2μF decoupling capacitance to GND and the isolated supply V_{CC2} has a 2.2μF decoupling capacitance to GND2 within the μModule package. Surplus current is available to external applications. The amount of surplus current is dependent upon the implementation and current delivered to the RS485 driver and line load. An example of available surplus current is shown in the Typical Performance Characteristics graph, V_{CC2} Surplus Current vs Temperature.

Driver

The driver provides full RS485 and RS422 compatibility. When enabled, if DI is high, Y–Z is positive. When the driver is disabled, both outputs are high impedance with less than 10μA of leakage current over the entire common mode range of –7V to 12V, with respect to GND2.

APPLICATIONS INFORMATION

Driver Overvoltage and Overcurrent Protection

The driver outputs are protected from short circuits to any voltage within the absolute maximum range of (V_{CC2} –15V) to (GND2 +15V) levels. The maximum V_{CC2} current in this condition is 250mA. If the pin voltage exceeds about ±10V, current limit folds back to about half of the peak value to reduce overall power dissipation and avoid damaging the part.

The device also features thermal shutdown protection that disables the driver and receiver output in case of excessive power dissipation (See Note 4 in the Electrical Characteristics section).

$\overline{\text{SLO}}$ Mode

The LTM2881 features a logic-selectable reduced slew rate mode ($\overline{\text{SLO}}$ mode) that softens the driver output edges to reduce EMI emissions from equipment and data cables. The reduced slew rate mode is entered by taking the $\overline{\text{SLO}}$ pin low to GND2, where the data rate is limited to about 250kbps. Slew limiting also mitigates the adverse effects of imperfect transmission line termination caused by stubs or mismatched cables.

Figures 9a and 9b show the frequency spectrums of the LTM2881 driver outputs in normal and $\overline{\text{SLO}}$ mode operating at 250kbps. $\overline{\text{SLO}}$ mode significantly reduces the high frequency harmonics.

Receiver and Failsafe

With the receiver enabled, when the absolute value of the differential voltage between the A and B pins is greater than 200mV, the state of RO will reflect the polarity of (A-B). During data communication the receiver detects the state of the input with symmetric thresholds around 0V. The symmetric thresholds preserve duty cycle for attenuated signals with slow transition rates on high capacitive busses, or long cable lengths. The receiver incorporates a failsafe feature that guarantees the receiver output to be a logic-high during an idle bus, when the inputs are shorted, left open or terminated, but not driven. The failsafe feature eliminates the need for system level integration of network pre-biasing by guaranteeing a logic-high on RO under the conditions of an idle bus. Further network biasing constructed to condition transient noise during an idle state is unnecessary due to the common mode transient rejection of the LTM2881. The failsafe detector monitors A and B in parallel with the receiver and detects the state of the bus when A-B is above the input failsafe threshold for longer than about 3μs with a hysteresis of 25mV. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of –7V to 12V.

The receiver output is internally driven high (to V_L) or low (to GND) with no external pull-up needed. When the receiver is disabled the RO pin becomes Hi-Z with leakage of less than ±1μA for voltages within the supply range.

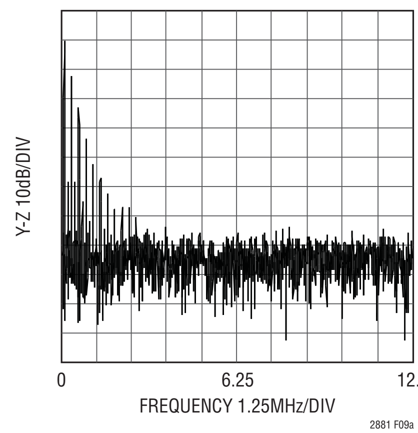


Figure 9a. Frequency Spectrum $\overline{\text{SLO}}$ Mode 125kHz Input

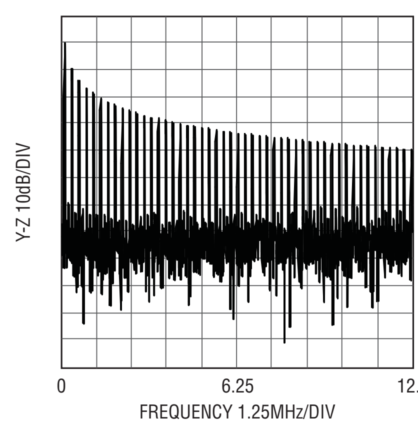


Figure 9b. Normal Mode Frequency Spectrum 125kHz Input

APPLICATIONS INFORMATION

Receiver Input Resistance

The receiver input resistance from A or B to GND2 is greater than 96k permitting up to a total of 256 receivers per system without exceeding the RS485 receiver loading specification. The input resistance of the receiver is unaffected by enabling/disabling the receiver or by powering/unpowering the part. The equivalent input resistance looking into A and B is shown in Figure 10.

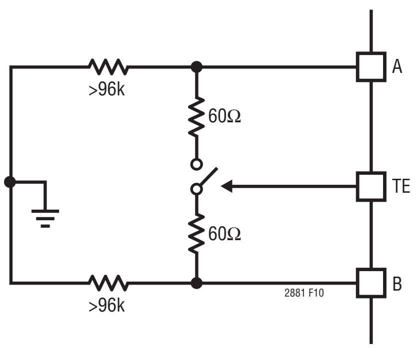


Figure 10. Equivalent Input Resistance into A and B

Switchable Termination

Proper cable termination is very important for signal fidelity. If the cable is not terminated with its characteristic impedance, reflections will distort the signal waveforms.

The integrated switchable termination resistor provides logic control of the line termination for optimal performance when configuring transceiver networks.

When the TE pin is high, the termination resistor is enabled and the differential resistance from A to B is 120Ω. Figure 11 shows the I/V characteristics between pins A and B with the termination resistor enabled and disabled. The resistance is maintained over the entire RS485 common mode range of –7V to 12V as shown in Figure 12. The integrated termination resistor has a high frequency response which does not limit performance at the maximum specified data rate. Figure 13 shows the magnitude and phase of the termination impedance versus frequency. The termination resistor cannot be enabled by TE if the device is unpowered, ON is low or the LTM2881 is in thermal shutdown.

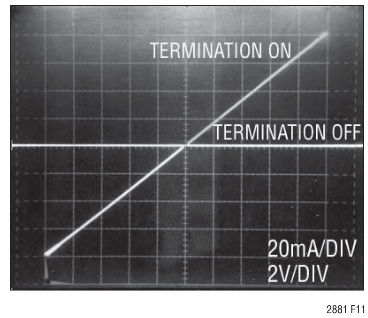


Figure 11. Curve Trace Between A and B with Termination Enabled and Disabled

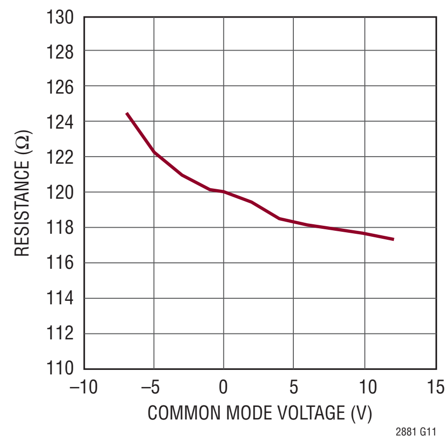


Figure 12. Termination Resistance vs Common Mode Voltage

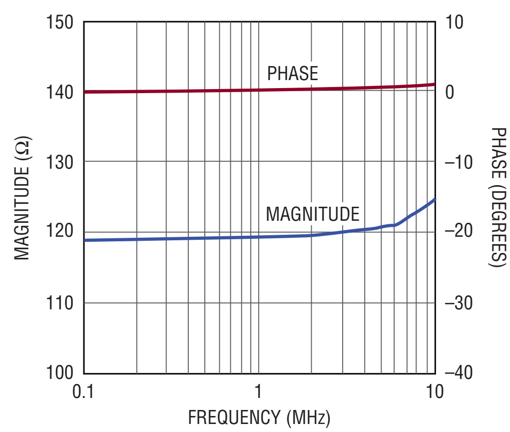


Figure 13. Termination Magnitude and Phase vs Frequency

APPLICATIONS INFORMATION

Supply Current

The static supply current is dominated by power delivered to the termination resistance. Power supply current increases with data rate due to capacitive loading. Figure 14 shows supply current versus data rate for three different loads for the circuit configuration of Figure 4.

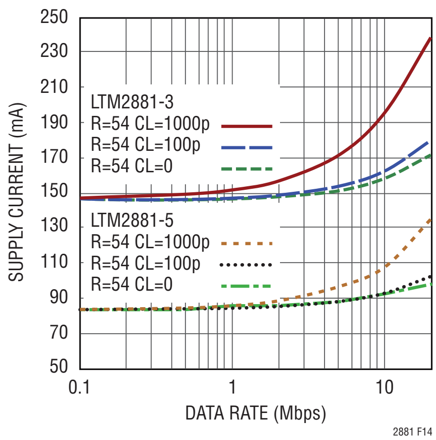


Figure 14. Supply Current vs Data Rate

PCB Layout Isolation Considerations

The high integration of the LTM2881 makes the PCB board layout very simple. However, to optimize its electrical isolation characteristics and thermal performance, some layout considerations are still necessary. Figure 15 is a suggested layout for good thermal performance and to optimize isolation characteristics.

- Use large PCB copper areas for high current paths, including V_{CC}, GND, V_{CC2}, and GND2. It helps to minimize the PCB conduction loss and thermal stress.
- The LTM2881 includes 2.2μF ceramic decoupling capacitors on V_{CC} to GND, V_L to GND, and V_{CC2} to GND2 supply pins. Further decoupling capacitance (10μF) can be added within one-quarter inch away from the V_{CC}, V_L, and/or V_{CC2} pin.
- If the LTM2881 voltage supply is hot plugged without additional protection, damage may occur. Refer to Linear Technology Application Note 88, entitled "Ceramic Capacitors Can Cause Overvoltage Transients" for a detailed discussion of this problem. To protect against hot plug transients use tantalum for aforementioned additional capacitor.
- Do not place copper on the PCB between the inner rows of pads. This area must remain open to withstand the rated isolation voltage. The PCB may also be slotted in this area to insure contamination does not compromise the isolation voltage.

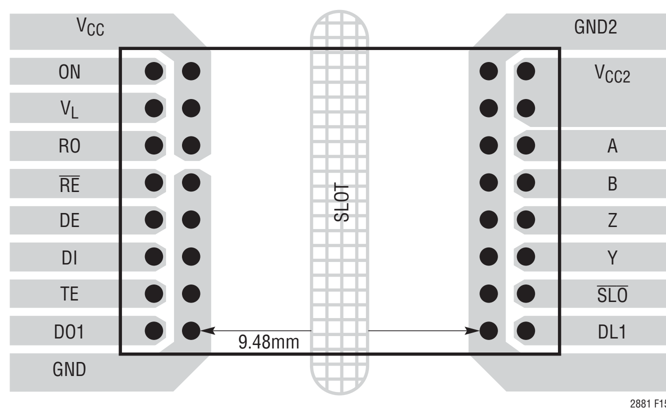


Figure 15. PCB Recommended Layout

APPLICATIONS INFORMATION

Cable Length versus Data Rate

For a given data rate, the maximum transmission distance is bounded by the cable properties. A typical curve of cable length versus data rate compliant with the RS485 standard is shown in Figure 16. Three regions of this curve reflect different performance limiting factors in data transmission. In the flat region of the curve, maximum distance is determined by resistive loss in the cable. The downward sloping region represents limits in distance and rate due to the AC losses in the cable. The solid vertical line represents the specified maximum data rate in the RS485 standard. The dashed line at 250kbps shows the maximum data rate when $\overline{SLO}$ is low. The dashed line at 20Mbps shows the maximum data rate when $\overline{SLO}$ is high.

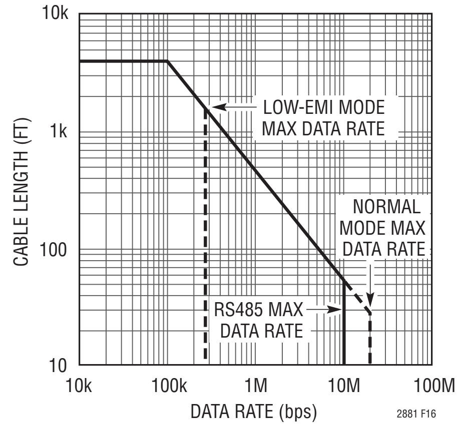
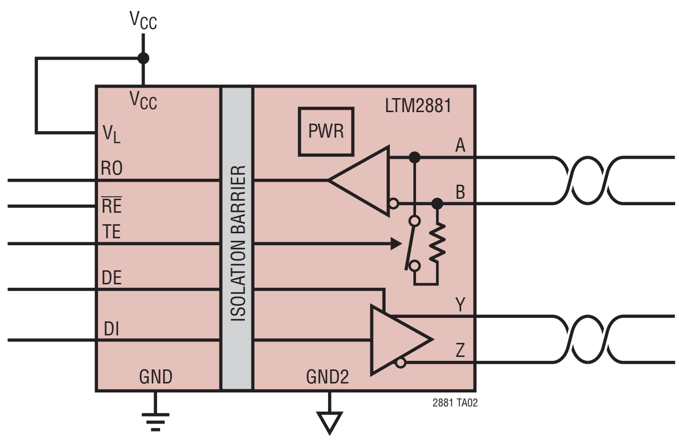


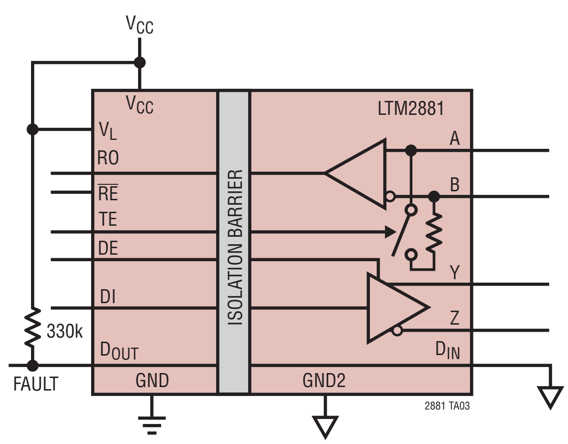
Figure 16. Cable Length vs Data Rate

TYPICAL APPLICATIONS

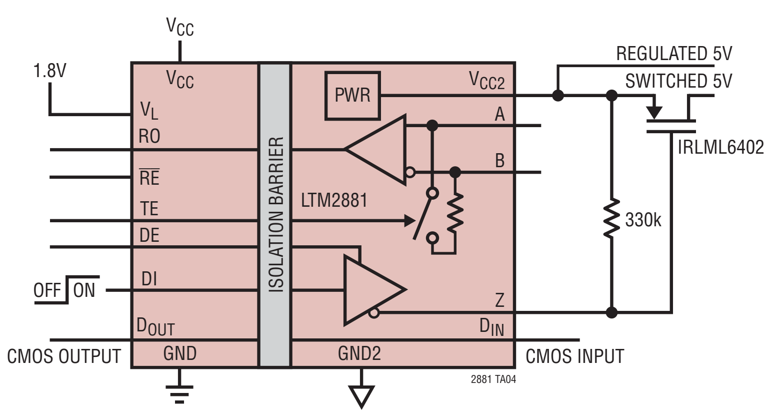
Full-Duplex RS485 Connection



Isolated System Fault Detection

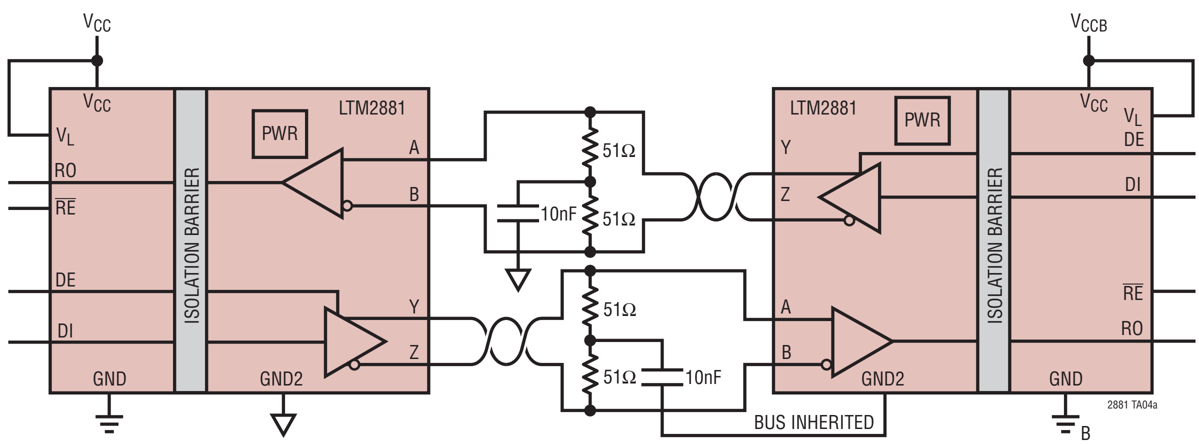


Switched 5V Power with Isolated CMOS Logic Connection with Low Voltage Interface



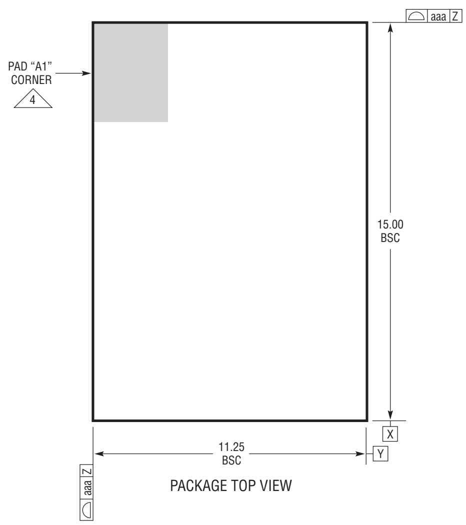
TYPICAL APPLICATIONS

4-Wire Full Duplex Self Biasing for Unshielded CAT5 Connection

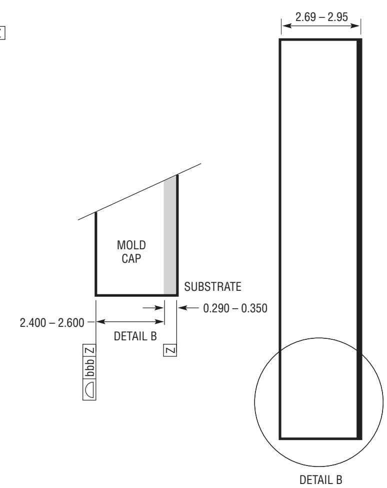


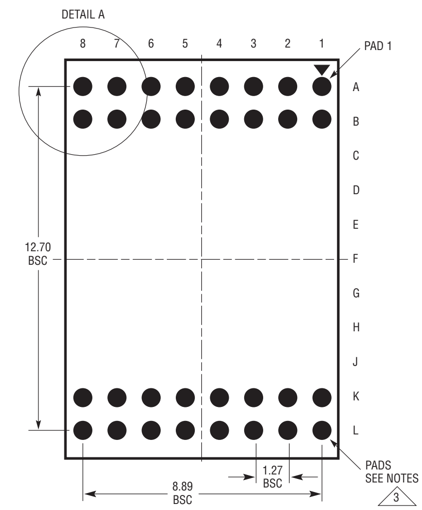
PACKAGE DESCRIPTION

LGA Package
32-Lead (15mm × 11.25mm × 2.8mm)
(Reference LTC DWG # 05-08-1773 Rev θ)

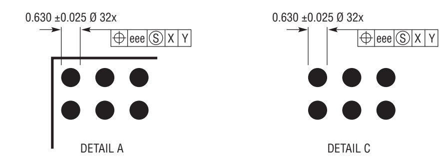


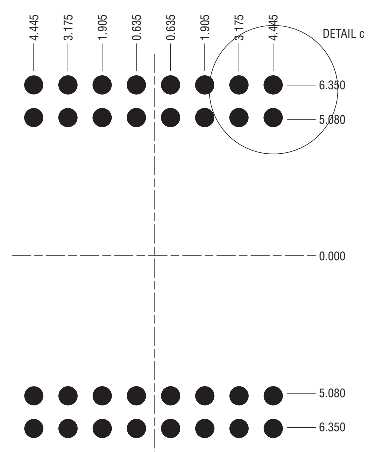
PACKAGE TOP VIEW





PACKAGE BOTTOM VIEW

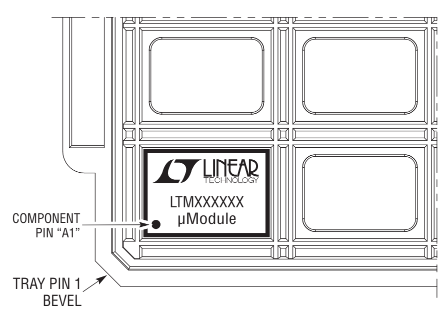




SUGGESTED PCB LAYOUT
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 32

SYMBOL	TOLERANCE
aaa	0.10
bbb	0.10
eee	0.05

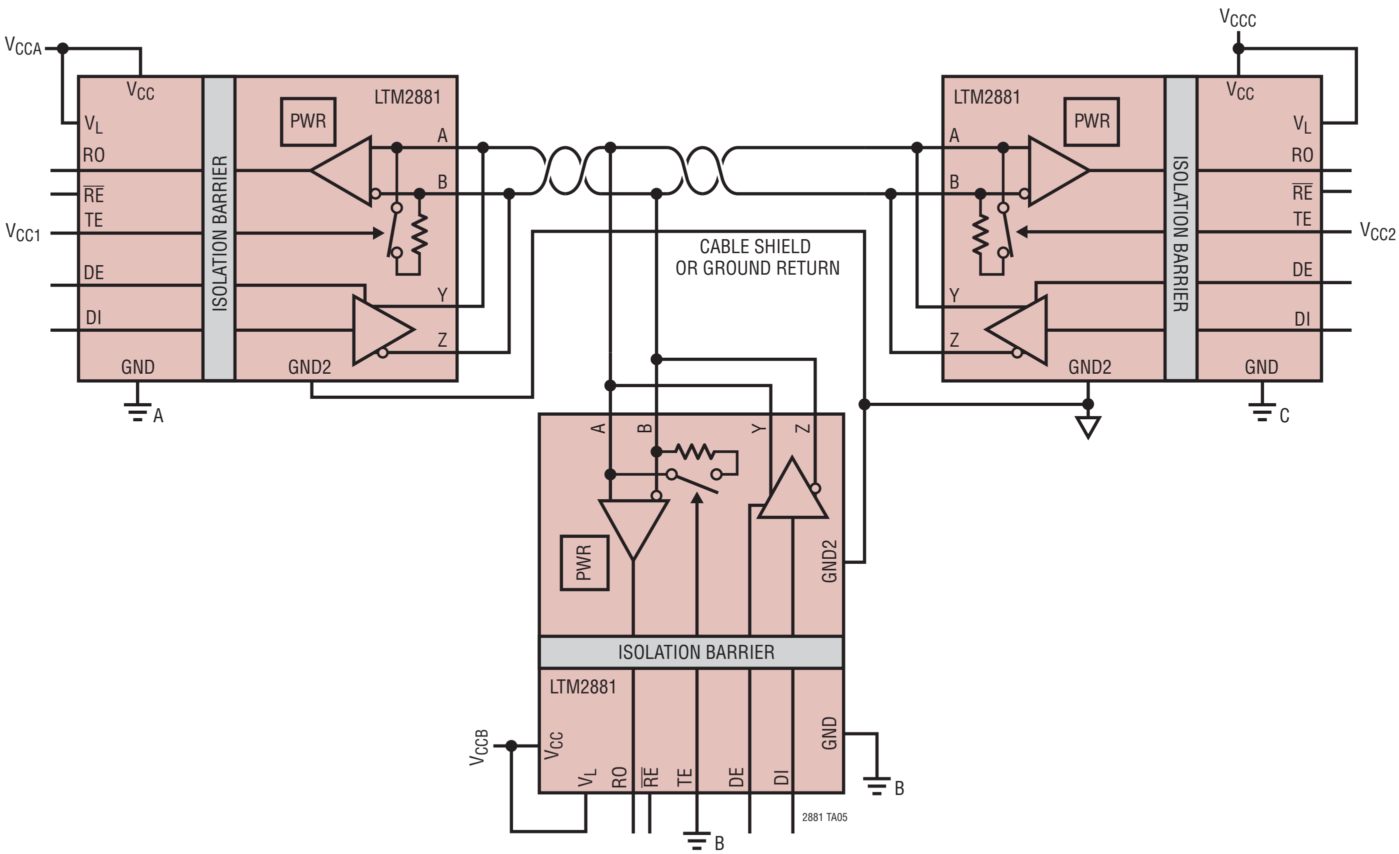


PACKAGE IN TRAY LOADING ORIENTATION

LGA 32 0308 REV Ø

TYPICAL APPLICATION

Multi-Node Network with End Termination and Single Ground Connection on Isolation Bus



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1535	Isolated RS485 Transceiver	2500V_{RMS} Isolation in Surface Mount Package
LT1785	±60V Fault-Protected Transceiver	Half Duplex
LT1791	±60V Fault-Protected Transceiver	Full Duplex
LTC2861	20Mbps RS485 Transceivers with Integrated Switchable Termination	Full Duplex 15kV ESD

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 1109 • PRINTED IN USA