CADEKA
Amplify the Human Experience

SPT7610

6-BIT, 1 GSPS FLASH A/D CONVERTER

JANUARY 21, 2002

FEATURES

- 1:2 demuxed ECL-compatible outputs
- 1.0 GSPS conversion rate
- Wide input bandwidth: 1.4 GHz
- Low input capacitance: 8 pF
- Metastable errors reduced to 1 LSB
- Monolithic construction
- Binary/Two's complement output

APPLICATIONS

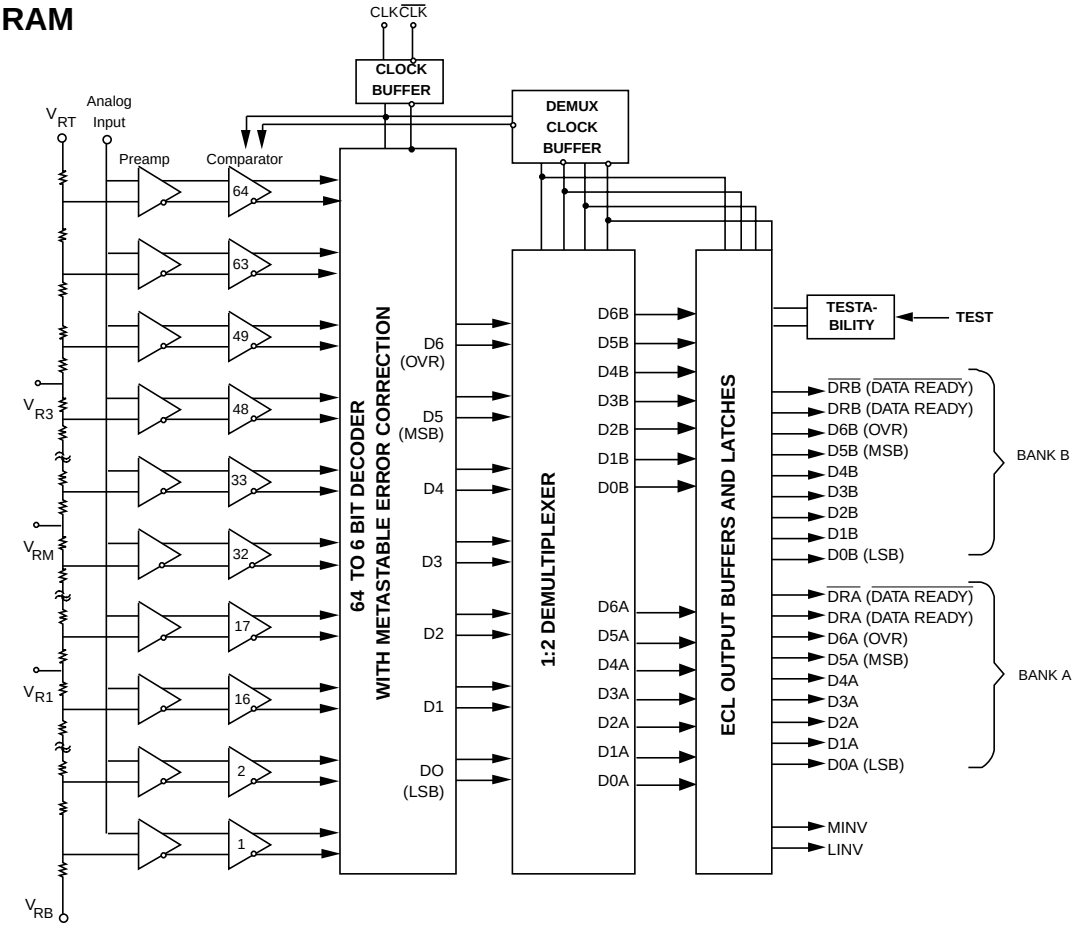
- Radar, EW, ECM
- Direct RF down-conversion
- Microwave modems
- Industrial ultrasound
- Transient capture
- Test and measurement

GENERAL DESCRIPTION

The SPT7610 is a full parallel (flash) analog-to-digital converter capable of digitizing full-scale (0 to –1 V) inputs into six-bit digital words at an update rate of 1 GSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data-ready outputs to ease the task of data capture. The SPT7610's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7610 operates from a single –5.2 V supply, with a nominal power dissipation of 2.75 W.

The SPT7610 is available in a 44L hermetic cerquad surface-mount package in the industrial temperature range (–40 °C to +85 °C).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Negative Supply Voltage (AV_{EE} TO GND) . –7.0 to +0.5 V
Ground Voltage Differential ..... –0.5 to +0.5 V

Input Voltage

Analog Input Voltage ..... +0.5 V to AV_{EE}
Reference Input Voltage ..... +0.5 V to AV_{EE}
Digital Input Voltage ..... +0.5 V to AV_{EE}
Reference Current V_{RT} to V_{RB} ..... +20 mA

Output

Digital Output Current ..... 0 to –25 mA

Temperature

Operating Temperature, Ambient ..... –40 to +85 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, $AV_{EE} = –5.2$ V, $V_{RB} = –1.00$ V, $V_{RM} = –0.5$ V, $V_{RT} = 0.00$ V, f_{CLK} = 1000 MSPS, Duty Cycle = 50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7610 MIN	SPT7610 TYP	SPT7610 MAX	UNITS
Resolution			6			Bits
DC Accuracy						
Integral Linearity		VI	–0.5		+0.5	LSB
Differential Linearity		VI	–0.5		+0.5	LSB
No missing codes		VI		Guaranteed		
Analog Input						
Offset Error V_{RT}		VI	–30		+30	mV
Offset Error V_{RB}		VI	–30		+30	mV
Input Voltage Range		VI	–1		0.0	Volts
Input Capacitance	Over Full Input Range	V		8		pF
Input Resistance		V		50		kΩ
Input Bias Current		VI		200	400	µA
Bandwidth	Small Signal	V		1.4		GHz
Input Slew Rate		V		5		V/ns
Clock Synchronous Input Currents		V		2		µA
Power Supply Requirements						
Supply Current		VI		550	770	mA
Power Dissipation		VI		2.85	4.0	W
Reference Inputs						
Ladder Resistance		VI	60	80	120	Ω
Reference Bandwidth		V		100		MHz
Digital Outputs						
Digital Output High Voltage	R_1 = 50 Ω to –2 V	VI	–1.2	–0.9		Volts
Digital Output Low Voltage	R_1 = 50 Ω to –2 V	VI		–1.8	–1.5	Volts
Digital Inputs						
Digital Input High Voltage (CLK, NCLK)		VI	–1.1		–0.7	Volts
Digital Input Low Voltage (CLK, NCLK)		VI	–2.0		–1.5	Volts
Clock Input Swing (CLK, NCLK)		IV	100	700		mV
Maximum Sample Rate		VI	1000	1200		MSPS
Clock Low Width, TPW0		VI	0.5	0.4		ns
Clock High Width, TPW1		VI	0.5	0.4		ns

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, $AV_{EE} = -5.2$ V, $V_{RB} = -1.00$ V, $V_{RM} = -0.5$ V, $V_{RT} = 0.00$ V, $f_{CLK} = 1000$ MSPS, Duty Cycle = 50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7610 MIN	SPT7610 TYP	SPT7610 MAX	UNITS
Timing Characteristics						
Clock to Data Ready delay (t_{dr})						
Data Bank A	+25 °C case	V		1.68		ns
Data Bank B	+25 °C case	V		1.73		ns
Clock to Output Data (t_{od})						
Data Bank A	+25 °C case	V		2.14		ns
Data Bank B	+25 °C case	V		2.00		ns
Output Data to Data Ready (t_{odr})						
Data Bank A	–40 to 85 °C case	IV		1.54		ns
Data Bank B	–40 to 85 °C case	IV		1.73		ns
Output Data Skew (t_{osk})	–40 to 85 °C case	IV	–150		150	ps
Aperture Jitter		V		2		ps
Acquisition Time		V		250		ps
Dynamic Performance						
Spurious Free Dynamic Range (SFDR)						
f_{IN} = 250 MHz		V		45		dB
f_{IN} = 400 MHz		V		34		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN} = 250 MHz		VI	31	34		dB
f_{IN} = 400 MHz		VI	28	32		dB
Signal to Noise Ratio (SNR)						
f_{IN} = 250 MHz		VI	33	36		dB
f_{IN} = 400 MHz		VI	32	36		dB
Total Harmonic Distortion (THD)						
f_{IN} = 250 MHz		VI		–40	–37	dB
f_{IN} = 400 MHz		VI		–34	–30	dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all test are pulsed tests; therefore, $T_J = T_C = T_A$.

LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

GENERAL OVERVIEW

The SPT7610 is an ultra high-speed monolithic 6-bit parallel flash A/D converter. The nominal conversion rate is 1 GSPS, and the analog bandwidth is typically 1.4 GHz. A major advance over previous flash converters is the inclusion of 64 input preamplifiers between the reference ladder and input comparators. (See the block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators.

The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges. This makes the part easier to drive than previous flash converters. The preamplifiers also add a gain of two to the input signal so that each comparator has a wider overdrive or threshold range to “trip” into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The SPT7610 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise. Signature errors are also reduced by careful layout of the analog circuitry. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Only one –5.2 V power supply is required. Two external references are applied across the internal reference ladder that has a resistance of 80 Ω typical (60 Ω minimum). The top reference is typically 0 V or connected to AGND (analog ground). The device has top force and sense pins (V_{RFT} and V_{RST}) that are internally connected together. These voltage force and sense pins can be used to minimize the voltage drop across the parasitic line resistance.

The bottom reference is typically –1 V. The device also has bottom force and sense pins (V_{RFB} and V_{RSB}) that are internally connected together. These can also be used to minimize the voltage drop across the parasitic line resistance. Three additional reference taps (V_{R3} = –0.25 V typ, V_{RM} = –0.5 V typ, and V_{R1} = –0.75 V typ) are brought out. These taps can be used to control the linearity error.

All logic levels are compatible with both 10K ECL or 100K ECL. It is recommended that the clock input be driven differentially (CLK and NCLK) to improve noise immunity and reduce aperture jitter.

The digital outputs are split into two banks of 6-bit words and an overrange bit. Each bank is updated at 1/2 of the clock rate and is 180° out of phase from the other. The differential data ready signals for each bank are provided to accurately latch each data bank into the register. The output data is in a straight binary, inverted binary, two’s complement or inverted two’s complement format. Figure 1 shows a timing diagram of the device and shows the input-to-output relationship, clock-to-output delay and output latency. The SPT7610 has a built-in offset in the ÷2 clock divider (D Flip-Flop) to assure that output bank A will come up first after power turn on.

Figure 1 – Timing Diagram

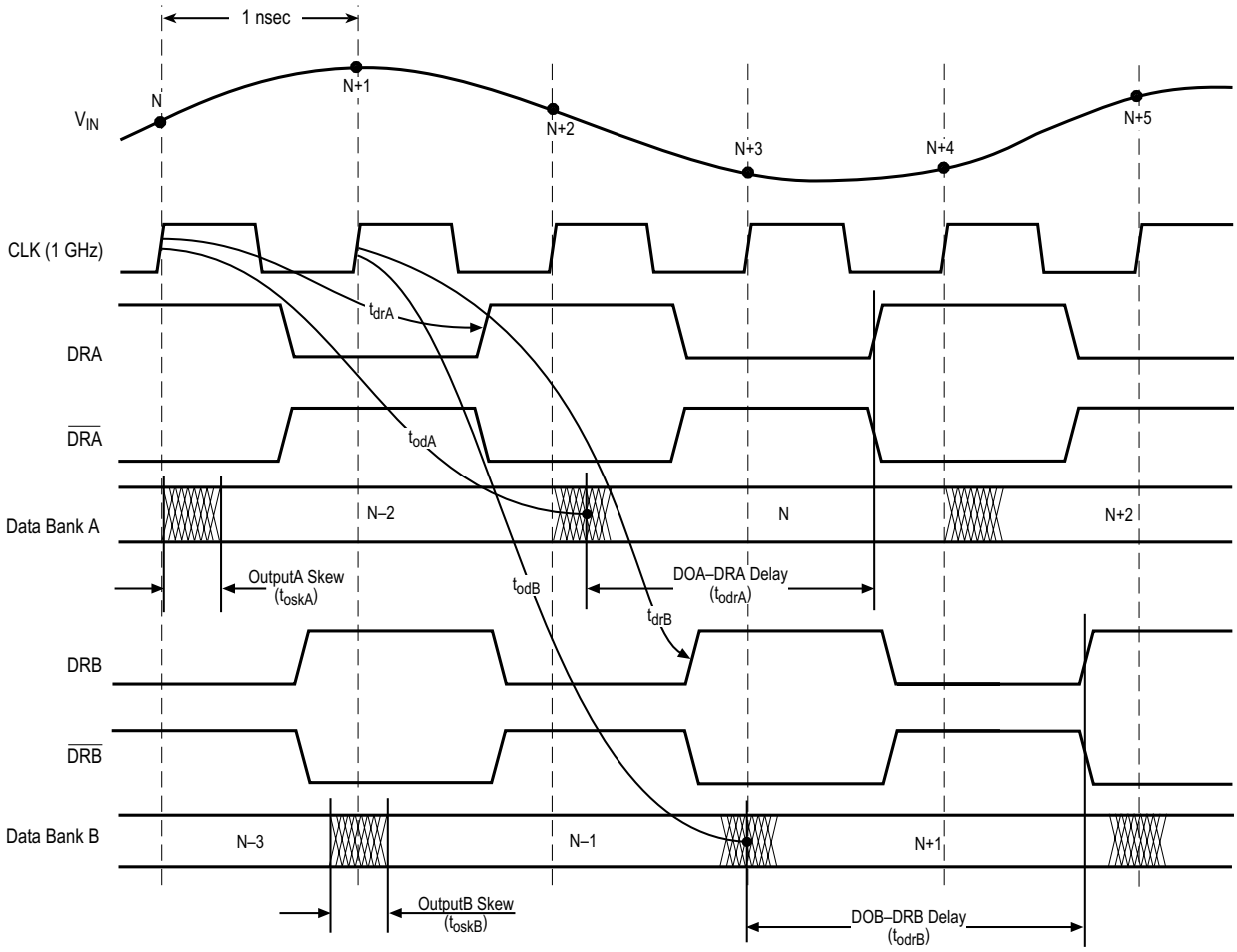


Figure 2 – Test Mode Timing Diagram

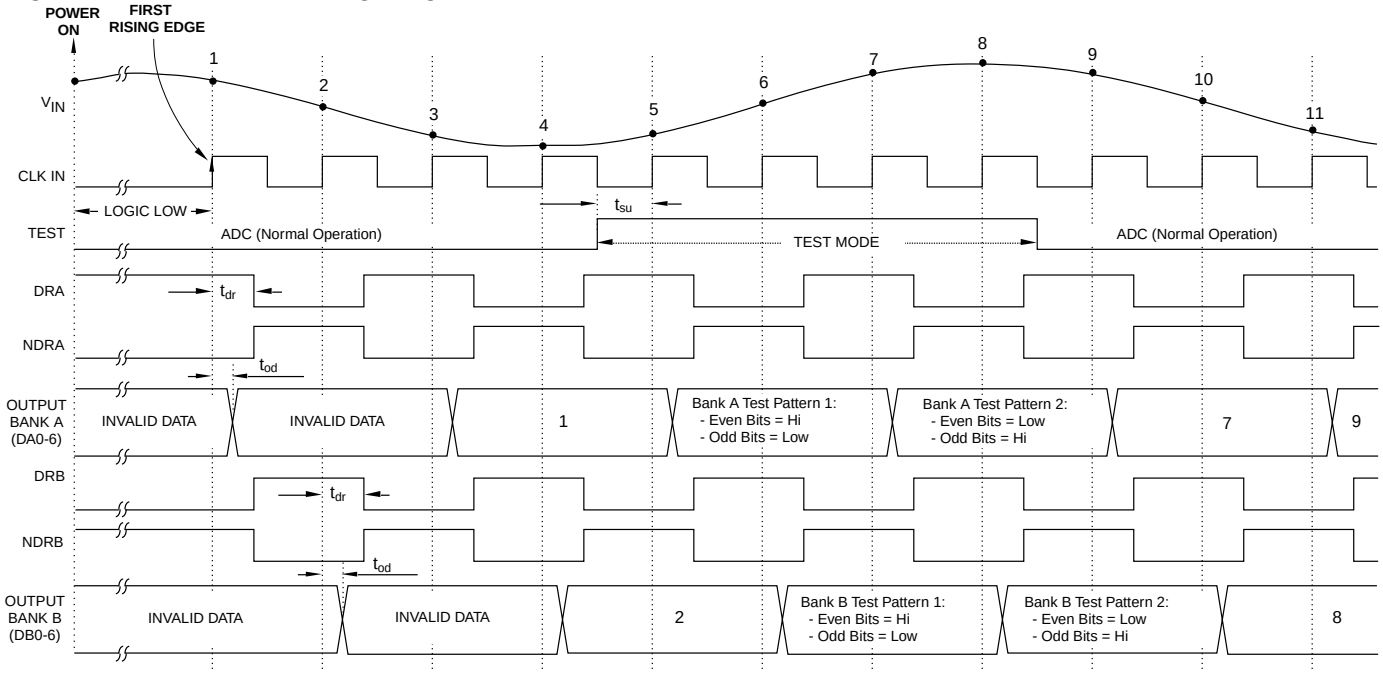
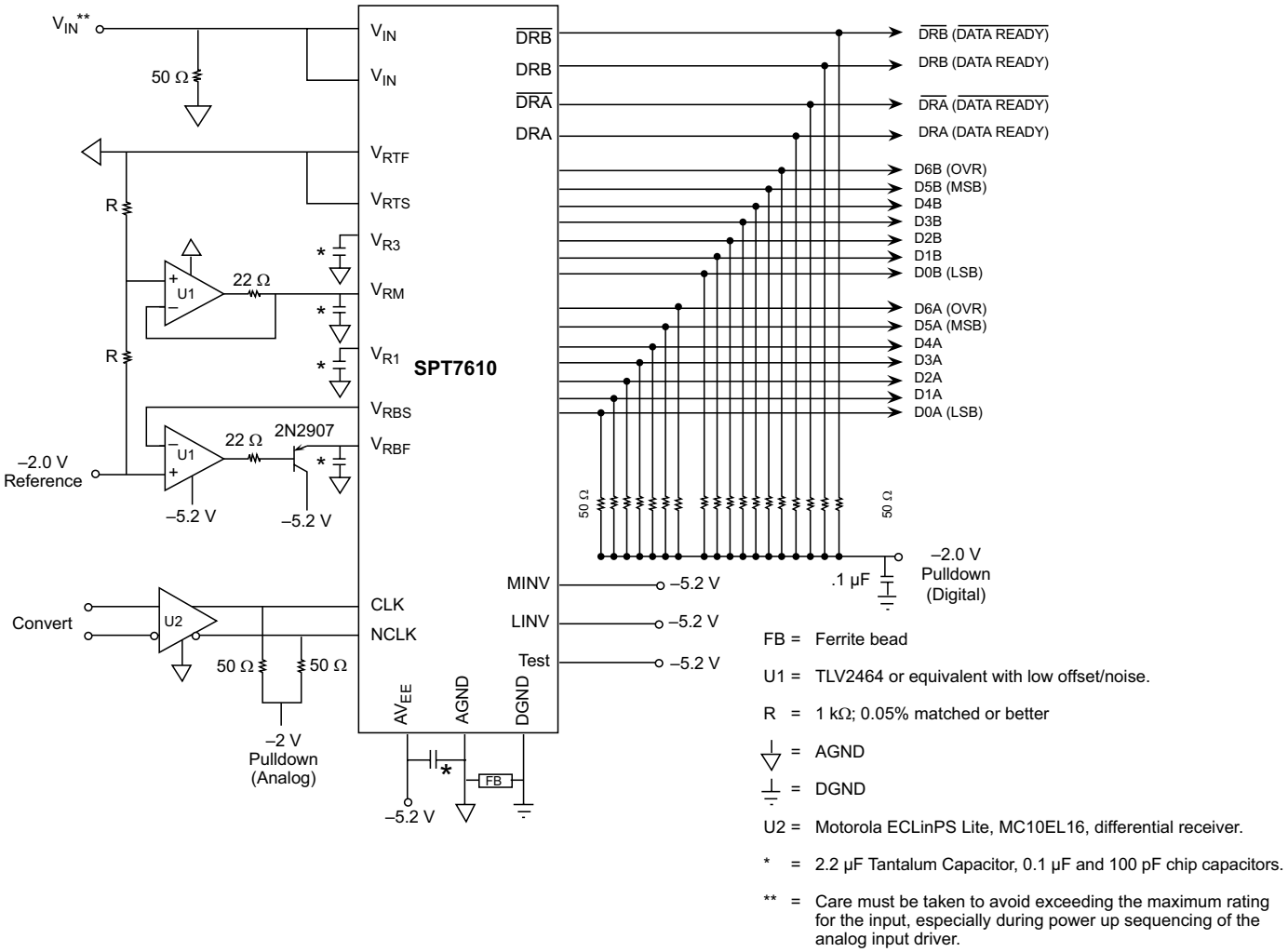


Figure 3 – Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

The typical interface circuit is shown in figure 3. External reference taps are provided for correcting integral nonlinearity errors. These taps can be actively driven to reduce these errors. (See the Reference Inputs discussion below.) The SPT7610 evaluation board application note contains more details on interfacing the SPT7610. The function of each pin and external connections to other components is as follows:

POWER SUPPLY PINS: AV_{EE}, AGND, DGND

AV_{EE} is the supply pin with AGND as ground for the device. The AV_{EE} power supply pin should be bypassed as close to the device as possible with a 10 µF tantalum capacitor, in parallel with 100 pF and .01 µF chip capacitors. Place the 100 pF chip capacitor closest to the SPT7610. Digital ground (DGND) is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 3.

ANALOG INPUT: V_{IN}

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7610 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion.

CLOCK INPUTS: CLK, NCLK

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

DIGITAL OUTPUTS: D0 TO D6, DR, NDR (A AND B)

The digital outputs can drive 50 Ω to ECL levels when pulled down to –2 V. When pulled down to –5.2 V, the outputs can drive 130 Ω to 1 kΩ loads. CADEKA recommends using differential receivers on the outputs of the data ready lines to ensure the proper output rise and fall times.

BINARY AND TWO'S COMPLEMENT OUTPUT: MINV, LINV

Control pins are provided that enable selection of one of four digital output formats. (Table I shows selection of these output formats as a function of the MINV and LINV pins.) When the MINV pin is high, the MSB output is inverted and when it is low, the it is noninverted. Likewise, when the LINV pin is high, the LSB output is inverted and when it is low, the it is noninverted. The user can select either binary, inverted binary, two's complement or inverted two's complement digital output format.

REFERENCE INPUTS: V_{RBF}, V_{RBS}, V_{R1}, V_{RM}, V_{R3}, V_{RTF}, V_{RTS}

There are two reference inputs and three external reference voltage taps. These are –1.0 V V_{RBF} (bottom force) and V_{RBS} (bottom sense), –0.75 V V_{R1} (1/4 tap), –0.5 V V_{RM} (mid-point tap), –0.25 V V_{R3} (3/4 tap) and 0.0 V (AGND) V_{RTF} (top force) and V_{RTS} (top sense). The top reference pin is normally tied to analog ground (AGND) and the bottom reference pin can be driven by an op amp as shown in figure 3.

The reference voltage taps can be used to control integral linearity over temperature. The mid-point reference tap (V_{RM}) is normally driven by an op amp to insure temperature stable operation or may be bypassed for limited temperature operation. The 1/4 (V_{R1}) and 3/4 (V_{R3}) reference ladder taps are typically bypassed to add noise suppression as shown in figure 3 or may be driven with op amps to adjust integral linearity.

SPT7610 TEST MODE FUNCTION: TEST PIN

The SPT7610 supports a special test mode function that overrides the SPT7610's internal data output latch stage and exercises the digital outputs in an alternating test pattern. This enables the user to test digital interface logic downstream from the SPT7610 with a known set of digital test patterns.

Test mode pin 3 controls the SPT7610 mode of operation such that when it is low, the SPT7610 operates in normal mode. When test mode pin 3 is brought high, the SPT7610 will begin to output test pattern 1 (table II) on the next rising edge of the clock. (See figure 2.) It will output the test patterns alternating between test pattern 1 and test pattern 2 as long as test mode pin 3 is held high. The minimum set-up time (t_{su}) can be as low as 0 nsec.

Only the digital output stage is involved in the test mode operation. All ADC stages before the digital output stage continue normal data conversion operation while the test mode is active. When test mode pin 3 is brought back low, the SPT7610 will resume output of valid data on the next rising edge of the clock. The valid data output will correspond to a two-clock-cycle pipeline delay as shown in figure 2.

Table II – SPT7610 Test Mode Output Bit Patterns

	D6	D5	D4	D3	D2	D1	D0
Test Pattern 1	1	0	1	0	1	0	1
Test Pattern 2	0	1	0	1	0	1	0

Table I – Output Coding Table

		BINARY		TWOs COMPLEMENT	
		TRUE	INVERTED	TRUE	INVERTED
		MINV=LINV=0	MINV=LINV=1	MINV=1; LINV=0	MINV=0; LINV=1
ANALOG INPUT VOLTAGE	D6	D_5 ____ D_0	D_5 ____ D_0	D_5 ____ D_0	D_5 ____ D_0
–1 V + 1/2 LSB	0	0 0 0 0 0 0	1 1 1 1 1 1	1 0 0 0 0 0 0	0 1 1 1 1 1 1
	0	0 0 0 0 0 1	1 1 1 1 1 0	1 0 0 0 0 0 1	0 1 1 1 1 1 0
–0.5 V	0	0 1 1 1 1 1 1	1 0 0 0 0 0	1 1 1 1 1 1	0 0 0 0 0 0
		1 0 0 0 0 0	0 1 1 1 1 1	0 0 0 0 0 0	1 1 1 1 1 1
0 V – 1/2 LSB	0	1 1 1 1 1 1	0 0 0 0 0 0	0 1 1 1 1 1	1 0 0 0 0 0
	1	1 1 1 1 1 1	0 0 0 0 0 0	0 1 1 1 1 1	1 0 0 0 0 0
0 V	1	1 1 1 1 1 1	0 0 0 0 0 0	0 1 1 1 1 1	1 0 0 0 0 0

[1] Tie MINV/LINV to GND for logic 1.

[2] Float MINV/LINV for logic 0. (MINV/LINV are internally pulled down to –5.2 V.)

THERMAL MANAGEMENT

Adequate heat sinking and air flow must be provided to keep the die temperature below +150 °C. This device is packaged with the cavity up (the die is on the bottom of the package). Therefore, CADEKA recommends that the device be heat sinked by contacting the bottom of the package through a hole in the circuit board.

The thermal coefficients of the SPT7610 (44L cerquad) are as follows:

θja = +78 °C/W (junction to ambient in still air with no heat sink)

θjc = +4 °C/W (junction to case)

SUBCIRCUIT SCHEMATICS

Figure 3A – Input Circuit

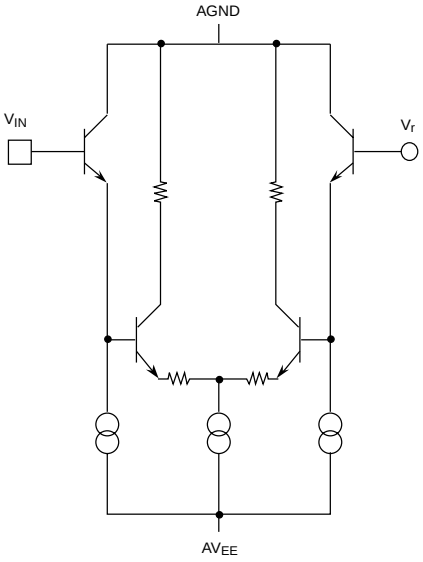


Figure 3B – Output Circuit

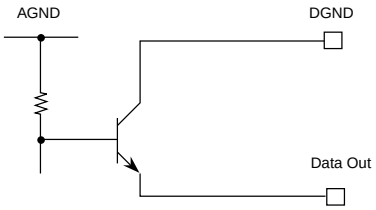
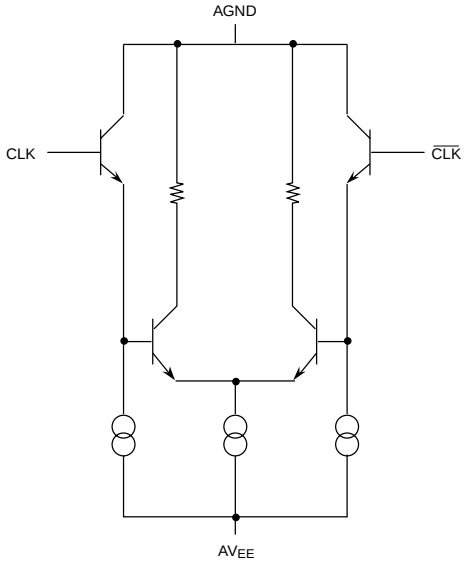
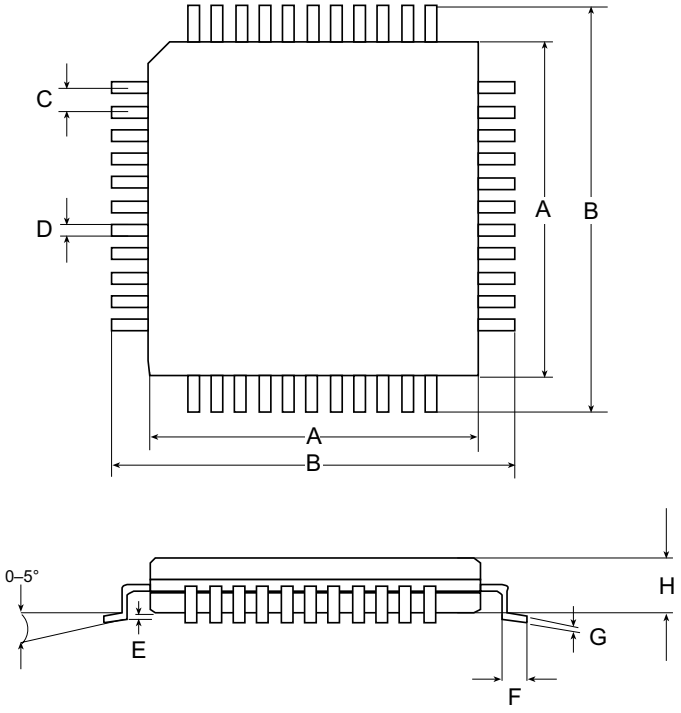


Figure 3C – Clock Input

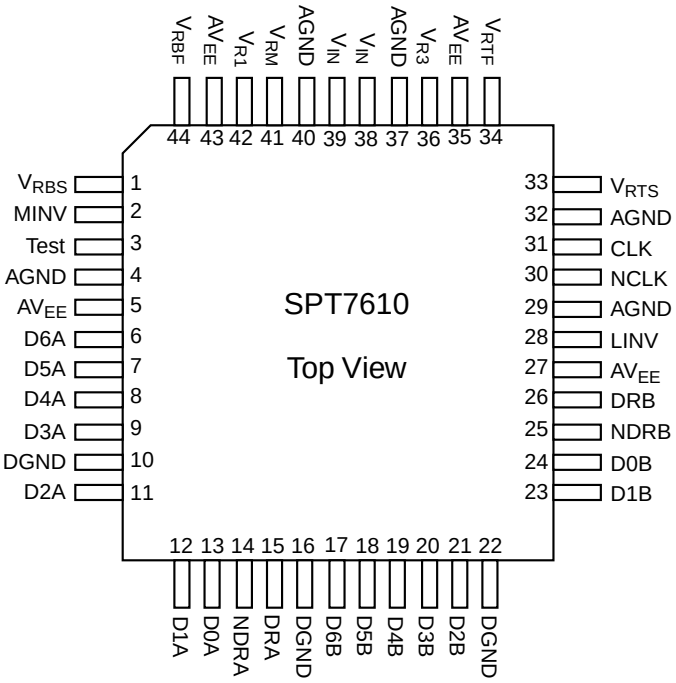


PACKAGE OUTLINE
44-Lead Cerquad



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.551 typ		14.0 typ	
B	0.685	0.709	17.40	18.00
C	0.037	0.041	0.94	1.04
D	0.016 typ		0.41 typ	
E	0.008 typ		0.20 typ	
F	0.027	0.051	0.69	1.30
G	0.006 typ		0.15 typ	
H	0.080	0.150	2.03	3.81

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
AV_{EE}	Negative Supply; nominally –5.2 V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top; nominally 0 V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle; nominally –0.5 V
V_{RBF}	Reference Voltage Force Bottom; nominally –1.0 V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage; can be either Voltage or Sense
DGND	Digital Ground
D0–D5A	Data Output Bank A
D0–D5B	Data Output Bank B
DRA	Data Ready Bank A
NDRA	Not Data Ready Bank A
DRB	Data Ready Bank B
NDRB	Not Data Ready Bank B
D6A	Overrange Output Bank A
D6B	Overrange Output Bank B
CLK	Clock Input
NCLK	Clock Input
MINV	MSB Control Pin
LINV	LSB Control Pin
TEST	Test Control Pin
V_{R1}	Reference Voltage 1/4, nominally –0.75 V
V_{R3}	Reference Voltage 3/4, nominally –0.25 V

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7610SIQ	–40 to +85 °C	44L Cerquad