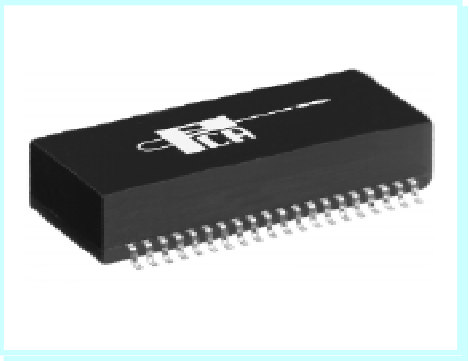
100BX Module for Multi-port Application with Enhanced Common Mode Attenuation

EPF8032S



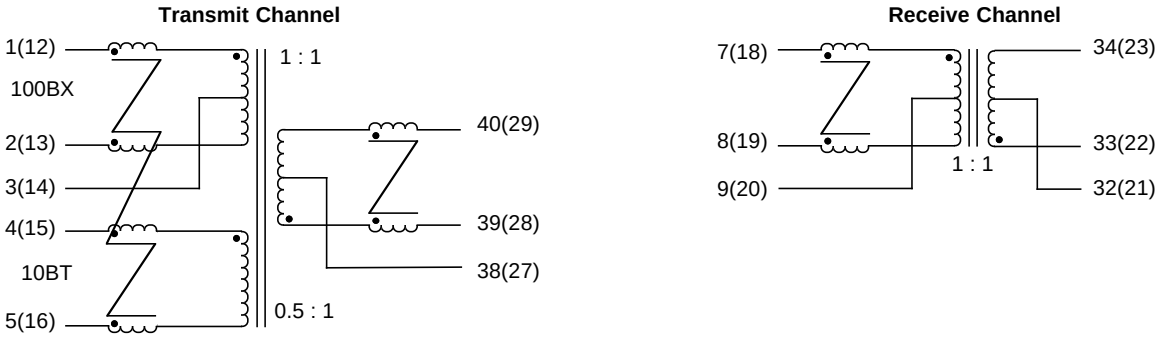
- Optimized for DP83840A/Twister combination
- Recommended for use with ICS1890 series, SSI TSC78Q2120 chips (with appropriate circuitry)
- Guaranteed to operate with 8 mA DC bias at 70°C
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards

Electrical Parameters @ 25° C

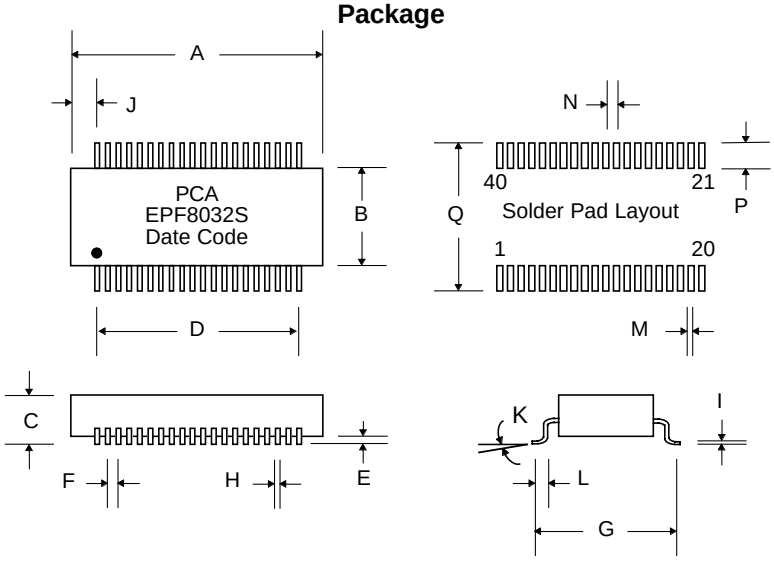
OCL @ 70°C	**Insertion Loss** (dB Max.)						**Return Loss** (dB Min.)						**Common Mode Rejection** (dB Min.)						**Crosstalk** (dB Min.) [Between Channels]	
100 KHz, 0.1 Vrms 8 mA DC Bias	0.1-80 MHz		100 MHz		150 MHz		1-10 MHz		60 MHz		100 MHz		30-100 MHz		200-300 MHz		500 MHz		5-10 MHz	10-100 MHz
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv		
350µH	-1	-1	-1	-1	-3.5	-3	-18	-18	-18	-18	-10	-10	-35	-30	-20	-20	-15	-15	-40	-30

• **Isolation** : 1500 Vrms • **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max. •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	1.110	1.130		28.19	28.70	
B	.470	.490		11.94	12.45	
C	.235	.255		5.97	6.48	
D	.950	Typ.		24.13	Typ.	
E	.008	.012		.203	.305	
F	.050	Typ.		1.27	Typ.	
G	.620	.640		15.75	16.26	
H	.016	.022.		.406	.559	
I	.008	.012		.203	.305	
J	.085	Typ.		2.16	Typ.	
K	0°	8°		0°	8°	
L	.045	Typ.		1.14	Typ.	
M			.030			.762
N			.050			1.27
P			.090			2.29
Q			.670			17.02

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CSF8032Sa Rev. 2 5/16/97

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The circuit below is a guideline for interconnecting PCA's EPF8032S with National DP83840A and DP83223 twister chip set for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes. Please consult PCA for applications help regarding the SSI78Q2120 or ICS1890 series parts or consult with the respective application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the TXREF resistor of the twister chip to get at least 2.12V pk-pk across pins 16-15.
Note that significant low frequency response improvement can be obtained in the system (improving equalization effects) if the DC blocking capacitors were not used; this can only be done by choosing a different pinout for the 10 Base-T receiver side. This is accomplished without impacting any other behavior. If any user has a need to improve this feature, please consult with the PCA Technical support group. Parts similar to EPF8032S are available from several LAN magnetics vendors.

It is recommended that system designers do not ground the receiver side center tap, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

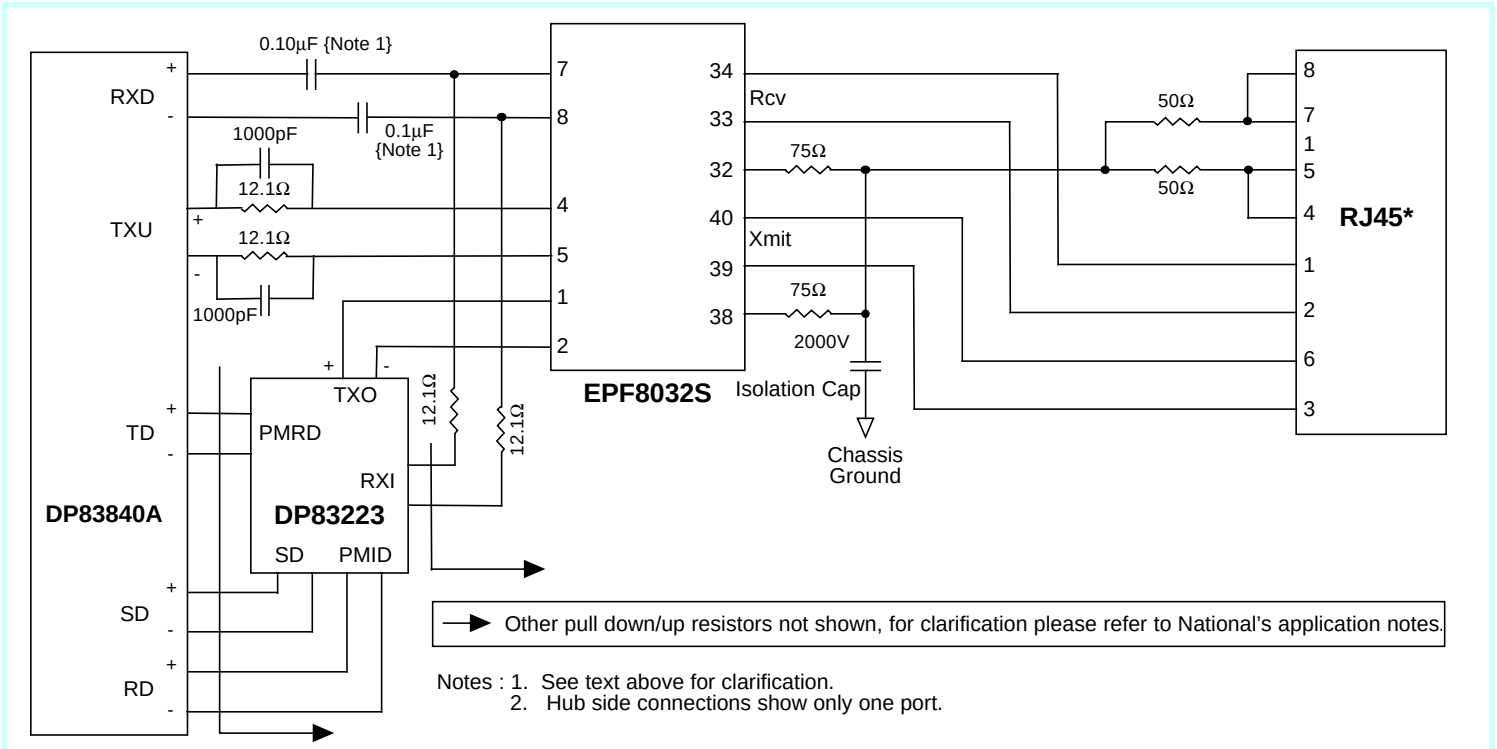
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75 Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8032S. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP (only one port shown)



Notes : 1. See text above for clarification.
2. Hub side connections show only one port.

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