FEATURES

- **Fast 35 ns Read Access & R/W Cycle Time**
- **Directly Replaces Battery-Backed SRAM Modules such as Dallas/Maxim DS1230W**
- **Unlimited Read/Write Endurance**
- **Automatic Non-volatile STORE on Power Loss**
- **Automatic RECALL to SRAM on Power Up**
- **Non-Volatile STORE and RECALL Under Software Control**
- **1 Million STORE Cycles**
- **100-Year Non-volatile Data Retention**
- **Single 3.3V ±0.3V Power Supply**
- **Commercial and Industrial Temperatures**
- **28-pin 600-mil PDIP Package (RoHS-Compliant)**

DESCRIPTION

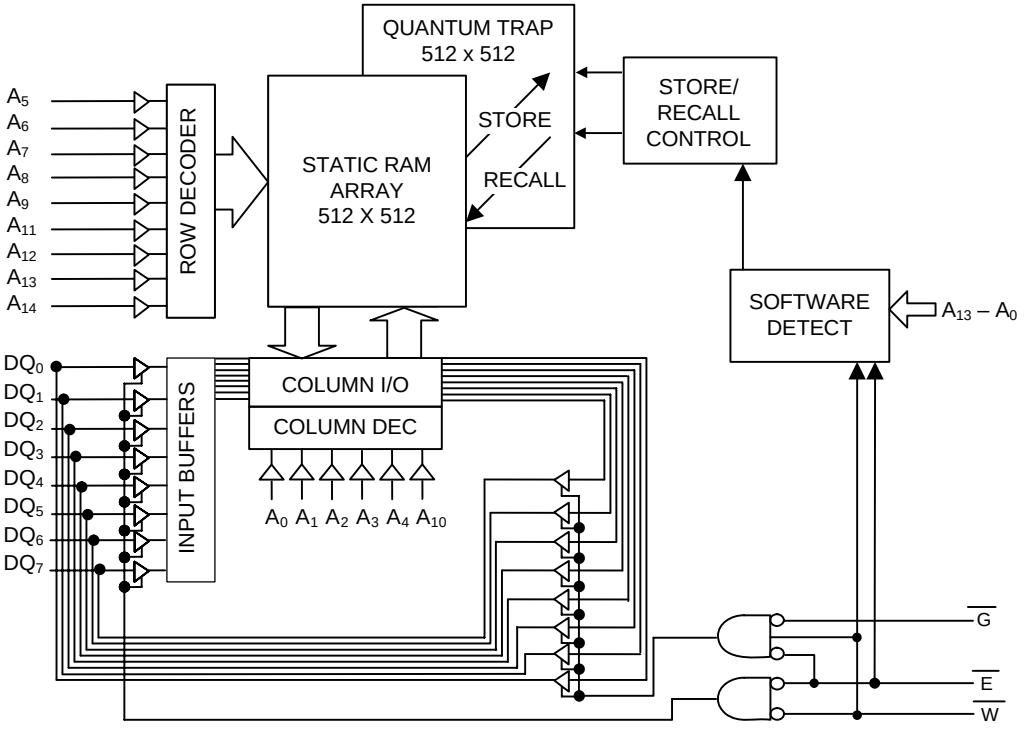
The Simtek STK16C88-3 is a 256Kb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

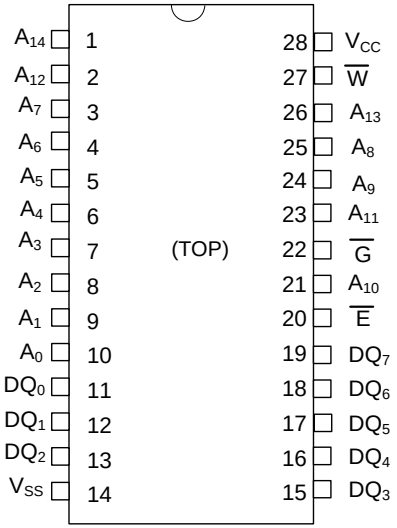
Data transfers automatically to the non-volatile storage cells when power loss is detected (the *STORE* operation). On power up, data is automatically restored to the SRAM (the *RECALL* operation). Both STORE and RECALL operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

BLOCK DIAGRAM



PIN CONFIGURATIONS



28 Pin 600 mil PDIP

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{14}-A_0	Input	Address: The 15 address inputs select one of 32,768 bytes in the nvSRAM array
DQ_7-DQ_0	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tri-state.
V_{CC}	Power Supply	Power: 3.3V, ±0.3V
V_{SS}	Power Supply	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . –0.5V to 4.5V
Voltage on Input Relative to V_{SS} . . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (V_{CC} = 3.0V-3.6V)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}[b]	Average V_{CC} Current		50		52	mA	t_{AVAV} = 35ns
I_{CC2}[c]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 3.3V, 25°C, Typical		8		8	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{SB1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		18		19	mA	t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$
I_{SB2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times . . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[e] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

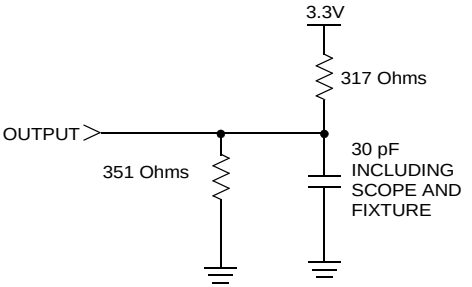


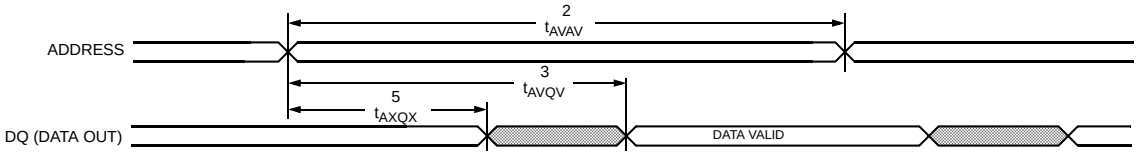
Figure 1: AC Output Loading

SRAM READ CYCLES #1 & #2 (V_{CC} = 3.0V-3.6V)

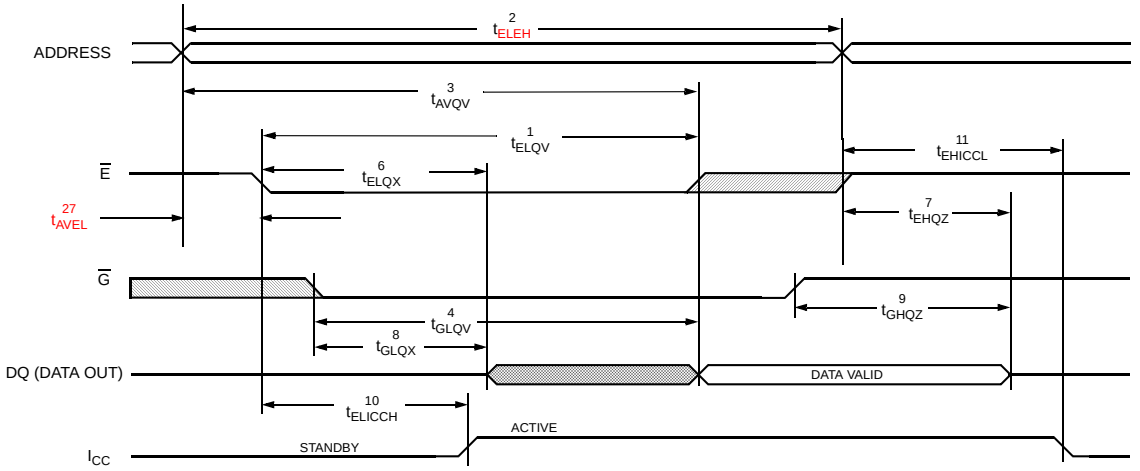
NO.	SYMBOLS		PARAMETER	STK16C88-3-35		UNITS
	#1, #2	Alt.		MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35	ns
2	t_{AVAV}[f], t_{ELEH}[f]	t_{RC}	Read Cycle Time	35		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		35	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		15	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold after Address Change	5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		ns
7	t_{EHQZ}[h]	t_{HZ}	Address Change or Chip Disable to Output Inactive		13	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		13	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		ns
11	t_{EHICCL}[d, e]	t_{PS}	Chip Disable to Power Standby		35	ns

Note f: $\overline{W}$ must be high during SRAM READ cycles and low during SRAM WRITE cycles.
Note g: I/O state assumes $\overline{E}$, $\overline{G} \le V_{IL}$ and $\overline{W} \ge V_{IH}$; device is continuously selected.
Note h: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[f, g]



SRAM READ CYCLE #2: $\overline{E}$ and $\overline{G}$ Controlled[f]

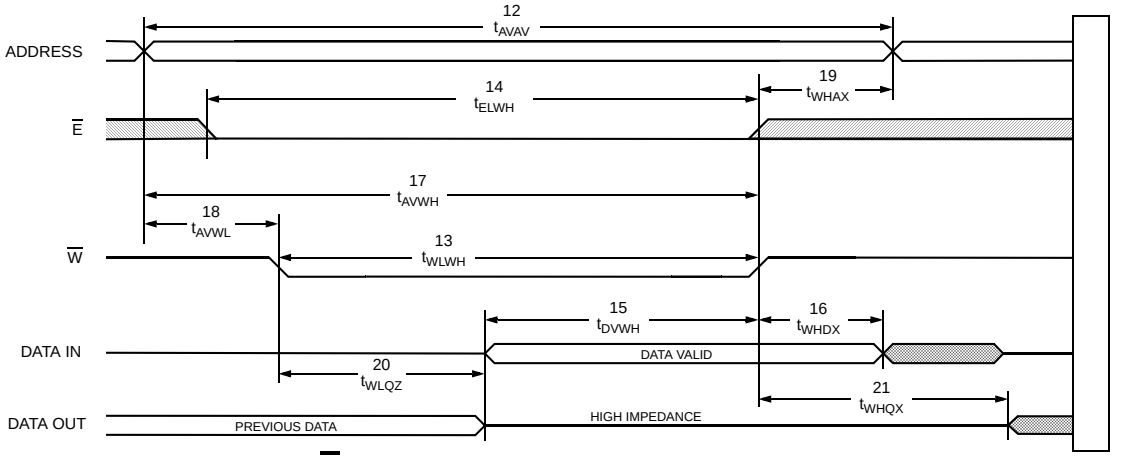


SRAM WRITE CYCLES #1 & #2 (V_{CC} = 3.0V-3.6V)

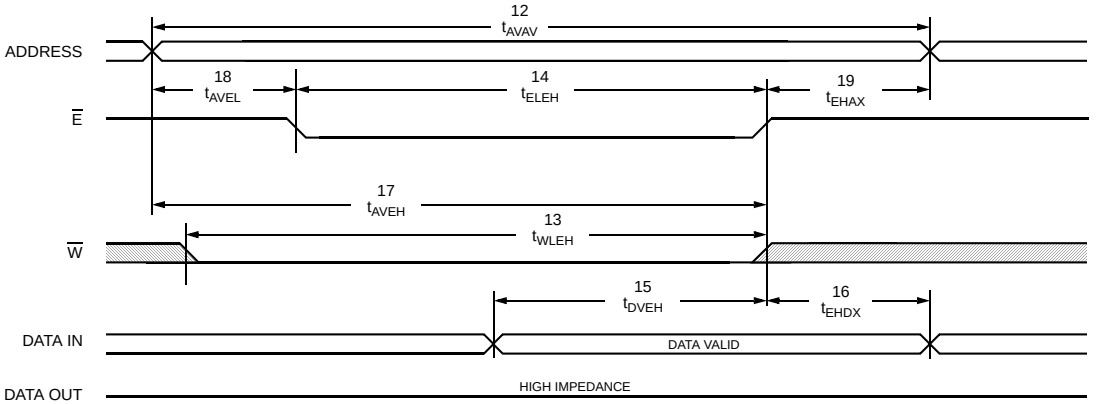
NO.	SYMBOLS			PARAMETER	STK16C88-3-35		UNITS
	#1	#2	Alt.		MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	35		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	25		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	25		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	12		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	25		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		ns
20	t_{WLQZ} [h, i]		t_{WZ}	Write Enable to Output Disable		13	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[j]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[j]

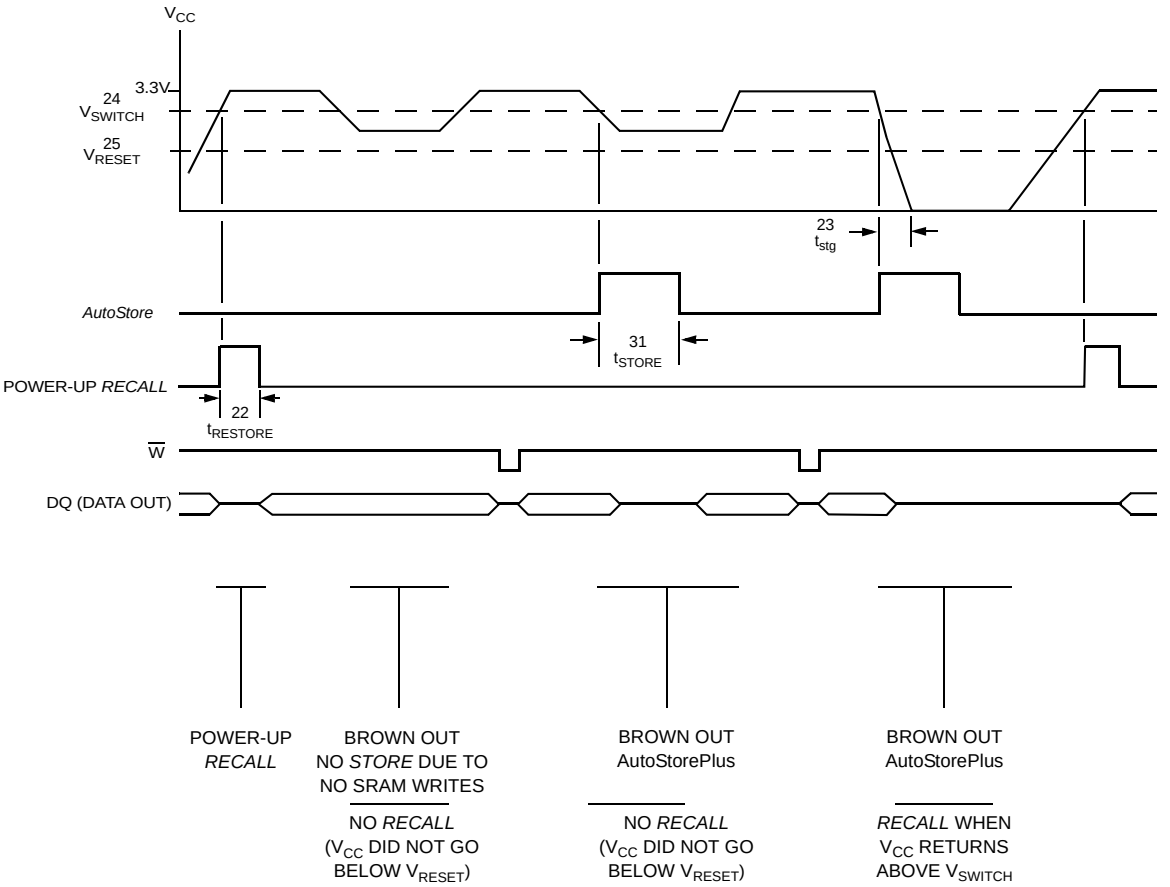


AutoStorePlus/POWER-UP *RECALL* (V_{CC} = 3.0V-3.6V)

NO.	SYMBOLS	PARAMETER	STK16C88-3		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up *RECALL* Duration		550	µs	k
23	t_{stg}	Minimum V_{CC} Slew Time to Ground	500		ns	e, g
24	V_{SWITCH}	Low Voltage Trigger Level	2.7	2.95	V	
25	V_{RESET}	Low Voltage Reset Level		2.4	V	e

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

AutoStorePlus/POWER-UP *RECALL*



SOFTWARE *STORE/RECALL* MODE SELECTION

$\overline{E}$	$\overline{W}$	A_{13} - A_0 (hex)	MODE	I/O	NOTES
L	H	0E38	Read SRAM	Output Data	l, m
		31C7	Read SRAM	Output Data	
		03E0	Read SRAM	Output Data	
		3C1F	Read SRAM	Output Data	
		303F	Read SRAM	Output Data	
		0FC0	Nonvolatile *STORE*	Output High Z	
L	H	0E38	Read SRAM	Output Data	l, m
		31C7	Read SRAM	Output Data	
		03E0	Read SRAM	Output Data	
		3C1F	Read SRAM	Output Data	
		303F	Read SRAM	Output Data	
		0C63	Nonvolatile *RECALL*	Output High Z	

Note l: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive $\overline{E}$ controlled cycles to enable a nonvolatile cycle.

Note m: While there are 15 addresses on the STK16C88-3, only the lower 14 are used to control software modes.

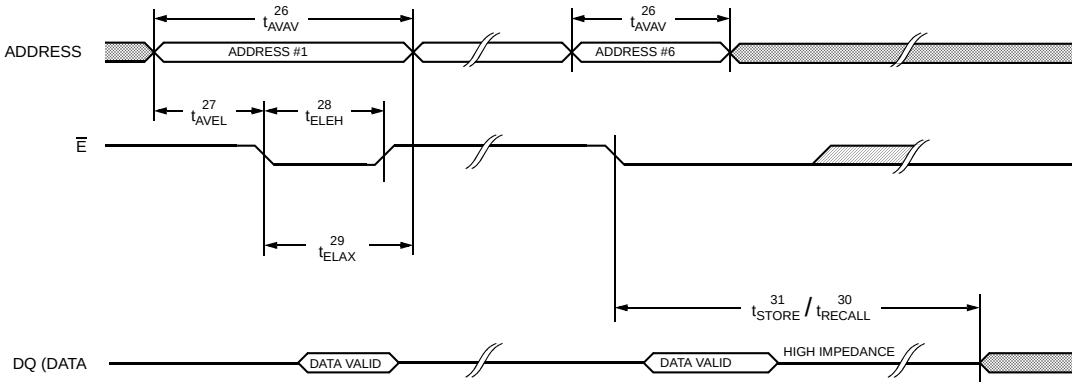
SOFTWARE *STORE/RECALL* CYCLE[n, o] (V_{CC} = 3.0V-3.6V)

NO.	SYMBOLS	PARAMETER	STK16C88-3-35		UNITS
			MIN	MAX	
26	t_{AVAV}	*STORE*/*RECALL* Initiation Cycle Time	35		ns
27	t_{AVEL}[n]	Address Set-up Time	0		ns
28	t_{ELEH}[n]	Clock Pulse Width	25		ns
29	t_{ELAX}[g, n]	Address Hold Time	20		ns
30	t_{RECALL}	*RECALL* Cycle Duration		20	µs
31	t_{STORE}	*STORE* Cycle Duration		10	ms

Note n: The software sequence is clocked on the falling edge of $\overline{E}$ controlled Reads without involving G (double clocking will abort the sequence). See application note: MA0002 http://www.simtek.com(/attachments/AppNote02.pdf.

Note o: The six consecutive addresses must be in the order listed in the Software *STORE*/*RECALL* Mode Selection Table: (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a *STORE* cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE/RECALL* CYCLE: $\overline{E}$ Controlled[o]



nvSRAM OPERATION

The AutoStore+ STK16C88-3 is a fast 32K x 8 SRAM that does not lose its data on power-down. The data is preserved in integral Quantum Trap nonvolatile storage elements when power is lost. Automatic STORE on power-down and automatic RECALL on power-up guarantee data integrity without the use of batteries.

NOISE CONSIDERATIONS

Note that the STK16C88-3 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK16C88-3 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore+ OPERATION

The STK16C88-3's automatic STORE on power-down is completely transparent to the system. The STORE initiation takes less than 500ns when power is lost (V_{CC} < V_{SWITCH}) at which point the part depends only on its internal capacitor for *STORE* completion.

If the power supply drops faster than 20µs/volt before Vcc reaches Vswitch, then a 1 ohm resistor should be inserted between Vcc and the system supply to avoid a momentary excess of current between Vcc and internal capacitor.

In order to prevent unneeded *STORE* operations, automatic *STORE*s will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether or not a WRITE operation has taken place.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CC} < V_{RESET}), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK16C88-3 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10kΩ resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

SOFTWARE NONVOLATILE *STORE*

The STK16C88-3 software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. During the *STORE* cycle, previous nonvolatile data is erased and then the SRAM contents are written to the nonvolatile storage elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0FC0 (hex)	Initiate *STORE* cycle

The software sequence must be clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of READ operations must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0C63 (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile storage elements. The nonvolatile data can be recalled an unlimited number of times.

HARDWARE PROTECT

The STK16C88-3 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When V_{CC} < V_{SWITCH}, all software *STORE* operations and SRAM WRITEs are inhibited.

LOW AVERAGE ACTIVE POWER

The STK16C88-3 draws significantly less current when it is cycled at rates slower than 35ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 3.6V, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK16C88-3 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

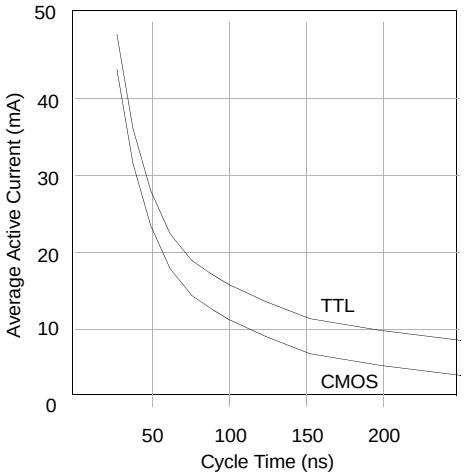


Figure 2: I_{CC} (max) Reads

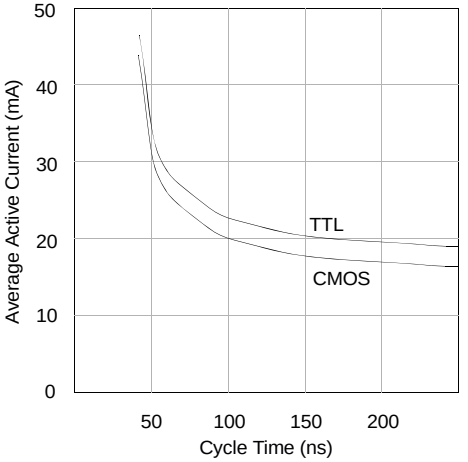


Figure 3: I_{CC} (max) Writes

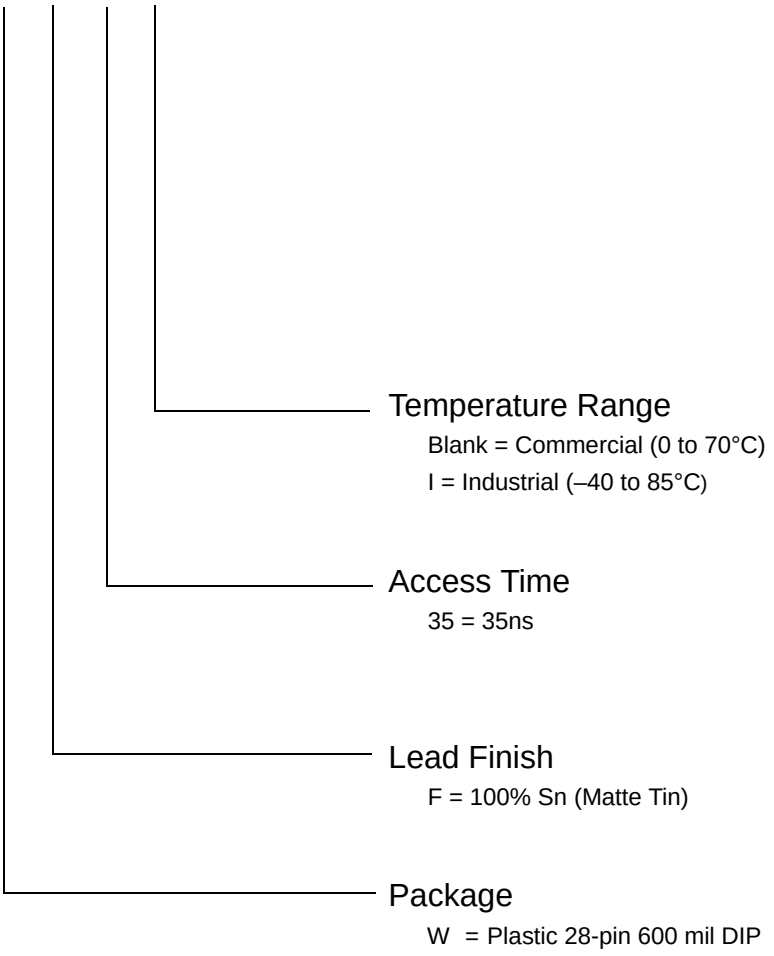
BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).

ORDERING INFORMATION

STK16C88-3 W F 35 I

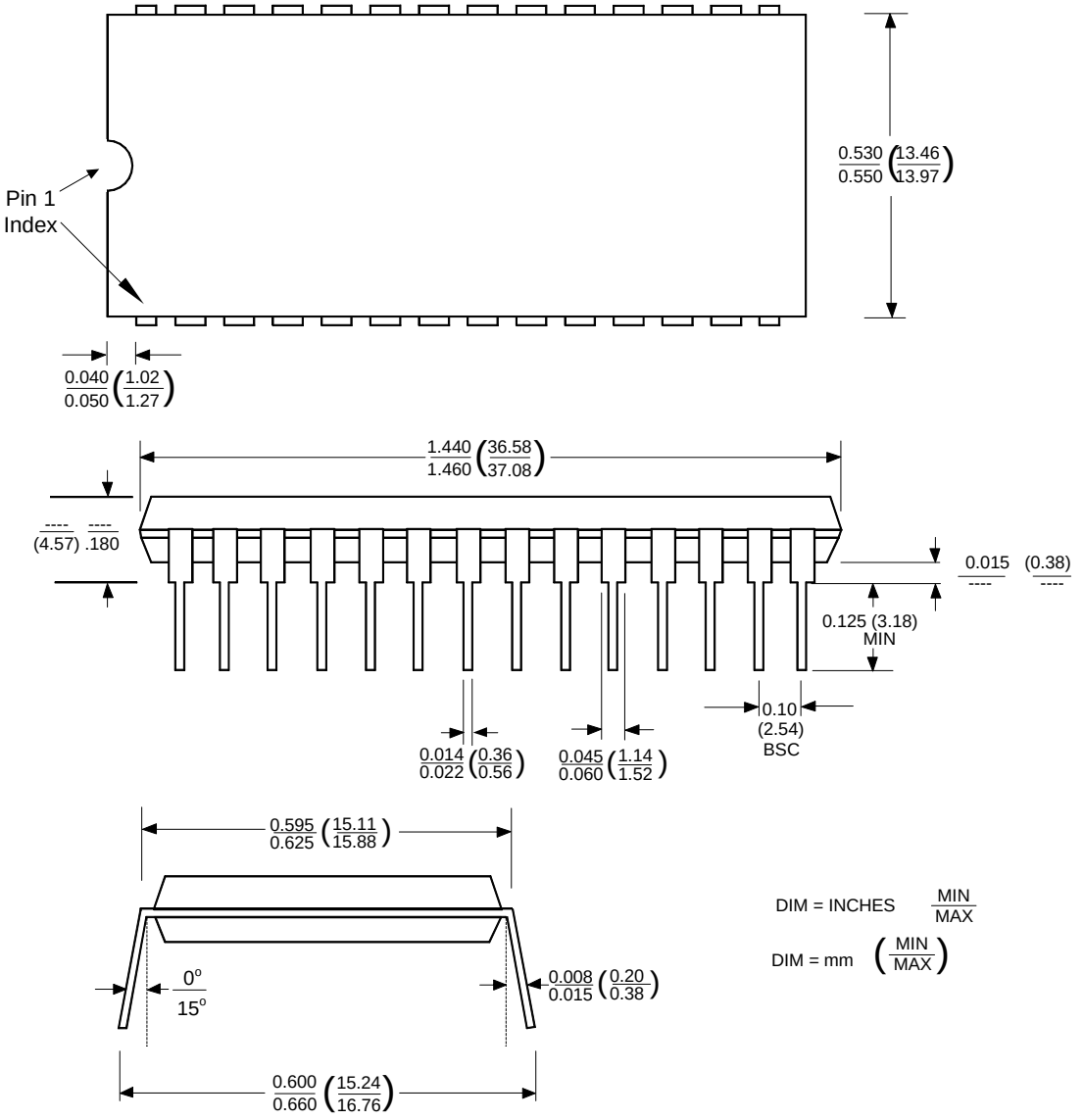


ORDERING CODES

Part Number	Description	Access Times	Temperature
STK16C88-3WF35	3.3V 32Kx8 AutoStore+ nvSRAM PDIP28-600	35 ns access times	Commercial
STK16C88-3WF35I	3.3V 32Kx8 AutoStore+ nvSRAM PDIP28-600	35 ns access times	Industrial

PACKAGE DRAWING

28 Pin 600 mil PDIP



Document Revision History

Revision	Date	Summary
0.0	December 2002	
0.1	September 2003	Added lead-free lead finish
0.2	March 2006	Removed 45ns and 55ns speed grades, Removed Leaded lead finish.
0.3	February 2007	Add fast power-down slew rate information Add Product Ordering Code Listing Add Package Drawings Reformat Entire Document
2.0	January 2008	Extend definition of t_{HZ} (#7) Page 4: updated the SRAM READ CYCLE #2 figure, SRAM WRITE CYCLE #1 figure, Note l, and Note n to clarify product usage Page 10: added best practices section. Page 11: added access times column to the Ordering codes.

SIMTEK STK16C88-3 Datasheet, January 2008