Low Cost, 60MHz Rail-to-Rail Input-Output Op-Amp

The ISL24020 is a low power, high voltage rail-to-rail input-output amplifier. Operating on supplies ranging from 5V to 15V, while consuming only 2.5mA per amplifier, the ISL24020 has a bandwidth of 60MHz (-3dB). It also provides common mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables the amplifier to offer maximum dynamic range at any supply voltage.

The ISL24020 also features fast slewing and settling times, as well as a high output drive capability of 65mA (sink and source). These features make the ISL24020 ideal for high speed filtering and signal conditioning application. Other applications include battery power, portable devices, and anywhere low power consumption is important.

The ISL24020 is available in 5 Ld TSOT package. It features a standard operational amplifier pinout and operats over a temperature range of -40°C to +85°C.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
ISL24020IHTZ-T7* (Note)	BCBA	5 Ld TSOT (Pb-free)	MDP0049

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

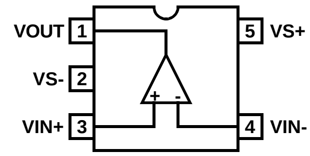
- Pb-free (RoHS compliant)
- 60MHz (-3dB) bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 2.5mA
- High slew rate = 75V/µs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- ±180mA output short current

Applications

- TFT-LCD panels
- V_{COM} amplifiers
- Drivers for A/D converters
- Data acquisition
- Video processing
- Audio processing
- Active filters
- Test equipment
- Battery-powered applications
- Portable equipment

Pinout

ISL24020
(5 LD TSOT)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . .+18V
Input Voltage . . . . V_S- - 0.5V, V_S +0.5V
Maximum Continuous Output Current 65mA
Maximum Die Temperature . . . .+150°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
5 Lead TSOT 215
Storage Temperature . . . .-65°C to +150°C
Ambient Operating Temperature . . . .-40°C to +85°C
Power Dissipation . . . . See Curves
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications V_S+ = +5V, V_S- = -5V, R_L = 1kΩ to 0V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 2)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	$-4.5V \le V_{OUT} \le 4.5V$	62	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.92	-4.85	V
V_{OH}	Output Swing High	I_L = 5mA	4.85	4.92		V
I_{SC}	Short-Circuit Current			±180		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current	No load		2.5	4.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$-4.0V \le V_{OUT} \le 4.0V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
d_G	Differential Gain (Note 4)	$R_F = R_G$ = 1kΩ and V_{OUT} = 1.4V		0.17		%
d_P	Differential Phase (Note 4)	$R_F = R_G$ = 1kΩ and V_{OUT} = 1.4V		0.24		°

NOTES:

2. Measured over operating temperature range.
3. Slew rate is measured on rising and falling edges.
4. NTSC signal generator used.

Typical Performance Curves

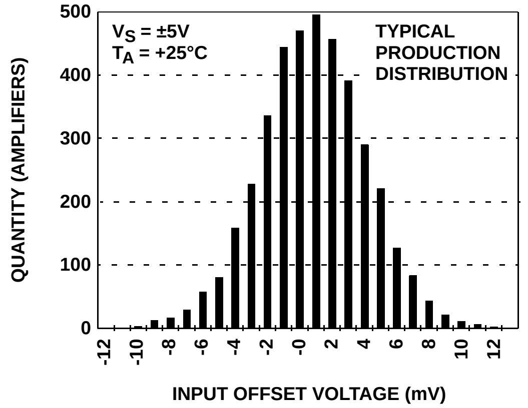


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

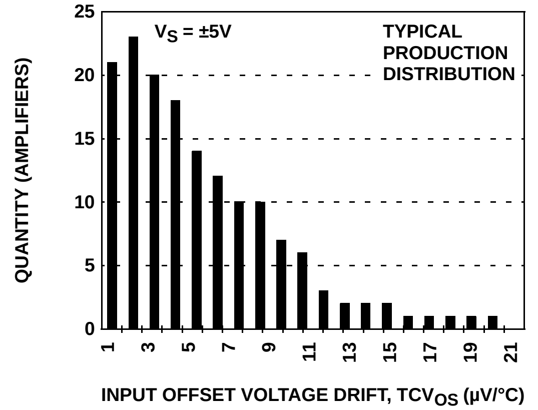


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

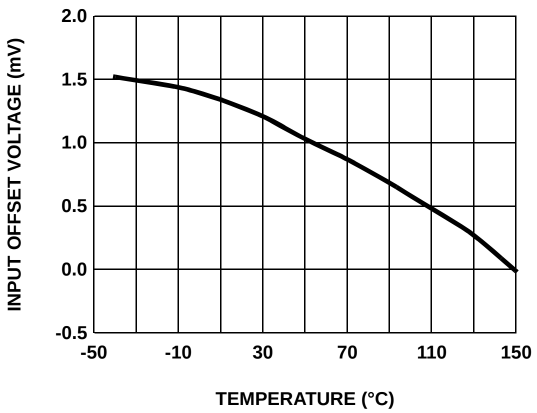


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

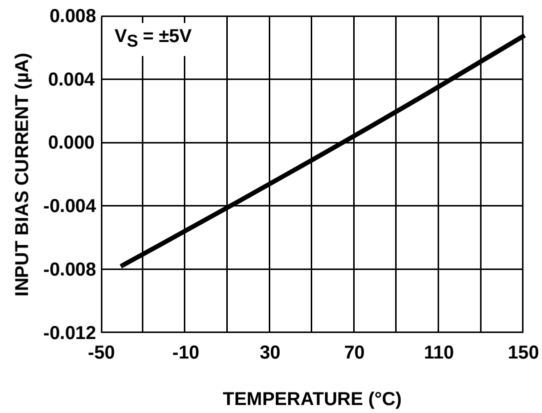


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

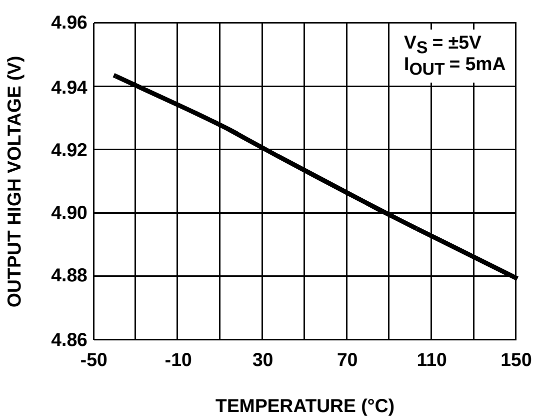


FIGURE 5. OUTPUT HIGH VOLTAGE vs TEMPERATURE

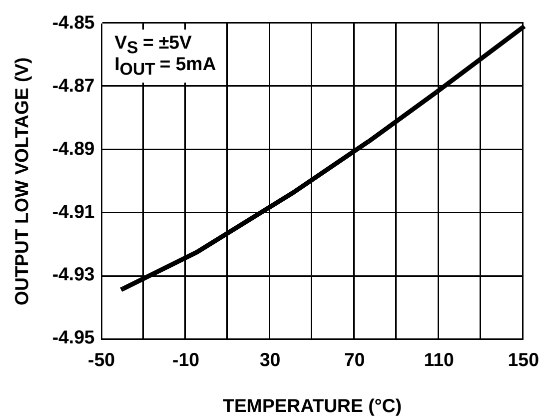


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

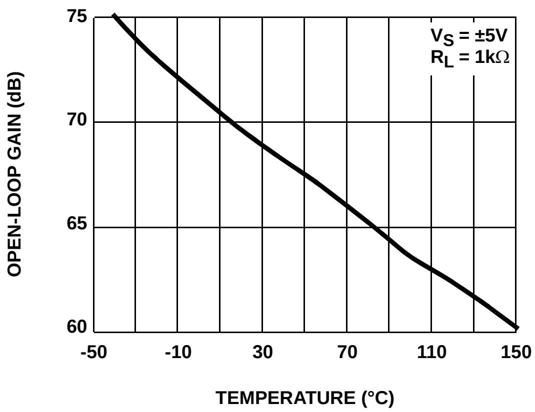


FIGURE 7. OPEN-LOOP GAIN vs TEMPERATURE

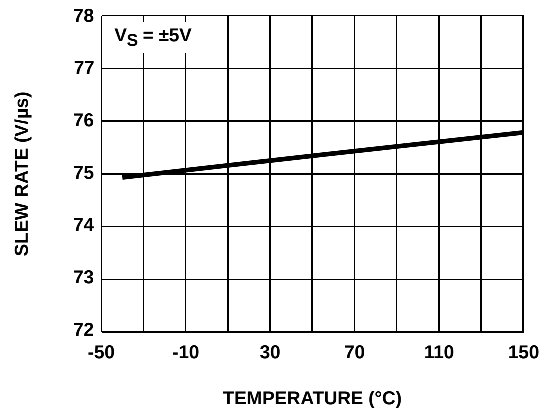


FIGURE 8. SLEW RATE vs TEMPERATURE

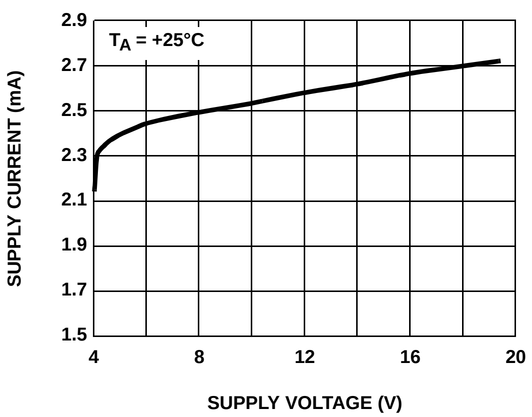


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

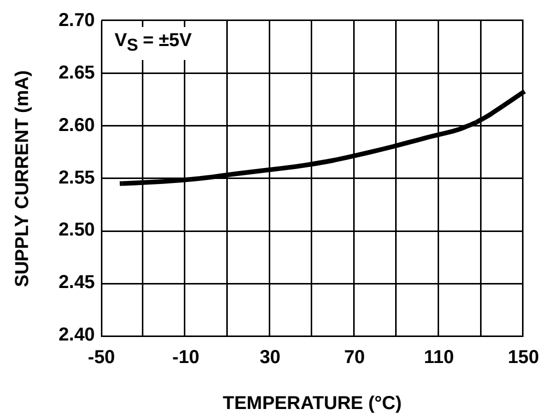


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

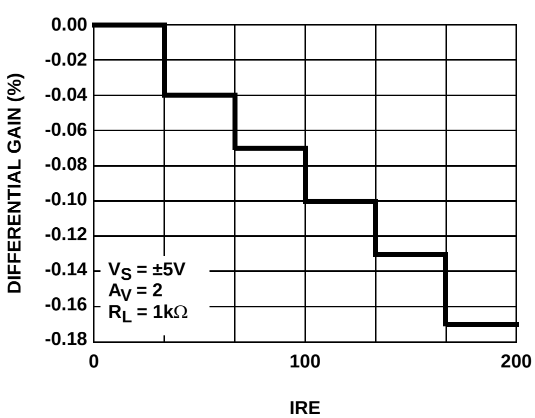


FIGURE 11. DIFFERENTIAL GAIN

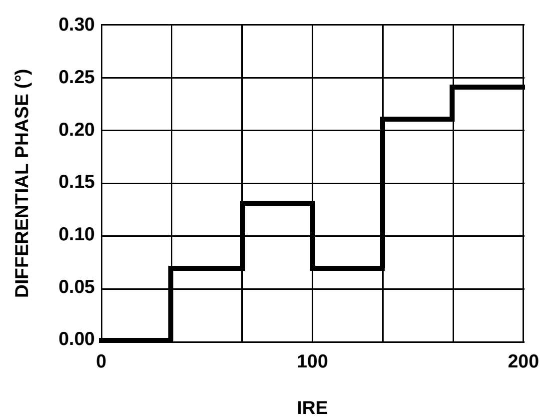


FIGURE 12. DIFFERENTIAL PHASE

Typical Performance Curves (Continued)

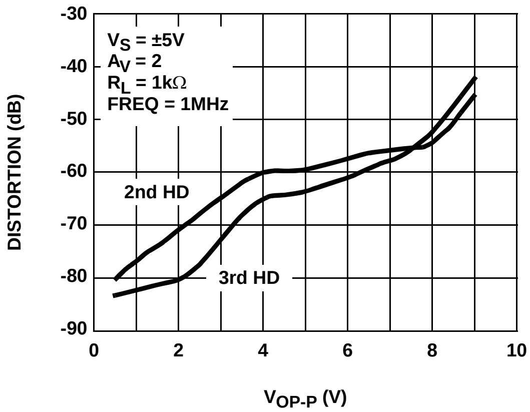


FIGURE 13. HARMONIC DISTORTION vs V_{OP-P}

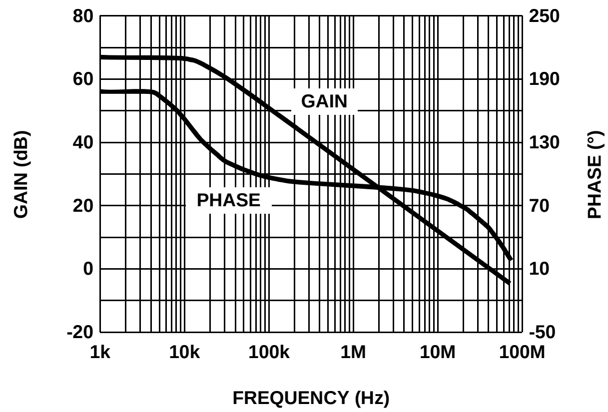


FIGURE 14. OPEN LOOP GAIN AND PHASE

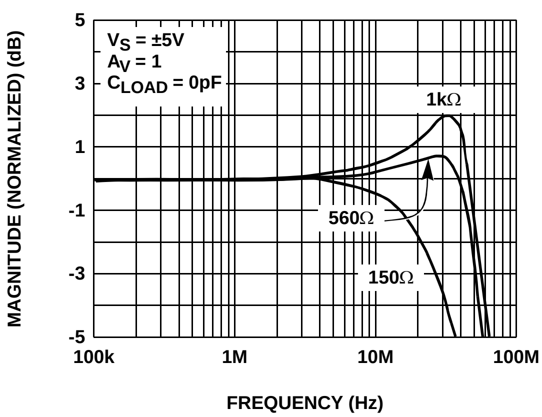


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS R_L

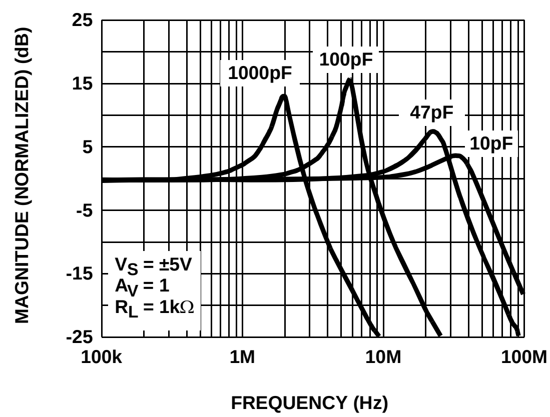


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS C_L

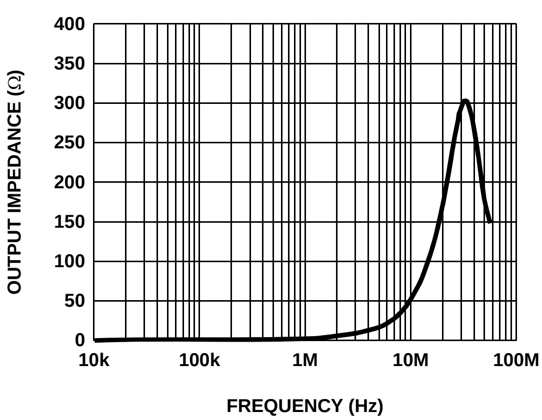


FIGURE 17. CLOSED LOOP OUTPUT IMPEDANCE

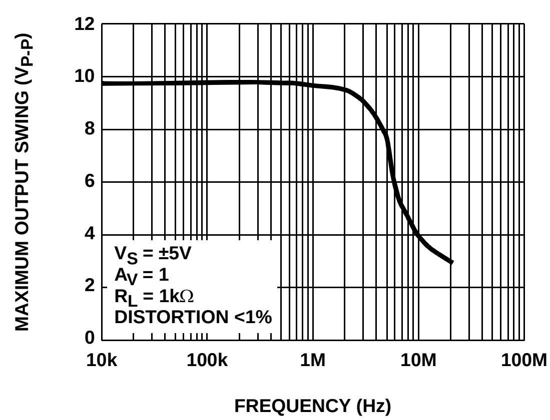


FIGURE 18. MAXIMUM OUTPUT SWING vs FREQUENCY

Typical Performance Curves (Continued)

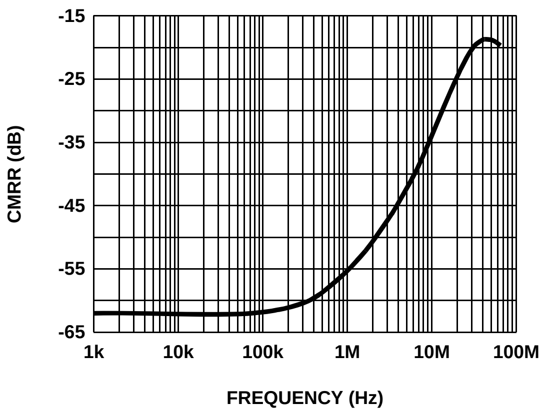


FIGURE 19. CMRR

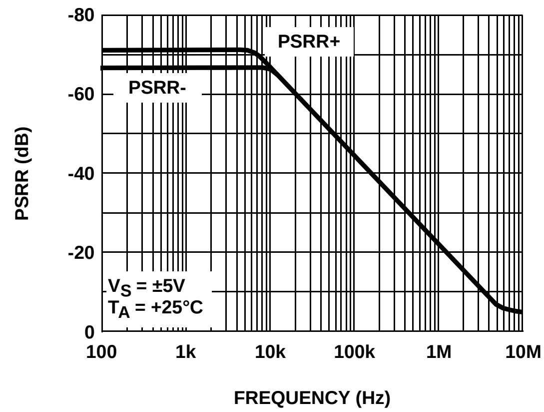


FIGURE 20. PSRR

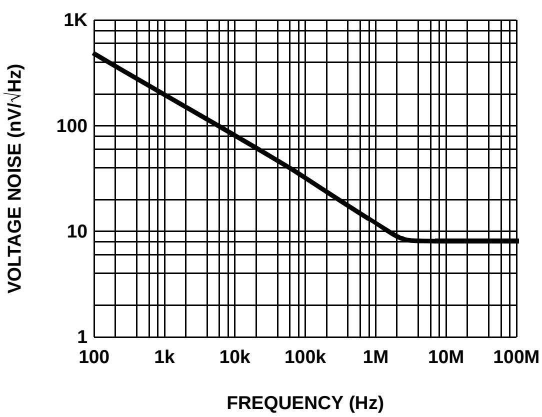


FIGURE 21. INPUT VOLTAGE NOISE SPECTRAL DENSITY

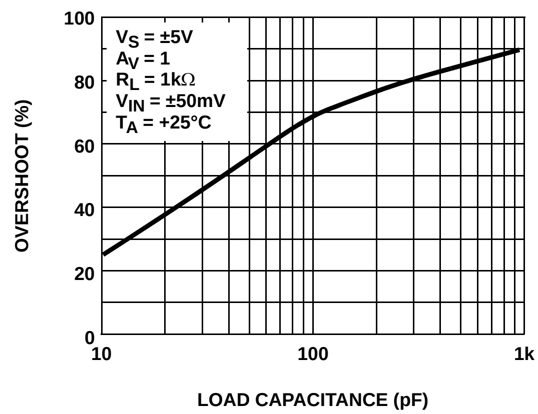


FIGURE 22. SEPARATIONSMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

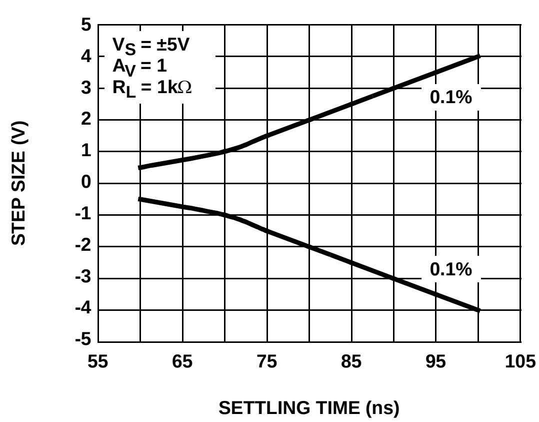
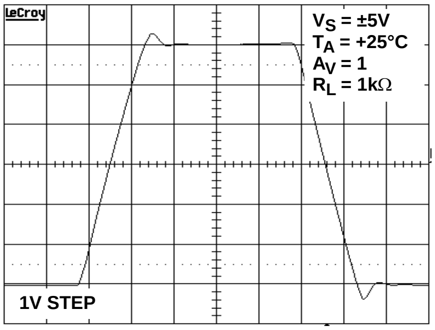


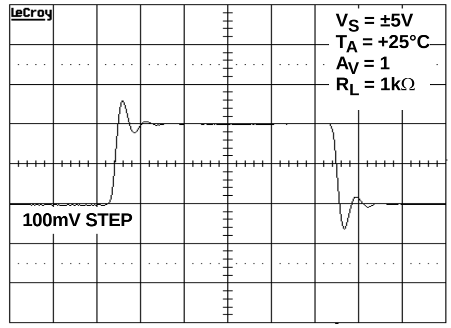
FIGURE 23. SETTLING TIME vs STEP SIZE

Typical Performance Curves (Continued)



50ns/DIV

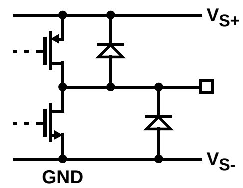
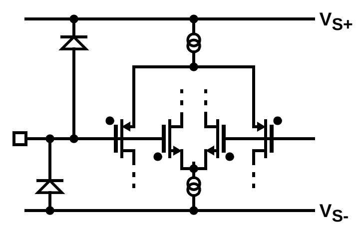
FIGURE 24. LARGE SIGNAL TRANSIENT RESPONSE



50ns/DIV

FIGURE 25. SMALL SIGNAL TRANSIENT RESPONSE

Pin Descriptions

ISL24020 (TSOT-5)	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUT	Amplifier A output	 CIRCUIT 1
2	VS-	Negative power supply	
3	VIN+	Amplifier A non-inverting input	(Reference Circuit 2)
4	VIN-	Amplifier A inverting input	 CIRCUIT 2
5	VS+	Positive power supply	

Applications Information

Product Description

The ISL24020 voltage feedback amplifier is fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability, is unity gain stable and has low power consumption (2.5mA). These features make the ISL24020 ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 1kΩ, the ISL24020 has a -3dB bandwidth of 60MHz while maintaining a 75V/µs slew rate.

Operating Voltage, Input, and Output

The ISL24020 is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most ISL24020 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the "Typical Performance Curves" on page 3.

The input common-mode voltage range of the ISL24020 extends 500mV beyond the supply rails. The output swings of the ISL24020 typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 26 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ±5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.8V_{P-P}$.

V_S = ±5V, T_A = +25°C, A_V = 1, V_{IN} = $10V_{P-P}$

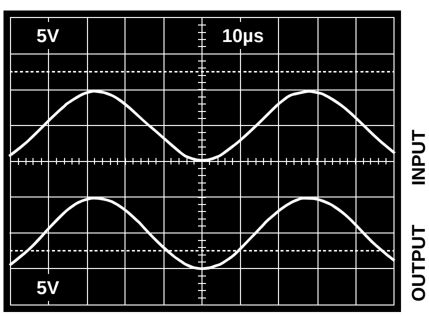


FIGURE 26. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The ISL24020 will limit the short circuit current to ±180mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±65mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The ISL24020 is immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 27 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

V_S = ±2.5V, T_A = +25°C, A_V = 1, V_{IN} = $6V_{P-P}$

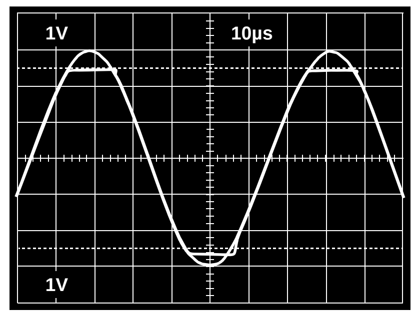


FIGURE 27. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the ISL24020 amplifier, it is possible to exceed the +125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT} i) \times I_{LOAD} i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT} i - V_S -) \times I_{LOAD} i] \quad \text{(EQ. 3)}$$

when sinking.

Where:

- i = 1 to 2 for dual and 1 to 4 for quad
- V_S = Total supply voltage
- I_{SMAX} = Maximum supply current per amplifier
- $V_{OUT}i$ = Maximum output voltage of the application
- $I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat.

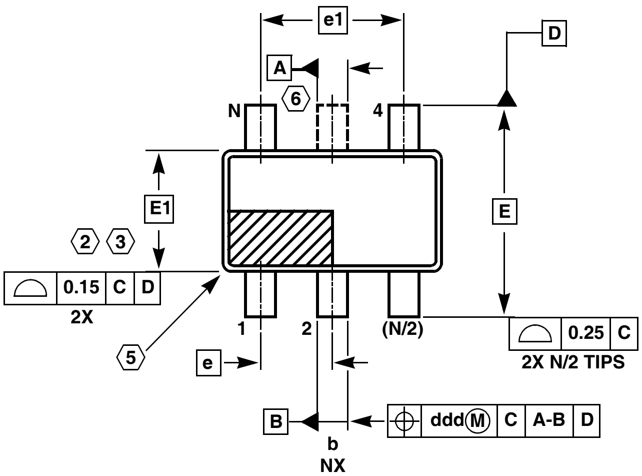
Unused Amplifiers

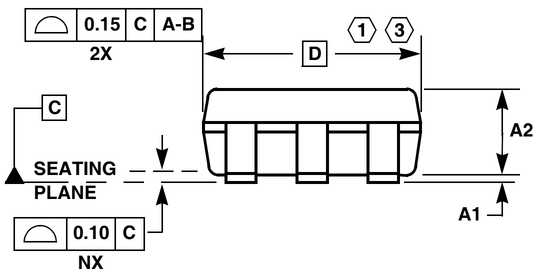
It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

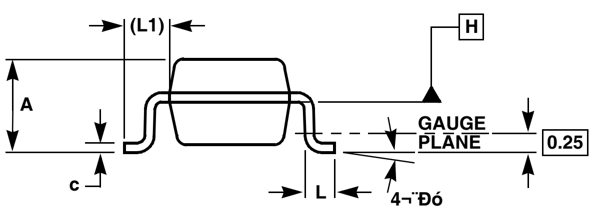
Power Supply Bypassing and Printed Circuit Board Layout

The ISL24020 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ to pin to V_S- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

TSOT Package Family







MDP0049

TSOT PACKAGE FAMILY

SYMBOL	MILLIMETERS			TOLERANCE
	TSOT5	TSOT6	TSOT8	
A	1.00	1.00	1.00	Max
A1	0.05	0.05	0.05	±0.05
A2	0.87	0.87	0.87	±0.03
b	0.38	0.38	0.29	±0.07
c	0.127	0.127	0.127	+0.07/-0.007
D	2.90	2.90	2.90	Basic
E	2.80	2.80	2.80	Basic
E1	1.60	1.60	1.60	Basic
e	0.95	0.95	0.65	Basic
e1	1.90	1.90	1.95	Basic
L	0.40	0.40	0.40	±0.10
L1	0.60	0.60	0.60	Reference
ddd	0.20	0.20	0.13	-
N	5	6	8	Reference

Rev. B 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.15mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (TSOT6 AND TSOT8 only).
6. TSOT5 version has no center lead (shown as a dashed line).