

RoHS Compliant Product  
A suffix of "-C" specifies halogen and lead-free

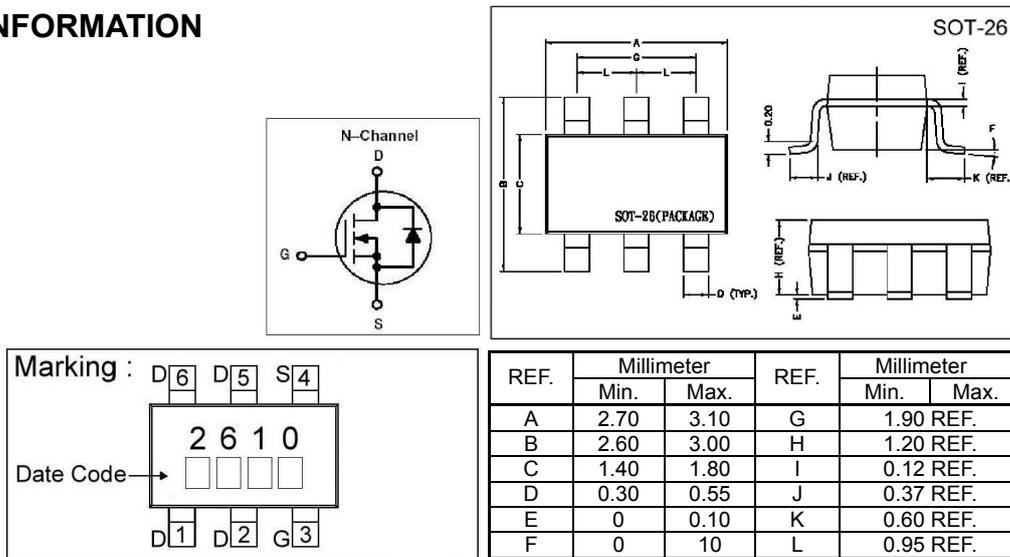
## DESCRIPTION

- The SST2610 uses advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device.
- It is universally used for all commercial-industrial applications.

## APPLICATIONS

- Low on-resistance
- Capable of 2.5V gate drive

## PACKAGE INFORMATION



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	±20	V
Continuous Drain Current <sup>3</sup>	$I_D$	3.0	A
Continuous Drain Current <sup>3</sup>	$I_D$	2.3	A
Pulsed Drain Current <sup>1,2</sup>	$I_D$	10	A
Power Dissipation	$P_D$	2	W
Linear Derating Factor		0.016	W / °C
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	-55 ~ +150	°C

## THERMAL DATA

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient <sup>3</sup>	$R_{\theta JA}$	62.5	°C / W

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified)**

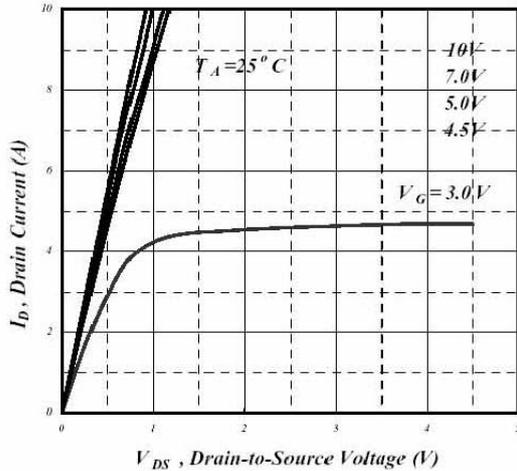
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	-	-	V	V <sub>GS</sub> = 0, I <sub>D</sub> = 250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	-	0.05	-	V / °C	Reference to 25°C, I <sub>D</sub> =1mA
Forward Transconductance	V <sub>GS(th)</sub>	1.0	-	3.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA
Gate Leakage Current	g <sub>fs</sub>	-	5.0	-	S	V <sub>DS</sub> = 5V, I <sub>D</sub> =3A
Zero Gate Voltage Drain Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V
Zero Gate Voltage Drain Current (T <sub>J</sub> =25°C)	I <sub>DSS</sub>	-	-	10		V <sub>DS</sub> =60V, V <sub>GS</sub> =0
Drain-Source Leakage Current (T <sub>J</sub> =70°C)		-	-	25		V <sub>DS</sub> =48V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	-	90	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =3A
		-	-	120		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	6	10	ns	I <sub>D</sub> =3A V <sub>DS</sub> =48V V <sub>GS</sub> =4.5V
Gate-Source Charge	Q <sub>gs</sub>	-	1.6	-		
Gate-Drain ("Miller") Change	Q <sub>gd</sub>	-	3	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(on)</sub>	-	6	-	ns	V <sub>DS</sub> =30V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω R <sub>D</sub> =30Ω
Rise Time	T <sub>r</sub>	-	5	-		
Turn-off Delay Time	T <sub>d(off)</sub>	-	16	-		
Fall Time	T <sub>f</sub>	-	3	-		
Input Capacitance	C <sub>iss</sub>	-	490	780	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	55	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	40	-		

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified)**

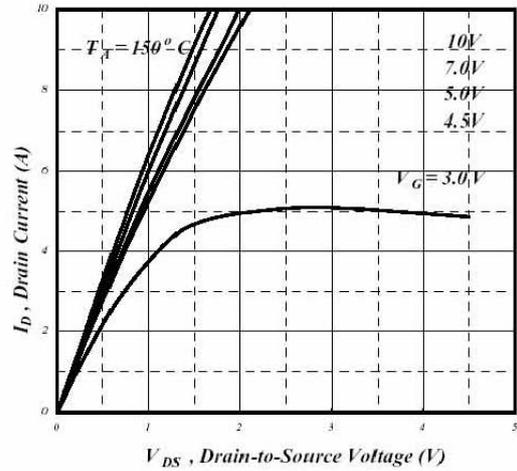
Parameter	Symbo	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	1.2	V	I <sub>S</sub> = 1.2 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	T <sub>rr</sub>	-	25	-	ns	I <sub>S</sub> =3A, V <sub>GS</sub> =0V
Reverse Recovery Charge	Q <sub>rr</sub>	-	26	-	nC	di/dt=100A/μs

- Notes:
1. Pulse width limited by Max. junction temperature.
  2. Pulse width 300us, duty cycle ≤ 2%.
  3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, 156°C/W when mounted on min. copper pad.

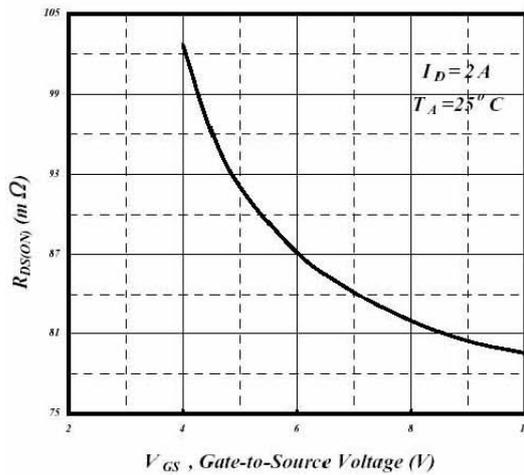
**CHARACTERISTIC CURVES**



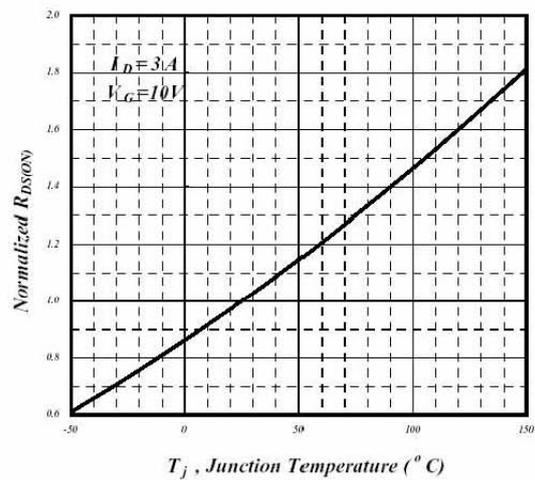
**Fig 1. Typical Output Characteristics**



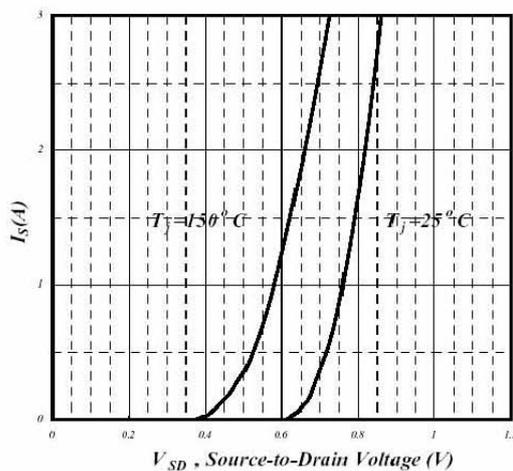
**Fig 2. Typical Output Characteristics**



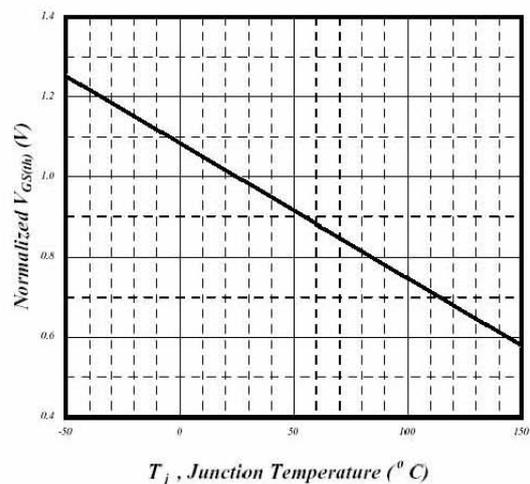
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

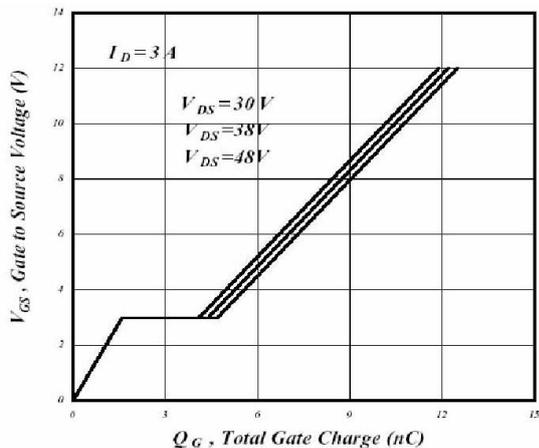


**Fig 5. Forward Characteristics of Reverse Diode**

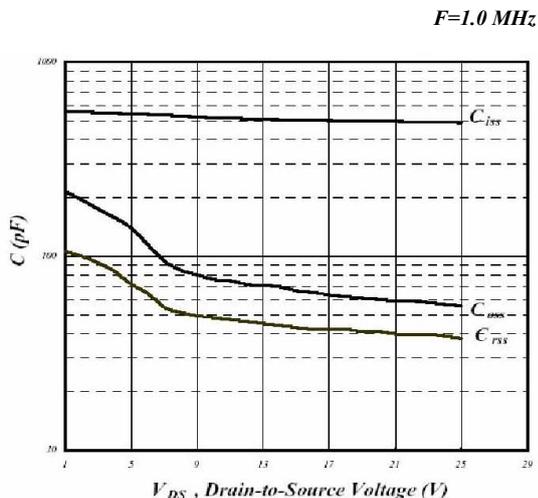


**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

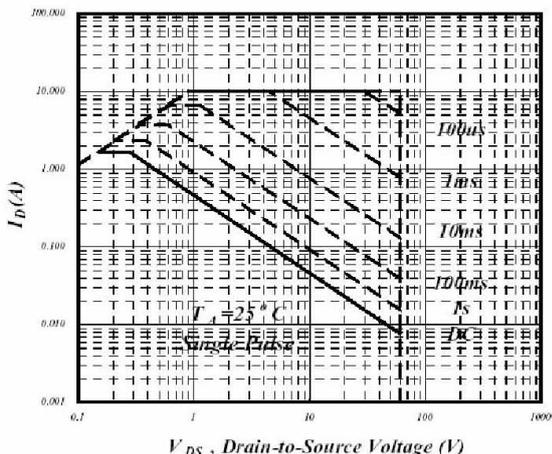
**CHARACTERISTIC CURVES (cont'd)**



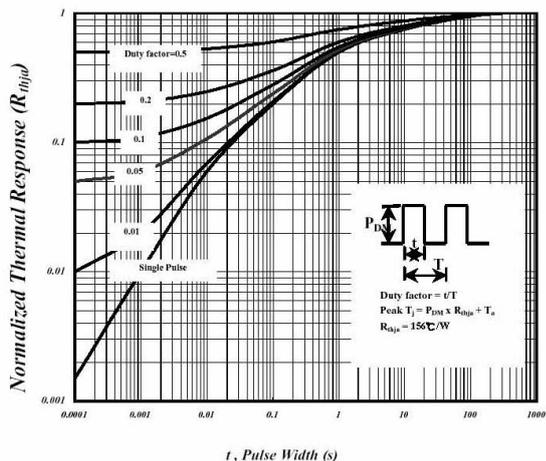
**Fig 7. Gate Charge Characteristics**



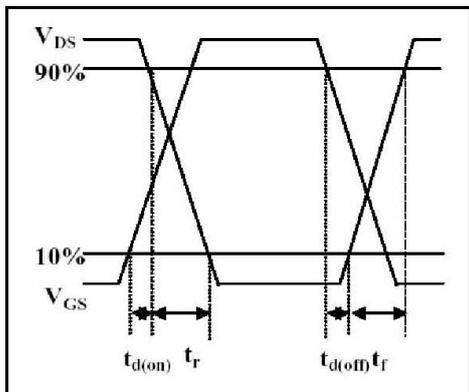
**Fig 8. Typical Capacitance Characteristics**



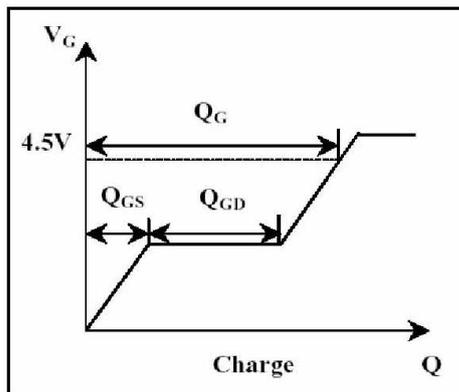
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Switching Time Waveform**



**Fig 12. Gate Charge Waveform**