PO74HSTL314A

3.3V 2:4 Differential Clock/Data Fanout Buffer

07/28/06

500MHz HSTL Potato Chip

FEATURES:

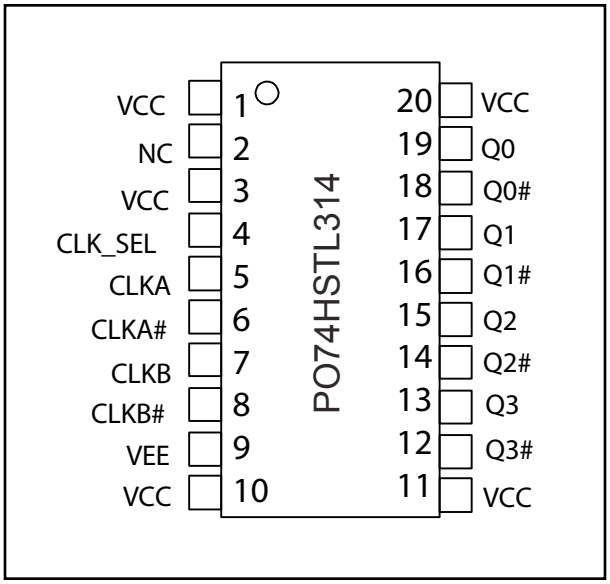
. Patented Technology
. Four HSTL differential outputs
. The two pair of LVDS/LVPECL/HSTL/ differential or single-ended inputs
. Hot-swappable/-insertable
. Operating frequency up to 500MHz with 2pf load
. Operating frequency up to 480MHz with 5pf load
. Operating frequency up to 400MHz with 15pf load
. Very low output pin to pin skew < 80ps
. Very low pulse skew < 80ps
. 2.8-ns propagation delay (typical)
. 2.4V to 3.6V power supply
. Industrial temperature range: –40°C to 85°C
. 20-pin 209 mil SSOP package

DESCRIPTION:

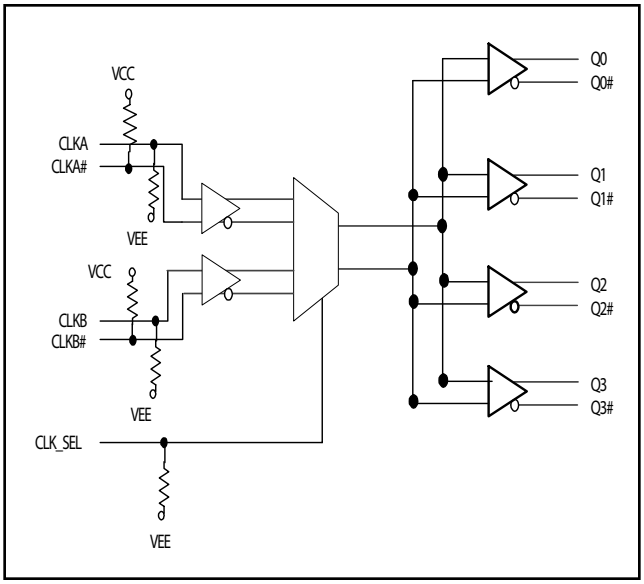
The PO74HSTL314 is a low-skew, 2-to-4 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on 0.35um CMOS technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 500MHz .

The device features two differential input paths that are multiplexed plexed internally. This mux is controlled by the CLK_SEL pin. The PO74HSTL314 may function not only as a differential clock buffer but also as a signal-level translator and fanout on HSTL or LVCMOS / LVTTL single-ended signal to four HSTL differential loads. Since the PO74HSTL314 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems.

Pin Configuration



Logic Block Diagram



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Pin Definitions

Pin	Name	I/O	Type	Description
1, 10,11,20,3	VCC	VCC	Power	Power supply, positive connection
2	NC			No connect
4	CLK_SEL	I,PD	LVCMOS	Input clock select with pull down resistor
5	CLKA	I,PD	LVDS, PECL, HSTL	Default differential clock input
6	CLKA#	I,PU	LVDS, PECL, HSTL	Input clock select with pull up resistor
7	CLKB	I,PD	LVDS, PECL, HSTL	Input clock select with pull down resistor
8	CLKB#	I,PU	LVDS, PECL, HSTL	Input clock select with pull up resistor
9	VEE	GND	Power	Power Ground
18, 16,14,12	Q[0:3]#	O	HSTL	Complement output
19, 17,15,13	Q[0:3]	O	HSTL	Ture output

Function Table

Control	
CLK_SEL	
0	CLKA, CLKA# input pair is active (Default condition with no connection to pin) CLKA can be driven with LVDS, ECL, PECL, HSTL or TTL compatible signals with respective power configurations
1	CLKB, CLKB# input pair is active CLKB can be driven with LVDS, ECL, PECL, HSTL or TTL compatible signals with respective power configurations

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			88		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			88		KΩ

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Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V_{IK}	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V
I_{OFF}	Power off output leakage current	Vcc = 0V. Vi or Vo = 0V to 5.5V	-	-	±5	uA

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{PD}	Propagation Delay CLKA or CLKB to Output pair	CL = 15pF	3.2	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(p)	Pulse Skew (Same Package)	CL = 15pF, 125MHz	80	ps
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	80	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	350	ps
fmax	Input Frequency	CL =15pF	400	MHz
fmax	Input Frequency	CL = 5pF	480	MHz
fmax	Input Frequency	CL = 2pF	500	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Waveforms

FIGURE 1. LVDS/ PECL/ ECL/ HSTL /DIFFERENTIAL INPUT WAVEFORM DEFINITIONS

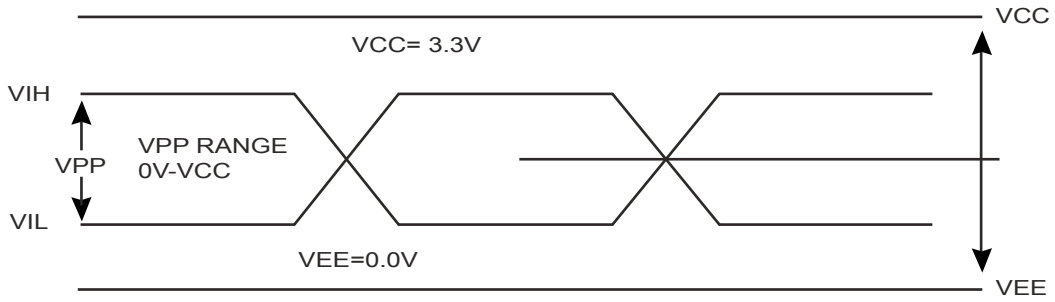


FIGURE 2. HSTL/HSTL OUTPUT

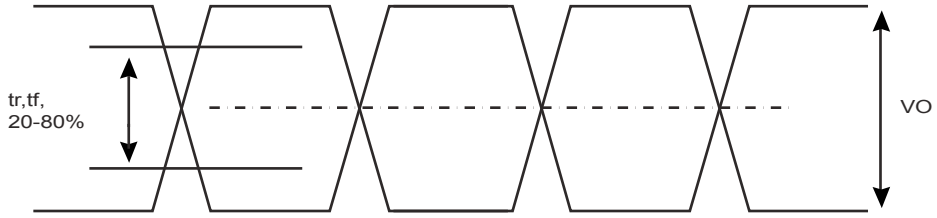
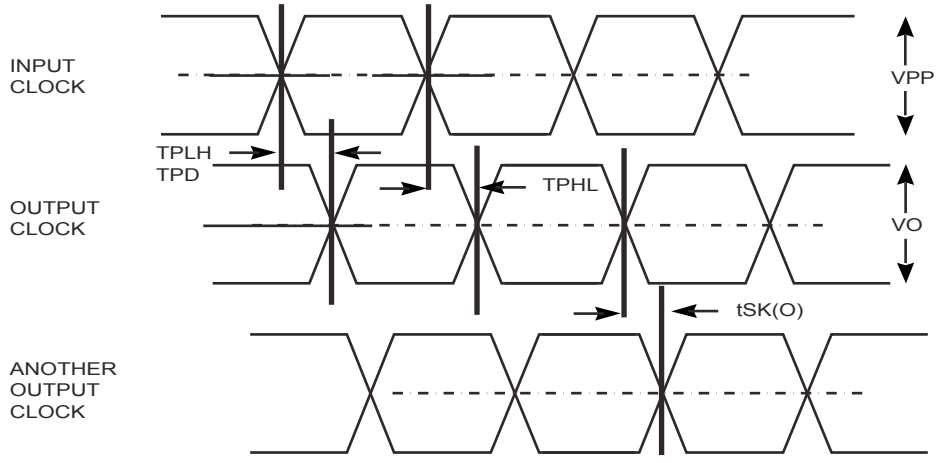
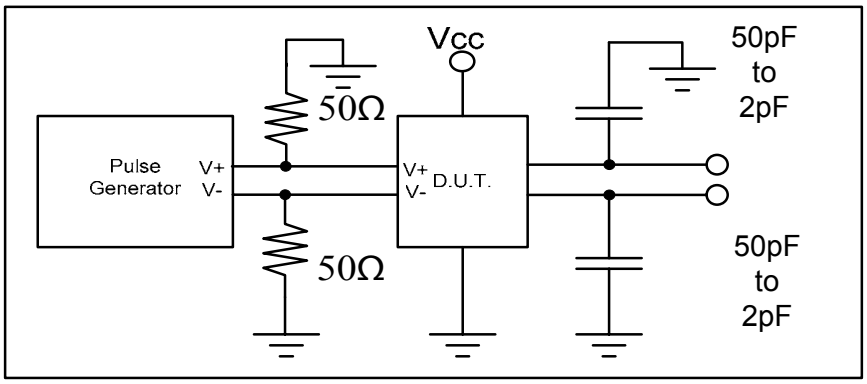


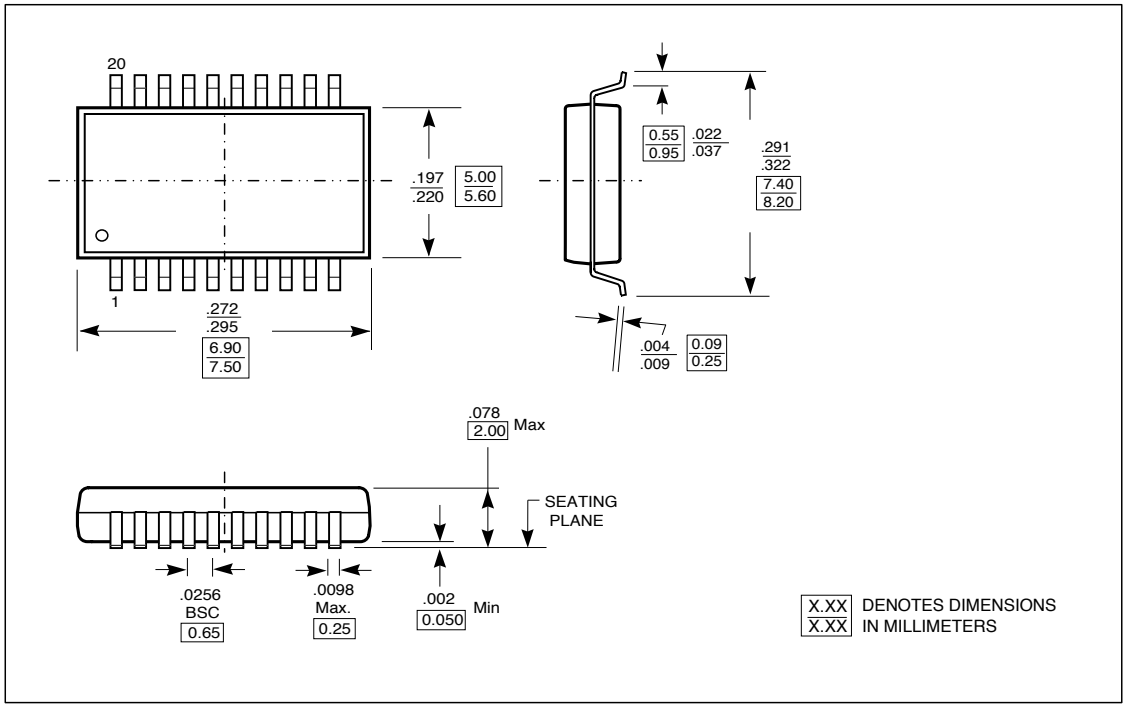
FIGURE 3. Propogation Delay, Output pulse skew, and output-to-output skew for both CLKA or CLKB to output pair



Test Circuit



Packaging Mechanical Drawing: 20 pin SSOP



Ordering Information

Ordering Code	Package			Top-Marking	T_A
PO74HSTL314ASU	20pin SSOP	Tube	Pb-free & Green	PO74HSTL314AS	-40°C to 85°C
PO74HSTL314ASR	20pin SSOP	Tape and reel	Pb-free & Green	PO74HSTL314AS	-40°C to 85°C