PECL3 Series 10K ECL Logic 3-Bit Programmable Delay Modules

Electrical Specifications at 25°C

3-Bit 10K ECL Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
			000	000	001	010	011	100	101	110	111
PECL3-0.5	0.5 ± .25	± .30	3 ± 0.5	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
PECL3-0.75	0.75 ± .3	± .50	3 ± 0.5	0.0	0.75	1.50	2.25	3.00	3.75	4.50	5.25
PECL3-1	1.0 ± .4	± .50	3 ± 0.5	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
PECL3-1.2	1.2 ± .4	± .60	3 ± 0.5	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
PECL3-1.25	1.25 ± .5	± .70	3 ± 0.5	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75
PECL3-1.3	1.3 ± .5	± .70	3 ± 0.5	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
PECL3-1.5	1.5 ± .5	± .70	3 ± 0.5	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
PECL3-1.75	1.75 ± .6	± .80	3 ± 0.5	0.0	1.75	3.50	5.25	7.00	8.75	10.50	12.25
PECL3-2	2.0 ± .7	± .80	3 ± 0.5	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
PECL3-2.5	2.5 ± .7	± .90	3 ± 0.5	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
PECL3-3	3.0 ± .7	± 1.0	3 ± 0.5	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0
PECL3-5	5.0 ± 1.0	± 1.5	3 ± 0.5	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0
PECL3-10	10.0 ± 1.5	± 3.0	3 ± 0.5	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0

3PECLH Series 10KH ECL Logic 3-Bit Programmable Delay Modules

Electrical Specifications at 25°C

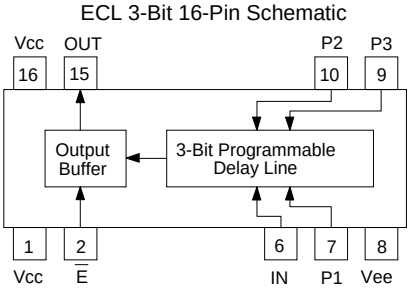
3-Bit 10KH ECL Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
			000	000	001	010	011	100	101	110	111
3PECLH-0.5	0.5 ± .25	± .30	1.5 ± 0.5	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
3PECLH0.75	0.75 ± .3	± .50	1.5 ± 0.5	0.0	0.75	1.50	2.25	3.00	3.75	4.50	5.25
3PECLH-1	1.0 ± .4	± .50	1.5 ± 0.5	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
3PECLH-1.2	1.2 ± .4	± .60	1.5 ± 0.5	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
3PECLH1.25	1.25 ± .5	± .70	1.5 ± 0.5	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75
3PECLH-1.3	1.3 ± .5	± .70	1.5 ± 0.5	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
3PECLH-1.5	1.5 ± .5	± .70	1.5 ± 0.5	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
3PECLH1.75	1.75 ± .6	± .80	1.5 ± 0.5	0.0	1.75	3.50	5.25	7.00	8.75	10.50	12.25
3PECLH-2	2.0 ± .7	± .80	1.5 ± 0.5	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
3PECLH-2.5	2.5 ± .7	± .90	1.5 ± 0.5	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
3PECLH-3	3.0 ± .7	± 1.0	1.5 ± 0.5	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0
3PECLH-5	5.0 ± 1.0	± 1.5	1.5 ± 0.5	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0
3PECLH-10	10.0 ± 1.5	± 3.0	1.5 ± 0.5	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays Referenced to Initial Delay, Setting "000." For example the setting "111" delay of PECL3-2 is 14.0 ± 0.8 ns ref. to "000," and 17.0 ± 1.3 ns referenced to the input.

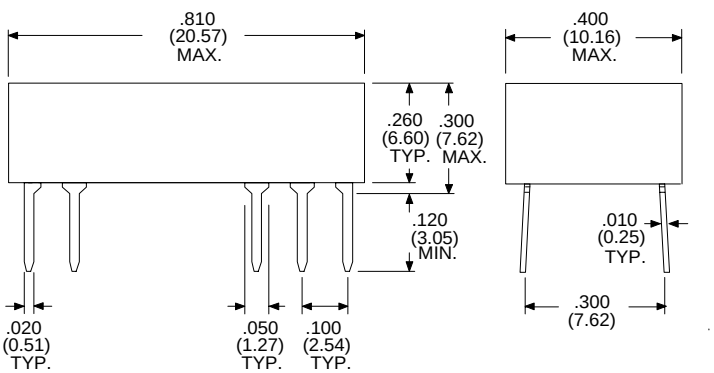
ENABLE input, Pin 2, is active low. Output will be disabled (low) when " $\overline{E}$ " is high.

INPUT LOADING: Input, Pin 6, internally connected to eight ECL gate inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

ECL 3-Bit 16-Pin Schematic



Dimensions in Inches (mm)



GENERAL: For Operating Specifications and Test Conditions, see Tables IV, V and VII on page 5 of this catalog. Delays specified for the Leading Edge.

Operating Temp. Range ..... -30°C to +85°C
Temperature Coefficient ..... ≤ 300ppm/°C typical
Minimum Input Pulse Width ..... 35% of max. Delay
Supply Current, I_{EE} ..... 75 mA typ., 85 mA max.

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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