



STS8DNH3LL

Dual n-channel 30 V - 0.018 Ω - 8 A - SO-8
low gate charge STripFET™ III Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STS8DNH3LL	30 V	< 0.022 Ω	8 A

- Optimal R_{DS(on)} x Q_g trade-off @ 4.5 V
- Conduction losses reduced
- Switching losses reduced

Application

- Switching applications

Description

This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology which is suitable for the most demanding DC-DC converter applications where high efficiency is required.

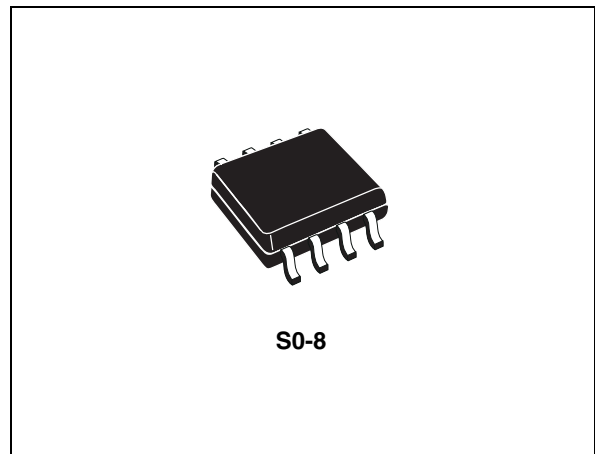


Figure 1. Internal schematic diagram

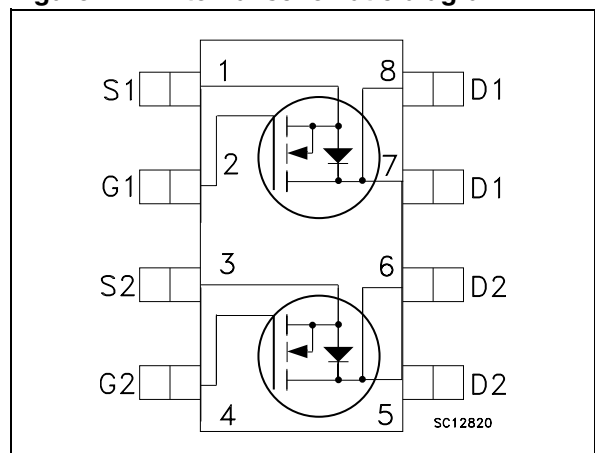


Table 1. Device summary

Order code	Marking	Package	Packaging
STS8DNH3LL	8DH3LL	SO-8	Tape & reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($v_{GS} = 0$)	30	V
V_{GS}	Gate- source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	8	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	100	mJ

1. Pulse width limited by safe operating area

2. Starting $T_J = 25^\circ\text{C}$, $I_D = 6\text{ A}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-a}^{(1)}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_J	Thermal operating junction-ambient	150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10\text{s}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$			1	μA
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating @ } 125^{\circ}C$			10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16 V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 4 A$		0.018	0.022	Ω
		$V_{GS} = 4.5 V, I_D = 4 A$		0.020	0.025	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$V_{DS} = 15 V, I_D = 4 A$		8.5		S
C_{iss}	Input capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz}, V_{GS} = 0$		857		pF
C_{oss}	Output capacitance			147		pF
C_{rss}	Reverse transfer capacitance			20		pF
Q_g	Total gate charge	$V_{DD} = 15 V, I_D = 8 A,$		7	10	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5 V$		2.5		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		2.3		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=4\text{ A}$, $R_G=4.7\ \Omega$,		12		ns
t_r	Rise time	$V_{GS}=4.5\text{ V}$ (see Figure 16)		14.5		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=15\text{ V}$, $I_D=4\text{ A}$, $R_G=4.7\ \Omega$,		23		ns
t_f	Fall time	$V_{GS}=4.5\text{ V}$ (see Figure 16)		8		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current	$V_{DD}=15\text{ V}$, $I_D=4\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$			8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	$V_{DD}=15\text{ V}$, $I_D=4\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$			32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=8\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=8\text{ A}$, $V_{DD}=15\text{ V}$		15		ns
Q_{rr}	Reverse recovery charge	$di/dt=100\text{ A}/\mu\text{s}$,		5.7		nC
I_{RRM}	Reverse recovery current	$T_j=150^\circ\text{C}$ (see Figure 15)		0.76		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

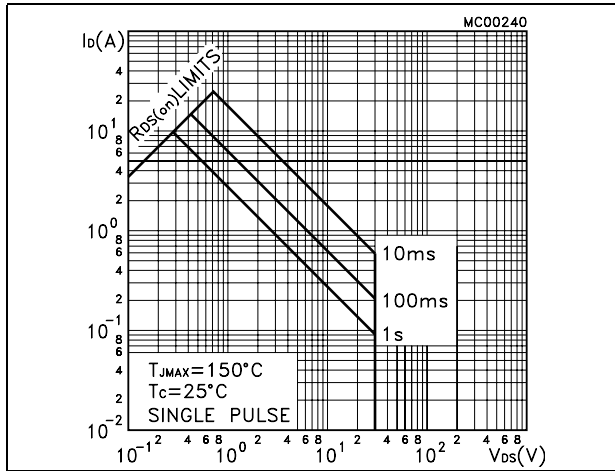


Figure 3. Thermal resistance

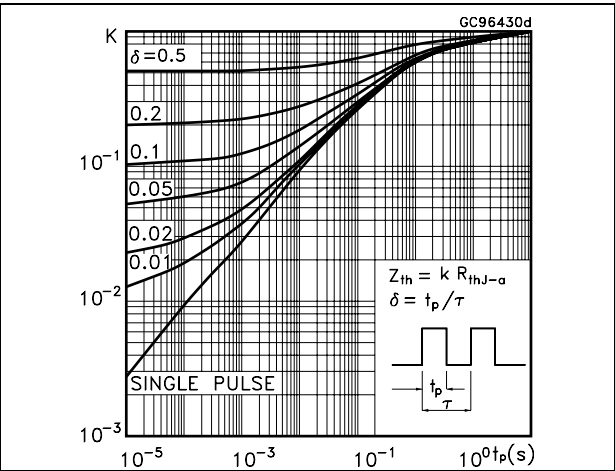


Figure 4. Output characteristics

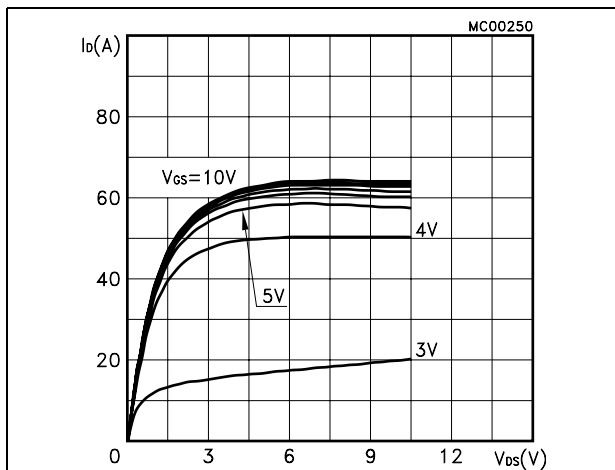


Figure 5. Transfer characteristics

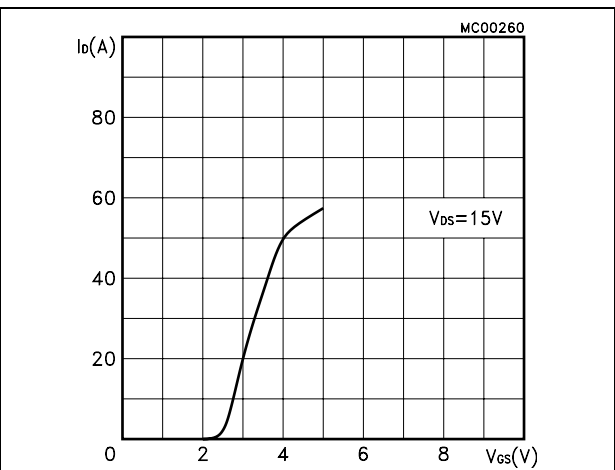


Figure 6. Static drain-source on resistance

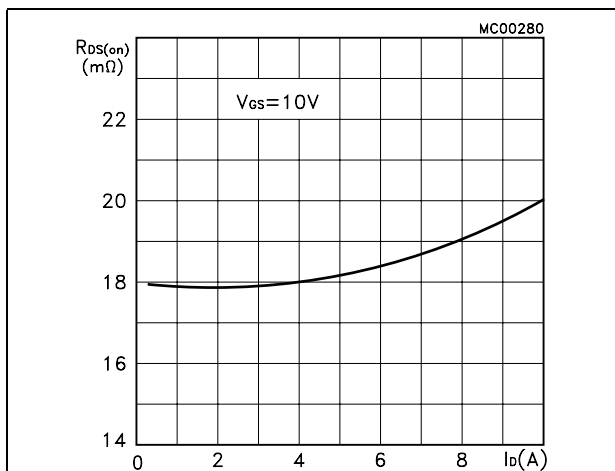


Figure 7. Normalized BV_{DSS} vs temperature

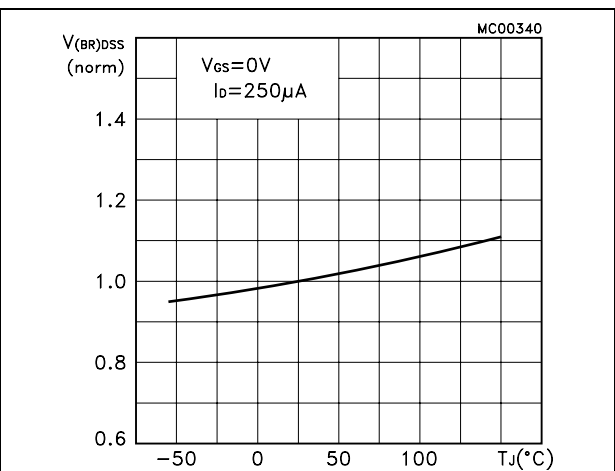


Figure 8. Gate charge vs gate-source voltage for Q1 **Figure 9. Capacitance variations**

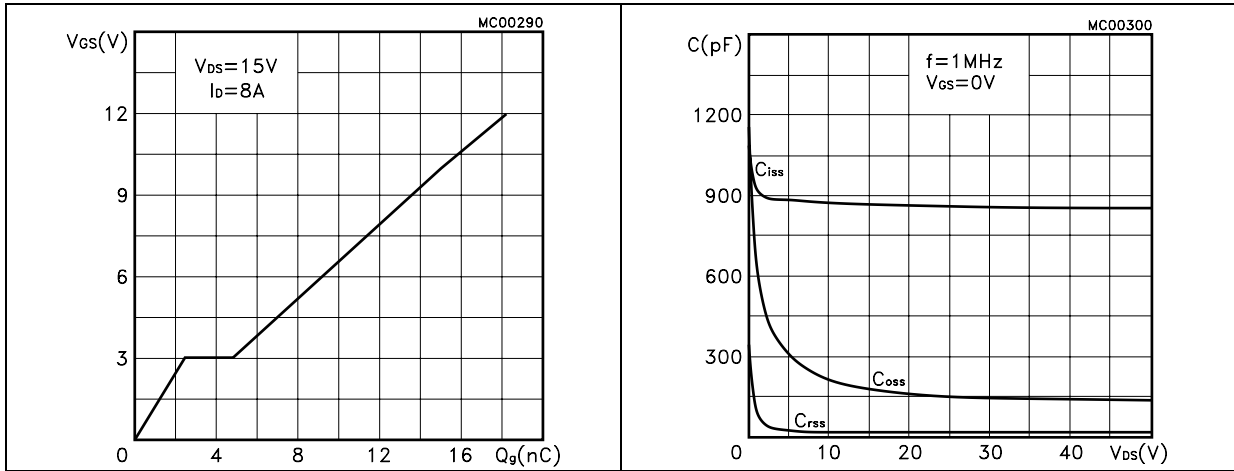


Figure 10. Normalized gate threshold voltage vs temperature for Q1 **Figure 11. Normalized on resistance vs temperature**

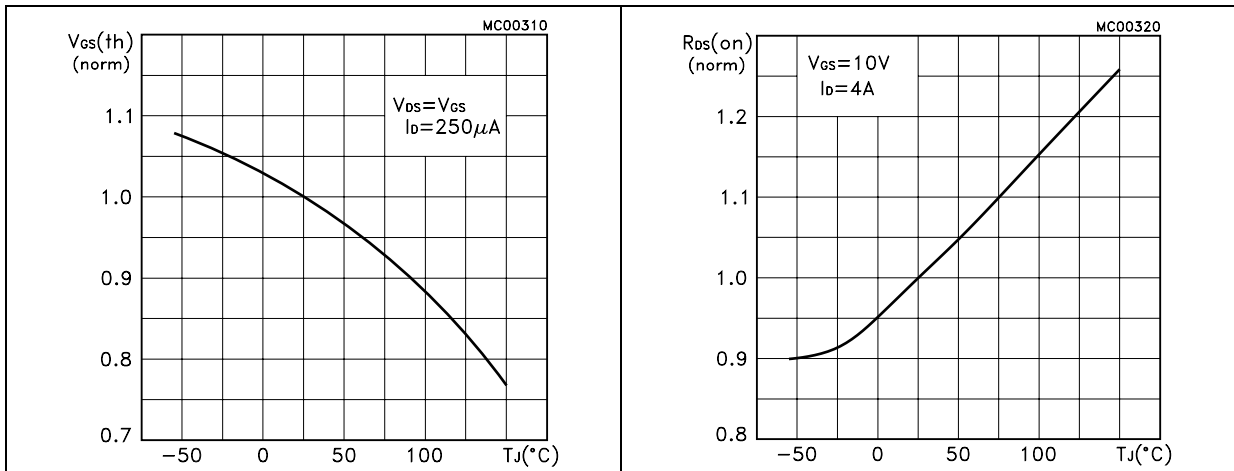
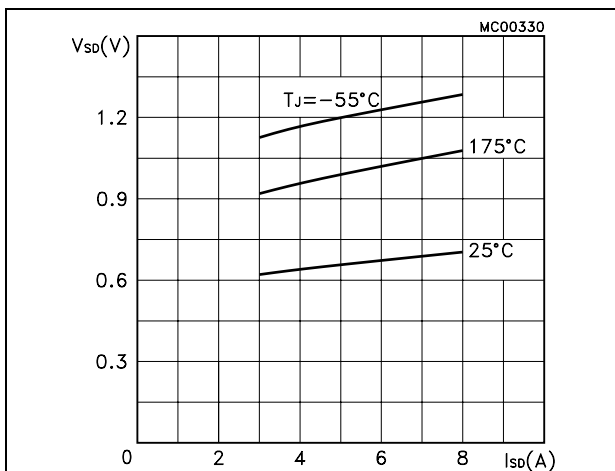


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

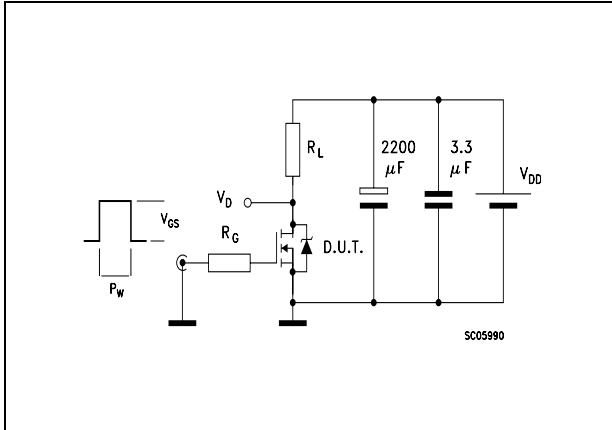


Figure 14. Gate charge test circuit



Figure 15. Test circuit for inductive load switching and diode recovery times

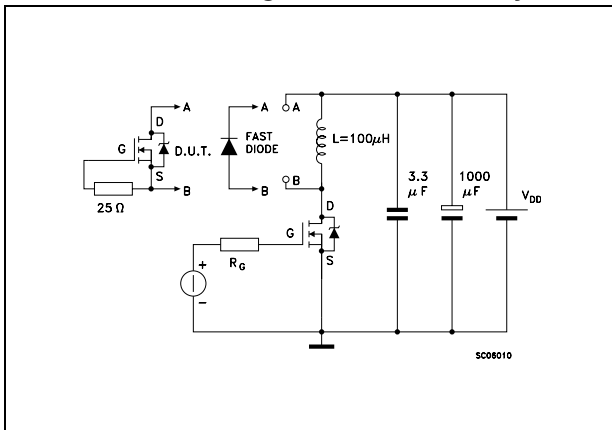


Figure 16. Unclamped Inductive load test circuit

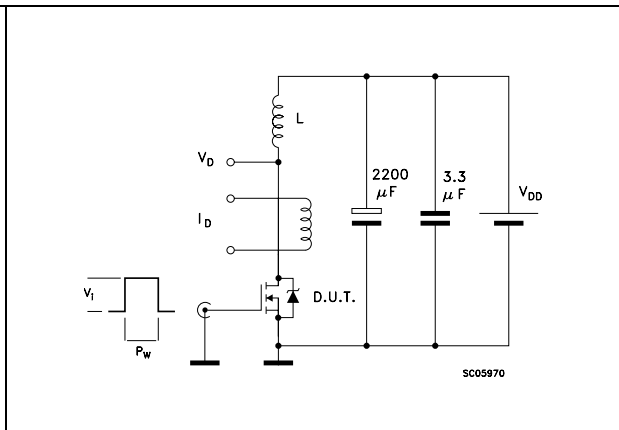


Figure 17. Unclamped inductive waveform

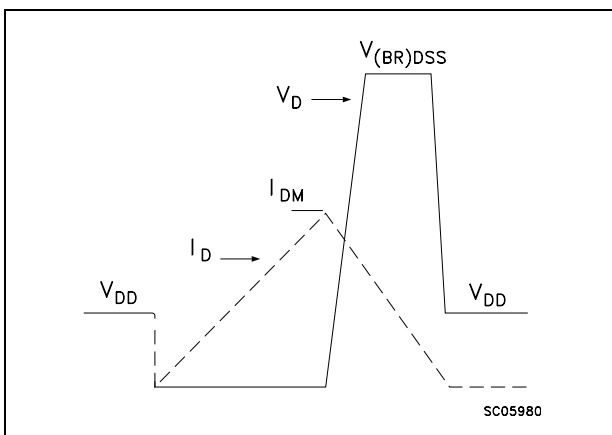
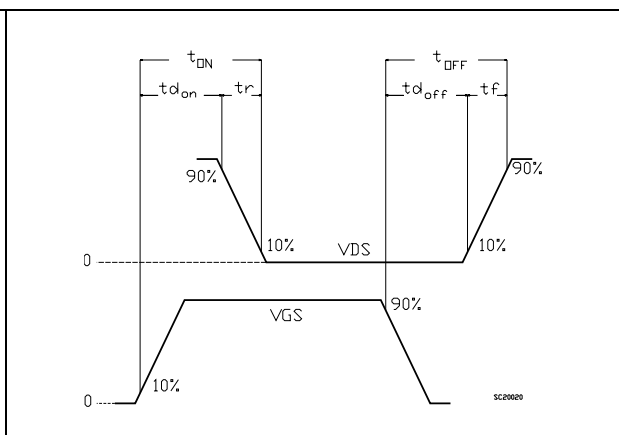


Figure 18. Switching time waveform

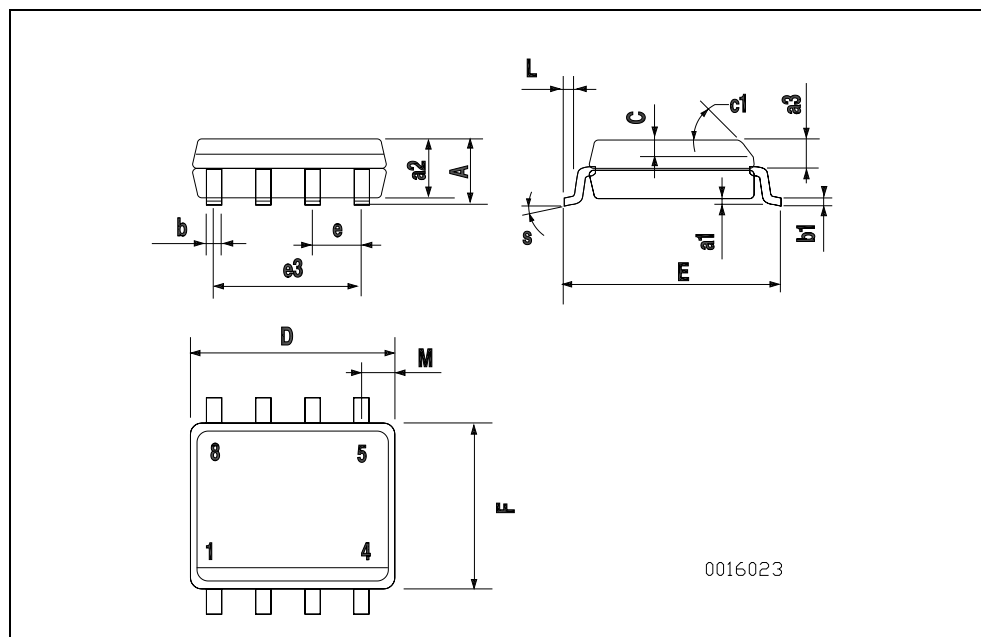


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-Jun-2004	1	First release
16-Jun-2008	2	Modified marking

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