FAIRCHILD SEMICONDUCTOR®

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FMS6143
Low-Cost Three-Channel 4th-Order Standard Definition Video Filter Driver

Features

- Three 4th-order 8MHz (SD) filters
- Drives single, AC- or DC-coupled, video loads ($2V_{pp}$, 150Ω)
- Drives dual, AC- or DC-coupled, video loads ($2V_{pp}$, 75Ω)
- Transparent input clamping
- AC- or DC-coupled inputs
- AC- or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Robust 8kV ESD protection
- Lead-free SOIC-8 package

Applications

- Cable set-top boxes
- Satellite set-top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6143 Low-Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Three 4th-order filters provide improved image quality compared to typical 2nd or 3rd-order passive solutions.

The FMS6143 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (see *Applications* section for details).

The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC-levels are offset approximately +280mV at the output (see the *Applications* section for details).

Related Application Notes

AN-8002 — FMS6418B 4:2:2 Application Note

AN-6024 — FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC-Restore, and AC or DC Coupling Methods

AN-6041 — PCB Layout Considerations for Video Filter / Drivers

Functional Block Diagram

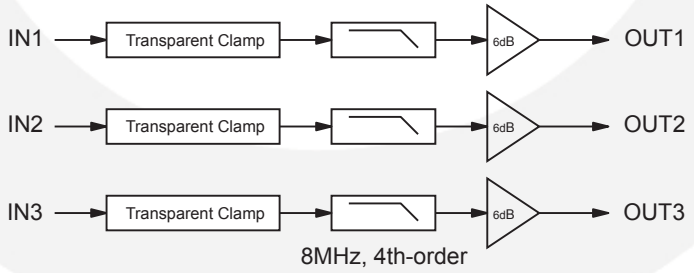


Figure 1. AC-Coupled Inputs and Outputs

Ordering Information

Part Number	Package	Pb-Free	Operating Temperture Range	Packaging Method
FMS6143CS	SOIC-8	Yes	-40 to +85°C	Tube
FMS6143CSX	SOIC-8	Yes	-40 to +85°C	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Pin Configuration

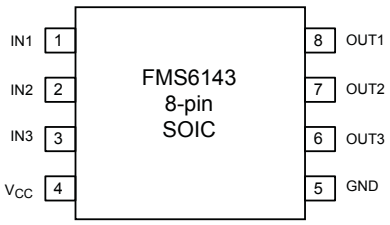


Figure 2. AC-Coupled Inputs and Outputs

Pin Assignments

Pin #	Name	Type	Description
1	IN1	Input	Video input, Channel 1
2	IN2	Input	Video input, Channel 2
3	IN3	Input	Video input, Channel 3
4	V_{CC}	Input	+5V supply, do not float
5	GND	Output	Must be tied to ground, do not float
6	OUT3	Output	Filtered output, Channel 3
7	OUT2	Output	Filtered output, Channel 2
8	OUT1	Output	Filtered output, Channel 1

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
	Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
	Output Channel - Any One Channel (Do Not Exceed)		50	mA

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.

Reliability Information

Symbols	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature (Soldering, 10s)			+300	°C
θ_{JA}	Thermal Resistance, JEDEC Standard Multi-layer Test Boards, Still Air		115		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbols	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	V_{CC} Range	4.75	5.00	5.25	V

DC Electrical Characteristics

T_A = 25°C, V_{CC} = 5V, R_{SOURCE} = 37.5Ω; all inputs are AC-coupled with 0.1µF; all outputs are AC-coupled with 220µF into 150Ω loads; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(1)	FMS6143 (No Load)		19	27	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC-coupled		1.4		V_{pp}
PSRR	Power Supply Rejection	DC (All Channels)		-50		dB

AC Electrical Characteristics

T_A = 25°C, V_{IN} = 1V_{pp}, V_{CC} = 5V, R_{SOURCE} = 37.5Ω; all inputs are AC-coupled with 0.1µF; all outputs are AC-coupled with 220µF into 150Ω loads; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV	Channel Gain(1)	All Channels	6.0	6.2	6.4	dB
f_{1dB}	-1dB Bandwidth(1)	All Channels	5.6	6.5		MHz
f_C	-3dB Bandwidth	All Channels		7.7		MHz
f_{SB}	Attenuation (Stopband Reject)	All Channels at f = 27MHz		48		dB
DG	Differential Gain	All Channels		0.3		%
DP	Differential Phase	All Channels		0.6		°
THD	Output Distortion (All Channels)	V_{OUT} = 1.8V_{pp}, 1MHz		0.4		%
X_{TALK}	Crosstalk (Channel-to-Channel)	at 1MHz		-60		dB
SNR	Signal-to-Noise Ratio	All Channels, NTC-7 Weighting: 100kHz to 4.2MHz		75		dB
t_{pd}	Propagation Delay	Delay from Input-to-Output, 4.5MHz		59		ns

Note:
1. 100% tested at 25°C.

Typical Performance Characteristics

T_A = 25°C, V_{CC} = 5V, R_{SOURCE} = 37.5Ω; all inputs AC-coupled with 0.1µF; all outputs are AC-coupled with 220µF into 150Ω loads; unless otherwise noted.

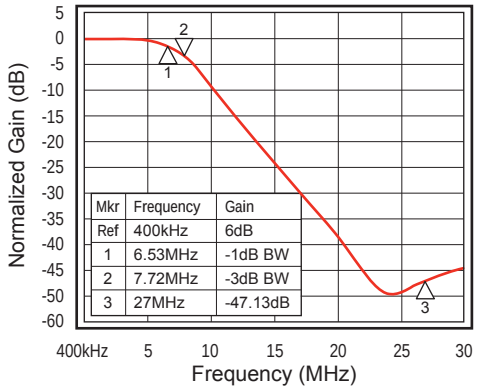


Figure 3. Frequency Response

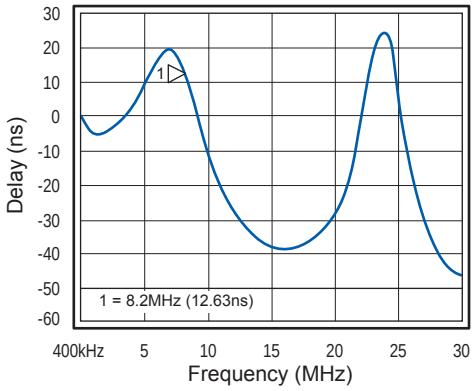


Figure 4. Group Delay vs. Frequency

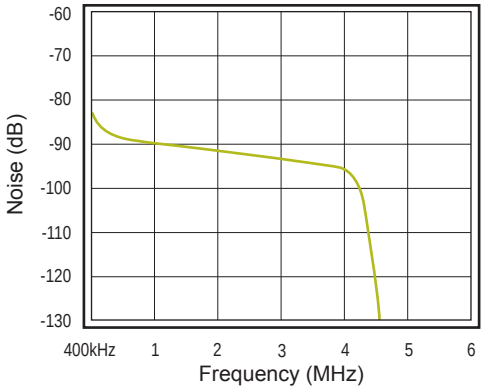


Figure 5. Noise vs. Frequency

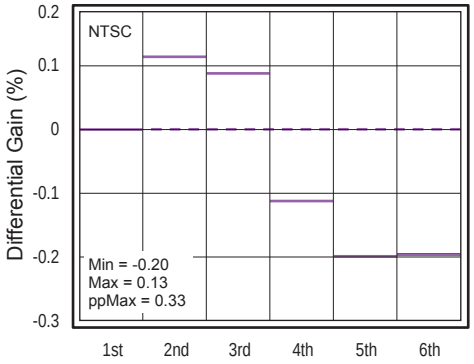


Figure 6. Differential Gain

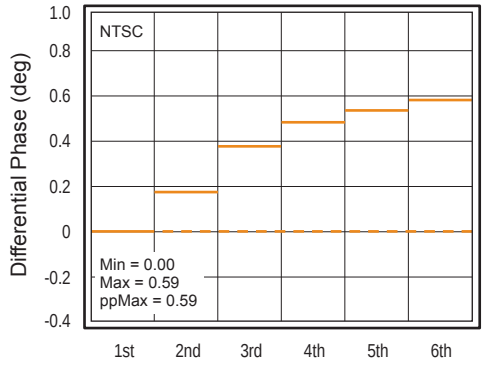


Figure 7. Differential Phase

Typical Application Diagrams

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V. AC-coupled or DC-coupled outputs may be used with AC-coupled outputs, offering slightly lower power dissipation.

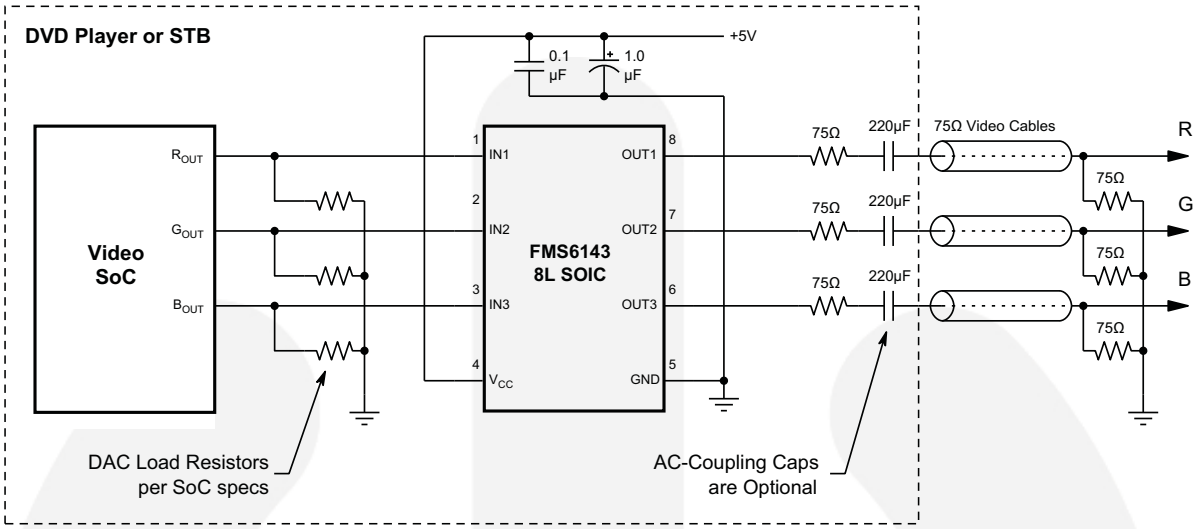
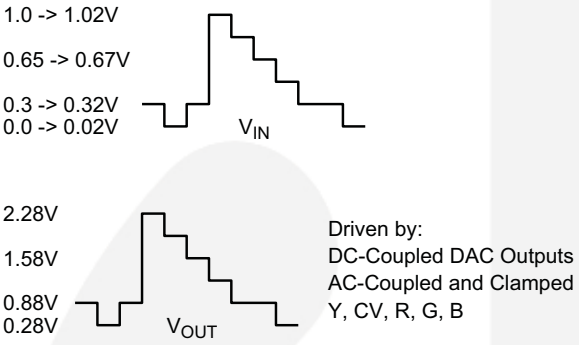


Figure 8. Typical Application Diagram

Application Information

Application Circuits

The FMS6143 Low Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in the diagram below:



There is a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$.

Figure 9. Typical Voltage Levels

The FMS6143 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6143 without an AC coupling capacitor. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp can not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr, the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 10:

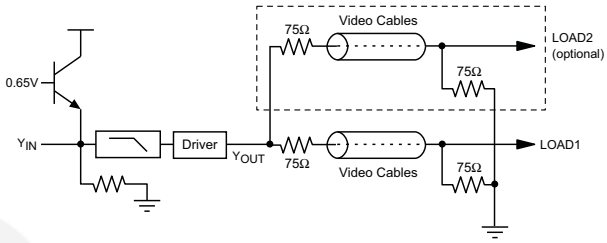


Figure 10. Input Clamp Circuit

I/O Configurations

For a DC-coupled DAC drive with DC-coupled outputs, use this configuration:

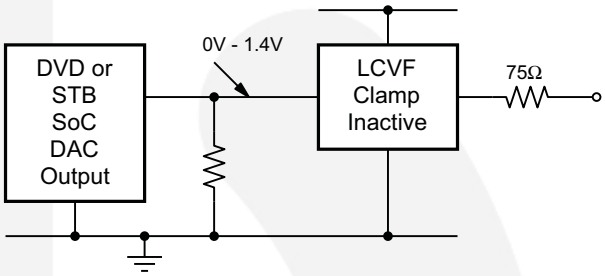


Figure 11. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC coupled as follows:

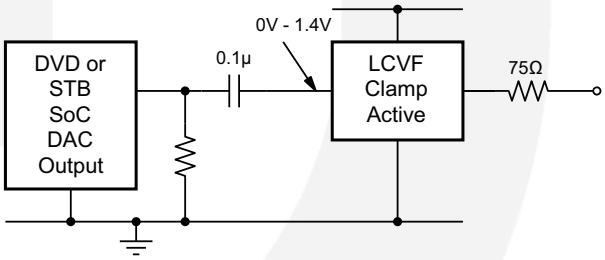


Figure 12. AC-Coupled Inputs, DC-Coupled Outputs

When the FMS6143 is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled like this:

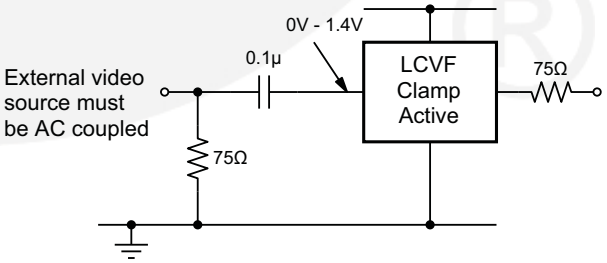


Figure 13. SCART with DC-Coupled Outputs

The same method can be used for biased signals, with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV:

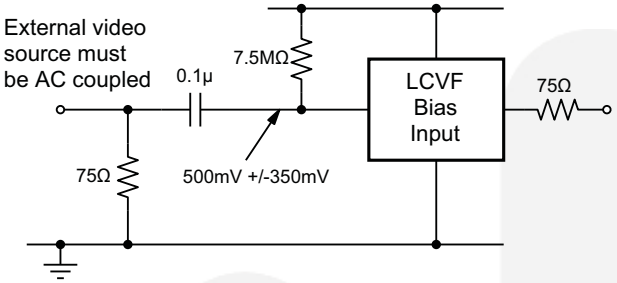


Figure 14. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

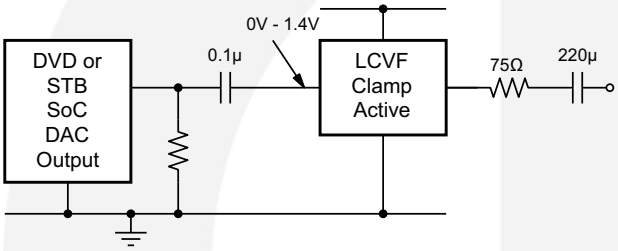


Figure 15. DC-Coupled Inputs, AC-Coupled Outputs

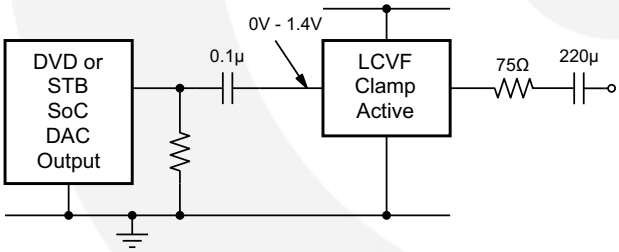


Figure 16. AC-Coupled Inputs and Outputs

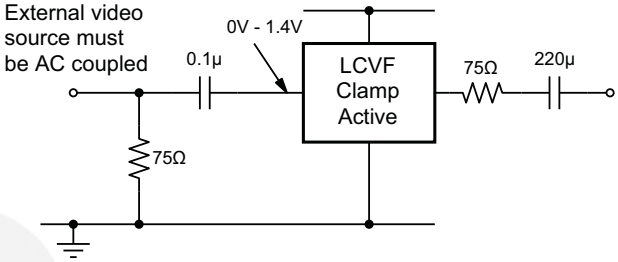


Figure 17. Biased SCART with AC-Coupled Outputs

NOTE: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6143 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the power dissipation and internal temperature rise.

$$T_J = T_A + P_d \bullet \theta_{JA} \quad (1)$$

where: $P_d = P_{CH1} + P_{CH2} + P_{CH3}$ and (2)

$$P_{CHx} = V_{CC} \bullet I_{CH} - (V_O^2/R_L) \quad (3)$$

where: $V_O = 2V_{IN} + 0.280V$ (4)

$$I_{CH} = (I_{CC}/3) + (V_O/R_L) \quad (5)$$

V_{IN} = RMS value of input signal

I_{CC} = 19mA

V_{CC} = 5V

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* section for details.

The FMS6143 is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief-duration short-circuit conditions. This capability is not guaranteed.

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10µF and 0.1µF ceramic power supply bypass capacitors.
- Place the 0.1µF capacitor within 0.1 inches of the device power pin.
- Place the 10µF capacitor within 0.75 inches of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players, are at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane), each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70µm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques provide a first-order approximation.

Mechanical Dimensions

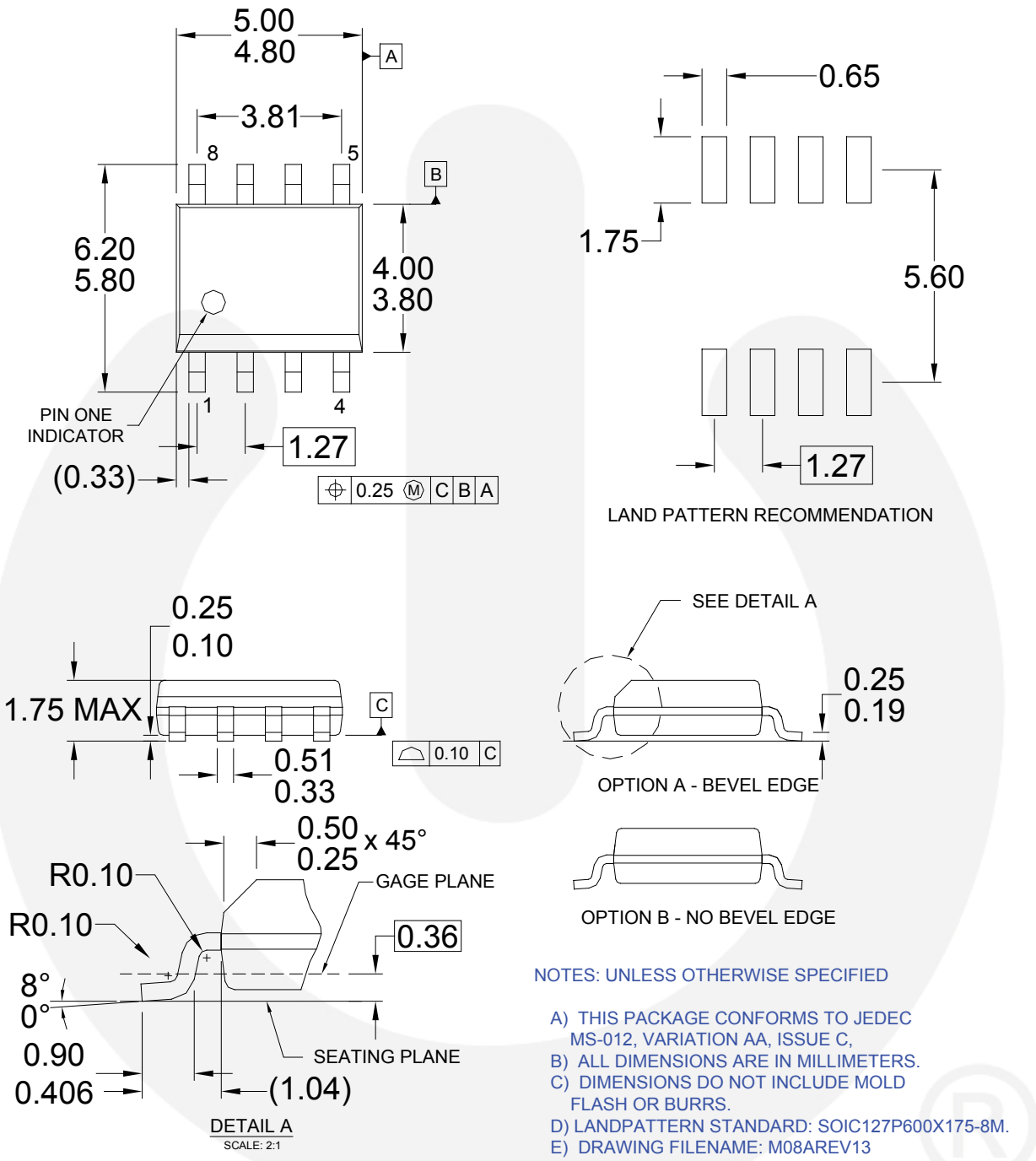


Figure 18. SOIC-8 Package

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Green FPS™
Green FPS™ e-Series™
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TinyPower™
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PRODUCT STATUS DEFINITIONS

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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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