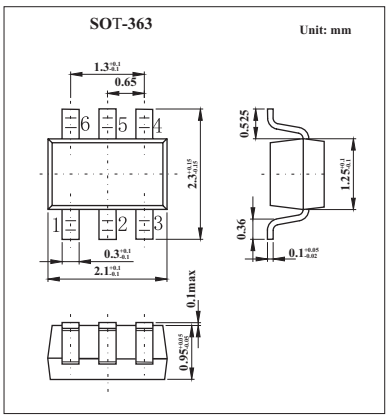
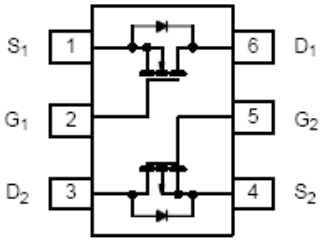
Complementary Low-Threshold MOSFET Pair

KI1555DL



■ PIN Configuration



■ Absolute Maximum Ratings T_A = 25℃

Parameter	Symbol	N-Channel		P-Channel		Unit
		5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage	V_{DS}	20		-8		V
Gate-Source Voltage	V_{GS}	±12		±8		V
Continuous Drain Current (T_J = 150℃)* T_A = 25℃	I_D	±0.70	±0.66	±0.60	±0.57	A
T_A = 85℃		±0.50	±0.48	±0.43	±0.41	A
Pulsed Drain Current	I_{DM}	±1				A
Continuous Source Current (Diode Conduction)a	I_S	0.25	0.23	-0.25	-0.23	A
Maximum Power Dissipation* T_A = 25℃	P_D	0.3	0.27	0.3	0.27	W
T_A = 85℃		0.16	0.14	0.16	0.14	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150				℃

*Surface Mounted on 1" X 1" FR4 Board.

■ Thermal Resistance Ratings T_A = 25℃

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient*	t ≤5 sec	R_{thJA}	360	415	℃/W
	Steady State		400	460	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	300	350	

*Surface Mounted on 1" X 1" FR4 Board.

KI1555DL

■ Electrical Characteristics TJ = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-Ch	0.6			V
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch	-0.45			
Gate Body Leakage	I_{GSS}	V_{DS} = 0 V V_{GS} = ±12V	N-Ch			±100	nA
		V_{DS} = 0 V V_{GS} = ±8V	P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0 V	N-Ch			1	
		V_{DS} = -6.4V, V_{GS} = 0 V	P-Ch			-1	
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 85℃	N-Ch			5	μA
		V_{DS} = -6.4V, V_{GS} = 0 V, T_J = 85℃	P-Ch			-5	
On State Drain Currenta	$I_{D(on)}$	V_{DS} ≥5 V, V_{GS} = 4.5 V	N-Ch	1.0			A
		V_{DS} ≤-5 V, V_{GS} = -4.5 V	P-Ch	-1.0			
Drain Source On State Resistance*	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.66A	N-Ch		0.320	0.385	Ω
		V_{GS} = -4.5 V, I_D = -0.57A	P-Ch		0.510	0.600	
		V_{GS} = 2.5 V, I_D = 0.40A	N-Ch		0.560	0.630	
		V_{GS} = -2.5 V, I_D = -0.48A	P-Ch		0.720	0.850	
		V_{GS} = -1.8 V, I_D = -0.20A	P-Ch		1.00	1.200	
Forward Transconductance*	g_{fs}	V_{DS} = 10 V, I_D = 0.66A	N-Ch		1.5		mS
		V_{DS} = -4 V, I_D = -0.57A	P-Ch		1.2		
Diode Forward Voltage*	V_{SD}	I_S = 0.23A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = -0.23A, V_{GS} = 0 V	P-Ch		-0.8	-1.2	
Total Gate Charge	Q_g	N-Channel	N-Ch		0.8	1.2	pC
		V_{DS} = 10 V, V_{GS} = 4.5V, I_D = 0.66A	P-Ch		1.5	2.3	
Gate Source Charge	Q_{gs}		N-Ch		0.06		
		P-Channel	P-Ch		0.17		
Gate Drain Charge	Q_{gd}	V_{DS} = -4 V, V_{GS} = -4.5 V, I_D = -0.57A	N-Ch		0.30		
			P-Ch		0.16		
Turn On Time	$t_{d(on)}$	N- Channel	N-Ch		10	20	ns
		V_{DD} = 10 V, R_L = 20Ω	P-Ch		6	12	
Rise Time	t_r	I_D= 0.5 A, V_{GEN} = 4.5V, R_g = 6 Ω	N-Ch		16	30	
			P-Ch		25	50	
Turn Off Delay Time	$t_{d(off)}$	P-Channel	N-Ch		10	20	
		V_{DD} = -4 V, R_L = 8Ω	P-Ch		10	20	
Fall Time	t_f	I_D= -0.5 A, V_{GEN} = -4.5 V, R_g = 6 Ω	N-Ch		10	20	
			P-Ch		10	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 0.23 A, di/dt = 100 A/μs	N-Ch		20	40	
		I_F = -0.23 A, di/dt = 100 A/μs	P-Ch		20	40	

* Pulse test; pulse width ≤300μs, duty cycle≤2%.