F75375S/F75375SG

Fintek Hardware Monitor IC Datasheet

Release Date: July 2007
Revision: Version 0.26P

F75375 Datasheet Revision History

Version	Date	Page	Revision History
0.20P	2002 May.		Original version
0.21P	2003 Dec		1. Add external clock input function. 2. Add Linear mode for fan speed control
0.22P	2004 Jan	3	Revise pin13 description
0.23P	2004 Feb	15 45 - 46	1.Revise register description of Index01 2.Revise AC/DC characteristics
0.24P	2004 Sep	2	Add key spec.(supply voltage and operating supply current)
0.25P	2005 Apr	23	Support Green package F75375SG and delete version ID register
0.26P	2007 July		Company readdress

LIFE SUPPORT APPLICATIONS

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Table of Contents

1 General Description

F75375S is a system hardware monitoring and automatic fan speed controlling IC specific designed for graphic cards and mini PC etc. The F75375S can monitor several critical hardware parameters of the system, including voltages, temperatures and fan speeds which are very important for the system to work stably and properly.

An 8-bit analog-to-digital converter (ADC) was built inside F75375S. The chip can monitor up to 4 analog voltage inputs, 2 fan tachometer inputs and 2 remote temperature sensors. The remote temperature sensor is suggested to be performed by thermistor, transistor 2N3906 and CPU thermal diode. The F75375S can provide automatic fan speed control so that the system can operate at the minimum acoustic noise. This chip support not only PWM duty mode but also linear mode for fan speed control. Internal oscillator was built in this chip and user can use external clock input if users need accurate fan speed count. Also the users can set up the upper and lower limits (alarm thresholds) of all monitored parameters and this chip can also issue warning messages for system protection when there is something wrong with monitored items.

Through the BIOS or application software, the users can read all the monitored parameters of system all the time. And a pop-up warning can be also activated when the monitored item was out of the proper/pre-setting range. The application software could be Fintek's application software MyGuard™ or other management application software. The F75375S is in the package of 150mil 16-pin SOP and powered by 3.3V.

2 Feature

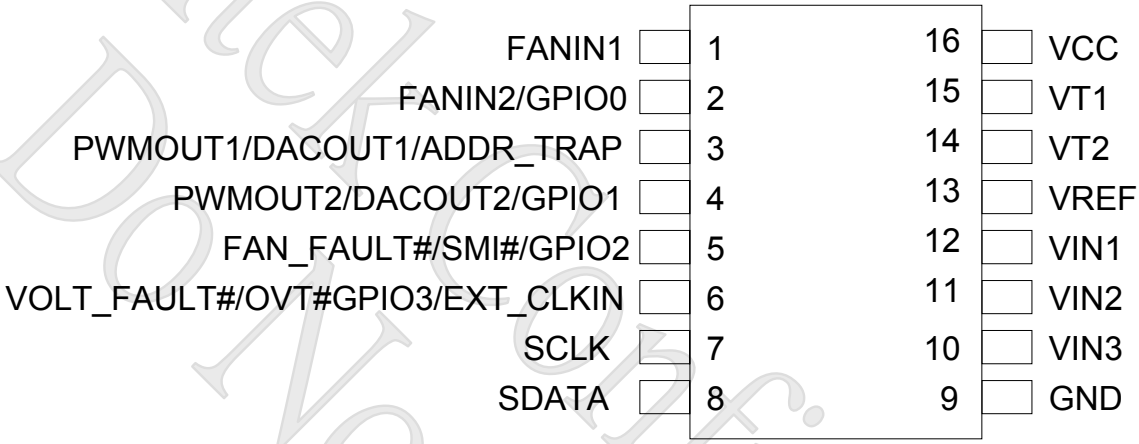
- 4 voltage inputs
- Monitor up to 2 remote temperature sensor
  -- from remote thermistor / transistor / thermal diode (BJT diode-connected)
- Up to 2 fan speed monitoring input and 2 automatic fan speed control
  -- Support both linear and PWM fan speed control (PWMOUT 25KHz support 4 pin fan)
  -- 3 flexible fan speed controlled modes : Manual mode, Speed mode and Temperature mode.
- Programmable limited and setting points(alert threshold) for all monitored items
- Issue FAN_FAULT# or VOLT_FAULT# or OVT# or SMI# signal to activate system protection
- Can use external clock for accurate fan speed count
- Up to 4 general purpose I/O support
- 2-wire I^2C interface
- V_{CC}3V operation and 16SOP package(150mil)

Noted: Patented TW207103 TW207104 TW220442 US6788131 B1

3 Key Specifications

- Supply voltage 3.0~3.6V
- Operating supply current 3 mA typ.

4 Pin Configuration



5 Pin Description

O_8 - TTL level output pin with 8 mA source-sink capability

IN_{ts}/OD_{12} - TTL level bi-directional pin, can select to O.D or OUT by register, with 12mA source-sink capability

I/OD_8 - TTL level bi-directional pin, Open-drain outpu with 8 mA sink capability

I/OD_{16} - TTL level bi-directional pin, Open-drain outpu with 16 mA sink capability

AOUT - Output pin(Analog)

OD_{16} - Open-drain output pin with 16 mA sink capability

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

$IN_{tsd100k}$ - TTL level input pin and schmitt trigger with internal pull down 100K ohm

AIN - Input pin(Analog)

P - Power

◆ Power Pin

Pin No.	Pin Name	Type	Description
16	VCC	P	3.3V power supply voltage input
9	GND	P	GND

◆ Monitoring Items and Fan Speed Control

Pin No.	Pin Name	Type	Description
1	FANIN1	IN_t	0V to +3.3V amplitude fan tachometer input.
2	GPIO0	IN_{ts}/OD_8	(Default) General purpose I/O pin. Default Open drain
	FANIN2	IN_t	0V to +3.3V amplitude fan tachometer input.
3	PWMOUT1	O_{12}	Fan speed control pin. This pin is either PWM-duty mode or Linear mode.
	DACOUT1	AOUT	
	ADDR_TRAP	$IN_{tsd100k}$	Address power on trapping pin. Internal pull down100k ohm. The internal pull-down resistor will be turn-off after power-on trapping.
4	GPIO1	IN_{ts}/OD_{12}	(Default) General purpose I/O pin. Default Open drain
	PWMOUT2	O_{12}	Fan speed control pin. This pin is either PWM-duty mode or Linear mode.
	DACOUT2	AOUT	
10	VIN3	AIN	0V to 2.048V FSR Analog Inputs
11	VIN2	AIN	0V to 2.048V FSR Analog Inputs
12	VIN1	AIN	0V to 2.048V FSR Analog Inputs
14	VT2	AIN	Thermistor / transistor / thermal diode terminal input
15	VT1	AIN	Thermistor / transistor / thermal diode terminal input

◆ Alert Signals and Others

Pin No.	Pin Name	Type	Description
5	GPIO2	IN_{ts}/OD_{14}	(Default) General purpose I/O function. Default pure open drain
	SMI#	OD_{14}	System management interrupt (Pure Open Drain)
	FAN_FAULT#	OD_{14}	This pin will be a logic **LOW** when the fan speed is abnormal.
6	GPIO3	IN_{ts}/OD_8	(Default) General purpose I/O function. Default Open drain
	OVT#	OD_8	Active-Low output. This pin will be a logic **LOW** when the temperature exceeds its limit.
	VOLT_FAULT#	OD_8	Active-Low output. This pin will be a logic **LOW** when the voltage exceeds its limit.
	EXT_CLKIN	IN_t	48MHz External clock input for chip operation source.

13	VREF	AOUT	Reference Voltage.

◆ **Serial Bus Control Pin**

Pin No.	Pin Name	Type	Description
8	SDATA	IN_{ts}/OD_{12}	Serial Bus data.
7	SCLK	IN_{ts}	Serial Bus clock.

6 Functional Description

F75375S is a system hardware monitoring and automatic fan speed controlling IC specific designed for graphic cards. The chip can monitor up to 4 analog voltage inputs, 2 fan tachometer inputs and 2 remote temperature sensors. The remote temperature sensor can be performed by thermistor, transistor and thermal diode. The F75375S can provide automatic fan speed control so that the system can operate at the minimum acoustic noise. Also the users can set up the upper and lower limits (alarm thresholds) of all monitored parameters and this chip can also issue warning messages for system protection when there is something wrong with monitored items.

6.1 Analog Input

For the 8-bit ADC has the 7.8125mv LSB, the maximum input voltage of the analog pin is 2V. Therefore the voltage under 2V (ex:1.5V) can directly connected to these analog inputs. The voltage higher than 2V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC is an exception for it is main power of the F75375S. Therefore 3VCC can directly connect to this chip and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F75375S and the second function is that this voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 50K ohm, so that the internal reduced voltage is half +3.3V.

There are four voltage inputs in the F75375S and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$

where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V_{+12v} will be 1.907V, which is within the tolerance.
As for application circuit, it can be refer to the figure shown as follows.

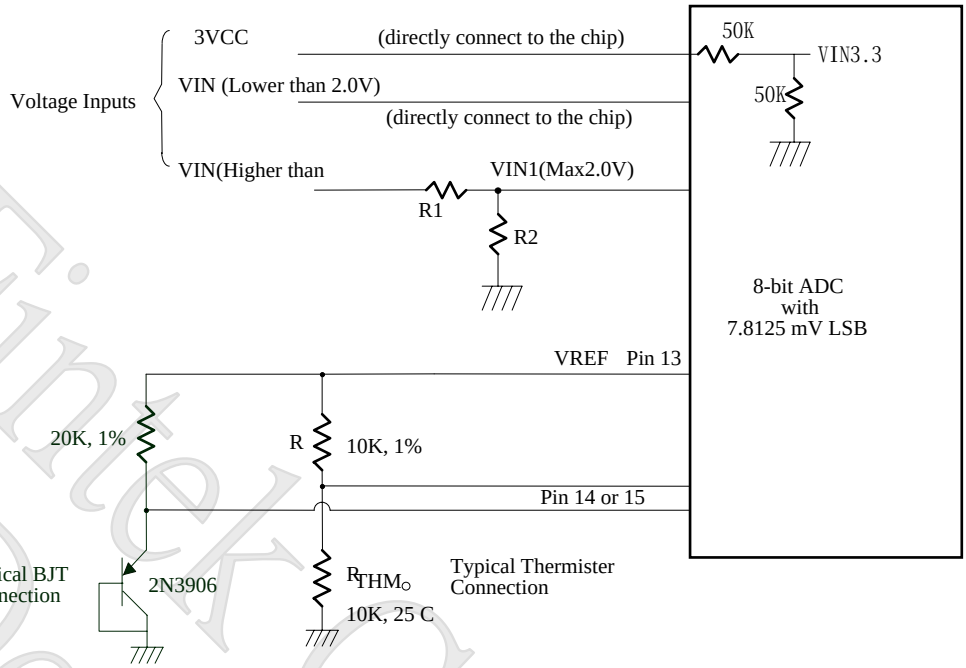


Figure 5-3

6.2 Access Interface

The F75375S provides one serial access interface, Serial Bus, to read/write internal registers. The address of Serial Bus is configurable by using power-on trapping. The pin 3 (PWMOUT1/ADDR_TRAP) is multi-function pin. During power-on, this pin serves as input detection of logic high or logic low. This pin is default pull-down resistor with 100K ohms mapping the Serial Bus address 0x5A (0101_1010). Another Serial Bus address 0x5C (0101_1100) is set when external pull-up resistor with 10K ohms is connected in this pin.

(a) ***Serial bus write to internal address register followed by the data byte***

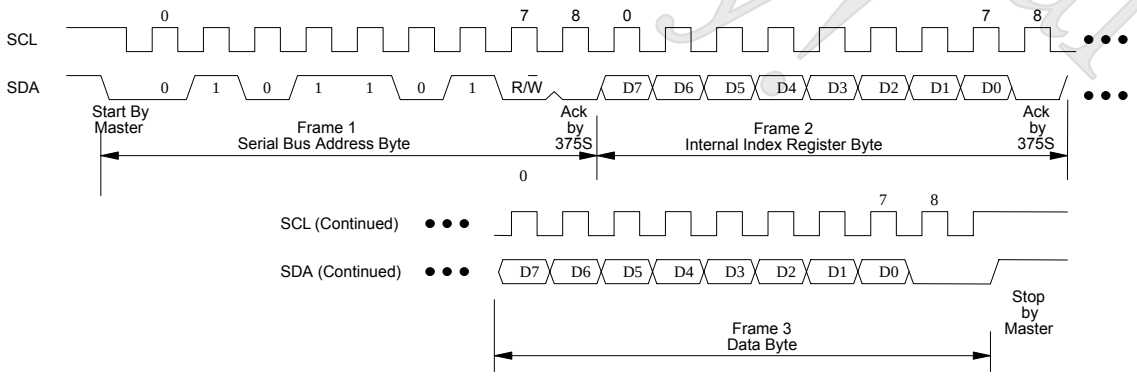


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read form internal address register followed by the data byte

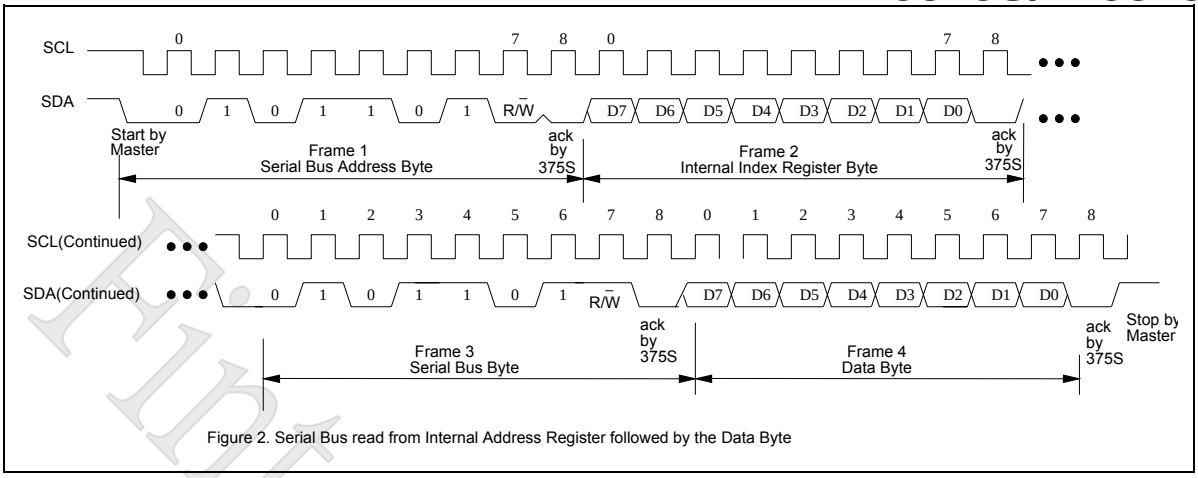


Figure 2. Serial Bus read from Internal Address Register followed by the Data Byte

6.3 Temperature Measurement Machine

The temperature data format is 8-bit two-complement for thermal sensor. The 8-bit temperature data can be obtained by reading through register. The format of the temperature data is show in Table 4-1.

Temperature	8-Bit Digital Output	
	8-Bit Binary	8-Bit Hex
+125°C	0111,1101	7Dh
+25°C	0001,1001	19h
+2°C	0000,0010	02h
+1°C	0000,0001	01h
+0°C	0000,0000	00h
-1°C	1111,1111	FFh
-2°C	1111,1110	FEh
-25°C	1110,0111	E7h
-50°C	1100,1110	CEh

Table 4-1.

Monitor Temperature from thermistor

The F75375S can connect two thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) β value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 5-3, the thermistor is connected by a serial resistor with 10K Ohm, then connected to VREF (pin13).

Monitor Temperature from thermo diode

Also, if the CPU, GPU or external circuits provide thermal diode for temperature monitor, F75375S is capable to these situations. The build-in reference table is for PNP 2N3906, and each different kind of thermal diode should be matched with specific offset and BJT gain. In the Figure 5-3, the 2N3906 PNP is connected by a serial resistor with 20K ohm, then connect to VREF (pin13).

Over Temperature Signal (OVT#)

The F75375S can provide two external thermal sensors to detect temperature. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

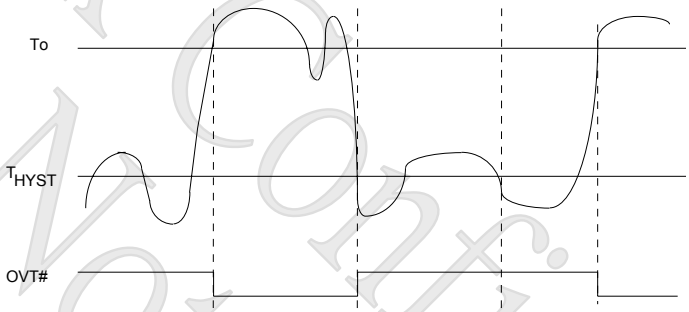


Figure 5-4

Fan

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over VCC. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as follows:

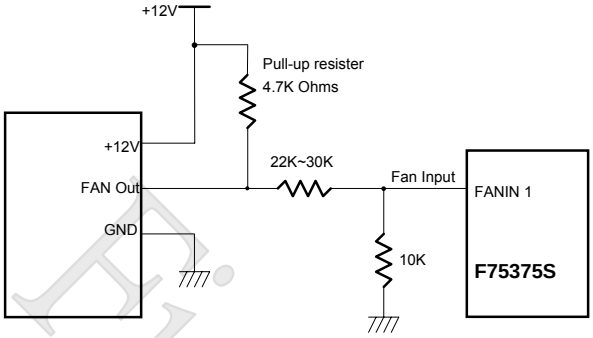


Figure 5-5 Fan with Tach Pull-Up to +12V, or Totern-Pole Output and Register Attenuator

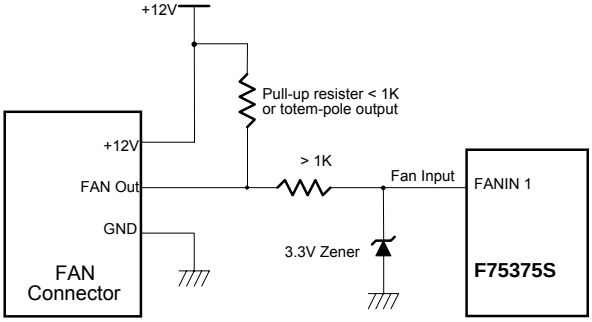


Figure 5-6 Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

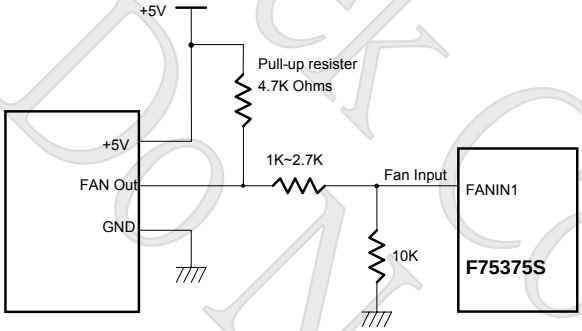
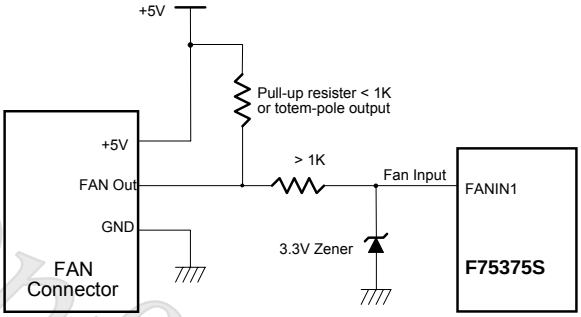


Figure 5-7. Fan with Tach Pull-Up to +5V, or Totern-Pole Output and Register Attenuator



.Figure 5-8 Fan with Tach Pull-Up to +5V, or Totem-Pole Putput and Zener Clamp

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation.

As for fan, it would be best to use 2 pulses tachmeter output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

6.3.1 Fan speed control

The F75375S provides 2 fan speed control methods: 1. LINEAR FAN CONTROL 2. PWM DUTY CYCLE

6.3.1.1 Linear Fan Control

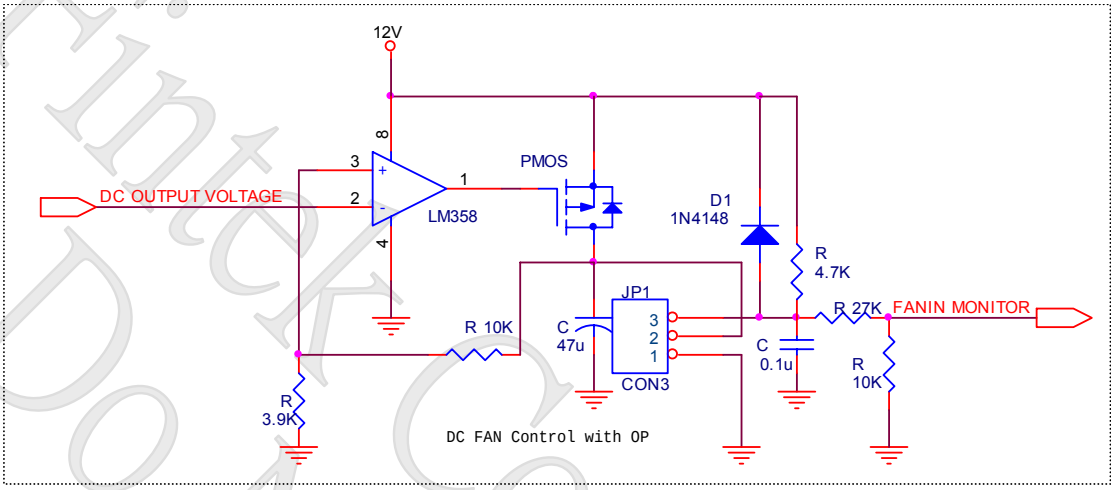
The range of DC output is 0~3.3V, controlled by 8-bit register (CR76 for FAN1 and CR86 for FAN2). 1 LSB is about 0.013V.

The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V.

The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = 3.3 \times \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

And the suggested application circuit for linear fac control would be:



6.3.1.2 PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register which are defined in the CR76h and CR86h. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

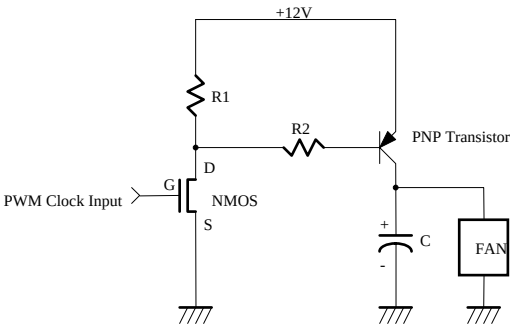


Figure 5-9

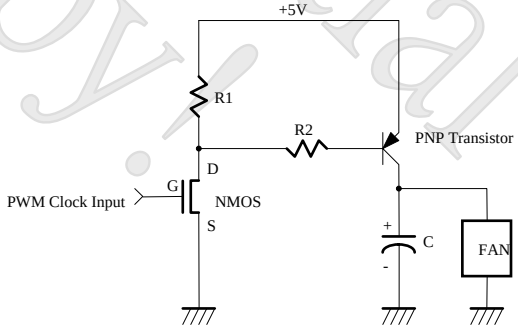


Figure 5-10

6.3.2 Fan speed control mechanism

There are 3 modes to control fan speed and they are manual, fan speed mode and temperature mode. For manual

mode, it generally acts as PWM fan speed control. As for speed mode and temperature mode, they are more intelligent fan speed control and described as below:

6.3.2.1 Fan Speed mode

Fan speed mode is an intelligent method according to expected fan speed pre-setting by BIOS. In the beginning, fan speed will operate at full speed and the F75375S will get the full speed count value. Then fan speed slows down to rotate at about 72.5% (8/11) of full speed. After that, the fan speed will automatically rotate according to the expected fan speed setting by BIOS. The register CR74h and CR75h are used for this mode.

6.3.2.2 Temperature mode

At this mode, F75375S provides the clever system to automatically control fan speed related to temperature of GPU or the system. The F75375S can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take figure 5-11 as example. When temperature setting value is 45,55,65, and 75°C. There are five intervals and each interval is 10°C. The related desired fan speed counts for each interval are 0500h, 0400h, 0300h, 0200h, 0100h. When the temperature is within 55~65°C, the fan speed count 300h will be load into FAN EXPECT COUNTregisters(CR74h~CR75h, CR84h~CR85h). Then, F75375S will adjust PWMOUT duty-cycle to make fan speed match the expected value. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature varying. The F75375S will take charge of all the fan speed control and need no software support.

Figure 5-11

6.3.2.3 PWMOUT Duty-cycle operating process

In both “FAN SPEED” and “TEMPERATURE” modes, F75375S adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is FFFFh, PWMOUT duty-cycle will be set to 00h to turn off fan.

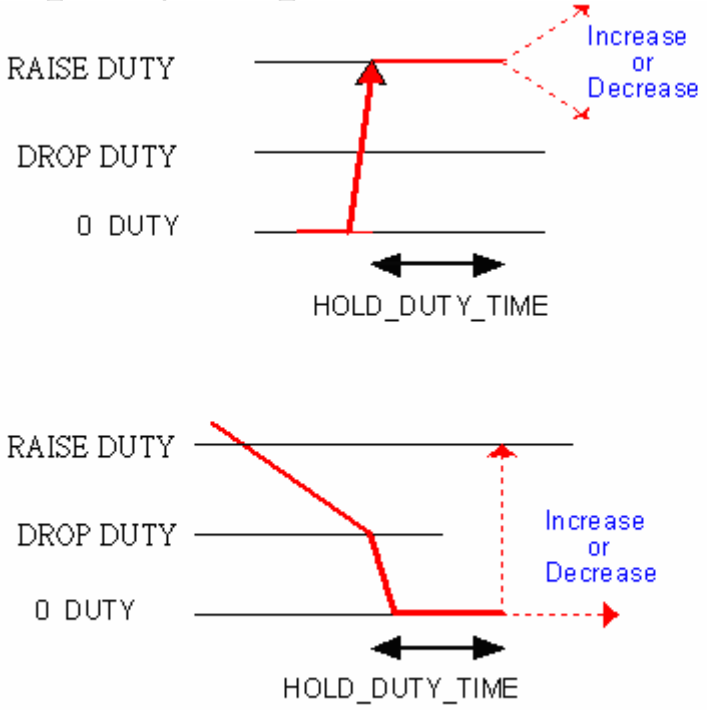
(2). When expected count is 0000h, PWMOUT duty-cycle will be set to FFh to turn on fan with full speed.

(3). If both (1) and (2) are not true and KEEP_DROP_DUTY(see INDEX 60h) is set to 0,

(a). When PWMOUT duty-cycle decrease to DROP_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, F75375S will keep duty-cycle at 00h 3 seconds[1]. After that, F75375S starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the 3 seconds[1] period, F75375S will ignore it.

(b). When PWMOUT duty-cycle increase from 00h to RAISE_DUTY(≠ 00h), F75375S also will keep duty-cycle at RAISE-DUTY 3 seconds[1]. After that, F75375S starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the 3 seconds[1] period, F75375S will ignore it.

Note 1: The period can be programmed at INDEX 6Eh.



6.3.3 FAN_Fault#

Fan_Fault will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 3

seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches FFh, the fan speed count can't reach the fan expected count in time. (Figure 5-12)

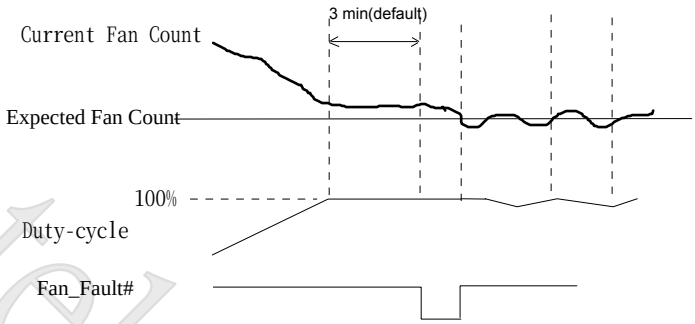


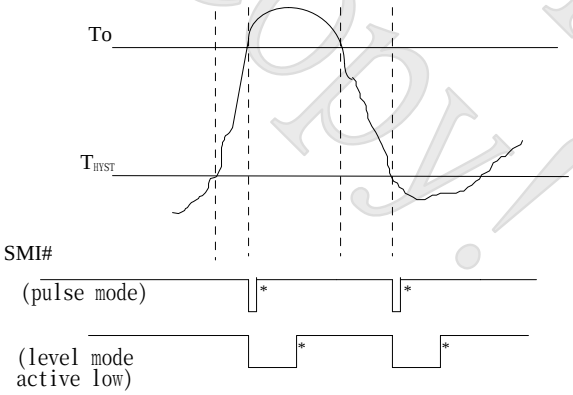
Figure 5-12

(2). After the period of detecting fan full speed, when PWM_Duty > (RAISE_Duty + 5), and current fan count is monitored FFFFh.

6.4 SMI#

6.4.1 Temperature

SMI# interrupt for temperature is shown as figure 5-13. Temperature exceeding high limit or going below hystersis will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

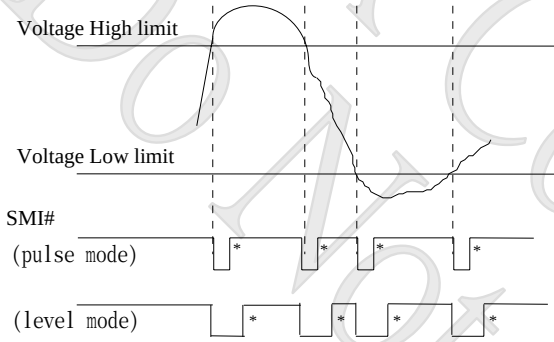
Figure 5-13

6.4.2 Voltage

SMI# interrupt for voltage is shown as figure 5-14. Voltage exceeding or going below high limit will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register. Voltage exceeding or going below low limit will result in the same condition as voltage exceeding or going below high limit.

6.4.3 Fan

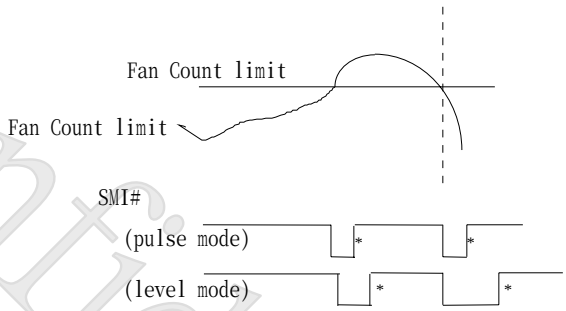
SMI# interrupt for fan is shown as figure 5-15 . SMI# will be asserted when the fan speed count exceeds or goes below the fan limit (Value RAM 2Ch~2Dh, 2Eh~2Fh).



*Interrupt Reset when Interrupt Status Registers are written 1

Voltage SMI# Mode

Figure 5-14



FAN SMI# Mode

Figure 5-15

6.5 VOLT_FAULT# (Voltage Fault Signal)

When voltage leaps from the security range setting by BIOS, the warning signal VOLT_FAULT# will be activated. Shown in figure 5-16

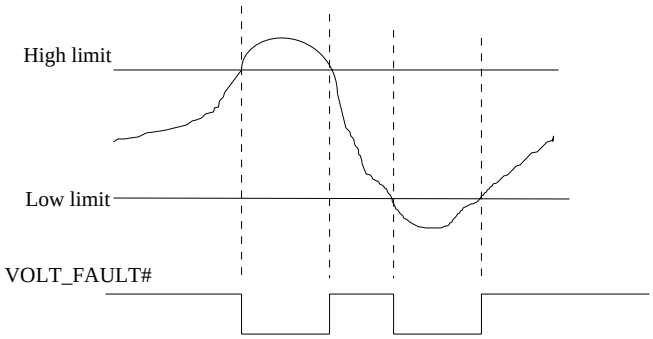


Figure 5-16

7 Register Description

7.1 Configuration Register — Index 00h

Power on default <7:0> = 01h

Bit	Name	Attribute	Description
7	INIT	R/W	Set one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.
6	SOFT_PWDN	R/W	Set this bit to 1 will power down A/D converter circuit. Default is 0
5-1	Reserved	RO	Read back will be 0
0	START	R/W	A one enables startup of monitoring operations; a zero puts the part in standby mode.

7.2 Configuration Register — Index 01h

Power on default <7:0> = 0000_00xx b

Bit	Name	Attribute	Description
7-6	Reserved	RO	Read back will be 0.
5	FAN2_LINEAR_MODE	R/W	Set to 0, FAN2 control mode is PWM Duty-cycle output. Set to 1, FAN2 control mode is LINEAR voltage output.
4	FAN1_LINEAR_MODE	R/W	Set to 0, FAN1 control mode is PWM Duty-cycle output. Set to 1, FAN1 control mode is LINEAR voltage output.

3	T2_MODE	R/W	Set to 1, select VT2 as connected to a BJT. Set to 0, select VT2 as connected to a thermistor. (Default is 0)
2	T1_MODE	R/W	Set to 1, select VT1 as connected to a BJT. Set to 0, select VT1 as connected to a thermistor. (Default is 0)
1	PIN4_MODE	R/W	Pin 4 mode select, set this bit to 1 will enable PWMOUT2 output, else if set this bit to 0, pin 4 will be enable the GPIO1 function.(default) This mode is trappable: When PIN3 trapped to high at power-on, PIN4 is set to PWMOUT2. When PIN3 trapped to low at power-on, PIN4 is set to GPIO1.
0	PIN2_MODE	R/W	Pin 2 mode select, set this bit to 1 will enable FANIN2 input, if set this bit to 0 pin 2 will be enable the GPIO0 function.(default). This mode is trappable: When PIN3 trapped to high at power-on, PIN2 is set to FANIN2. When PIN3 trapped to low at power-on, PIN2 is set to GPIO0.

7.3 Configuration Register — Index 02h

Power on default <7:0> = xx00_00x0 b

Bit	Name	Attribute	Description
7-6	PIN5_MODE	R/W	00: pin5 function is GPIO2 01: pin5 is used as SMI 10: pin5 is used as Fan fault function 11: LED out(1Hz/0.5Hz select by bit2) This mode is trappable: When PIN3 trapped to high at power-on, PIN5 is set to Fan fault function. When PIN3 trapped to low at power-on, PIN5 is set to GPIO2.
5	SMI_MODE	R/W	If set to 0, SMI will be level mode else if this bit set to 1, SMI will be pulse mode.
4	SMI_LEVEL	R/W	When set this bit to 0 SMI is low active (default). if set to 1 SMI is high active
3	Reserved	R/W	
2	LED_FREQ	R/W	When set this bit to 1 fan fault LED output frequency will be 0.5HZ, else is 1Hz(default)

1	F_FAULT_MODE	R/W	When set this bit to 0 the fan fault will be level mode, else if set to 1 the fan fault will indicate by LED function(1Hz or 0.5Hz) the LED frequency can set by REG02H bit2. This mode is trappable: When PIN3 trapped to high at power-on, this mode is set to LED function. When PIN3 trapped to low at power-on, this mode is set to level mode.
0	F_FAULT_LEVEL	R/W	When set this bit to 0 fan fault is low active (default). if set to 1 fan fault is high active

7.4 Configuration Register — Index 03h

Power on default <7:0> = xx00_0000 b

Bit	Name	Attribute	Description
7	PIN6_MODE	R/W	00: pin6 function is GPIO3. 01: pin6 is used as OVT 10: pin6 is used as Voltage fault function 11: pin6 is as operating clock input function. The External clock should be 48MHz. This input clock will be the clock source of the whole chip. This mode is trappable: When PIN3 trapped to high at power-on, PIN6 is set to OVT. When PIN3 trapped to low at power-on, PIN6 is set to GPIO3.
5	OVT_LEVEL	R/W	When set this bit to 0 OVT is low active (default), else if set to 1 OVT is high active
3-4	OVT_QUEUE	R/W	OVT queue is use to filter the temperature noise, it define the times of the event when OVT is asserted. 00: 1 times 01: 3 times 10: 5 times 11: 7 times
2	V_FAULT_LEVEL	R/W	Voltage fault level. When set this bit to 0 voltage fault is low active (default). if set to 1 fan fault is high active
1-0	V_FAULT_QUEUE	R/W	Voltage fault queue. It is used to filter the voltage noise, the follow define the times of the event when VOLT_FAULT is asserted. 00: 1 times 01: 3 times

			10: 5 times 11: 7 times

7.5 Serial Bus Address Register — Index 04h

Power on default: 5Ah or 5Ch.

Bit	Name	Attribute	Description
7-0	SERIAL_ADDR	RO	Serial Bus address. Power on default value depends on the status of pin3(PWMOUT1/ADDR_TRAP) at the moment of power on. If the pin status is 1, the value is 5Ch, otherwise is 5Ah. To read or write registers of this chip, the serial address must match this value. This register can be written by a sequence value to this register : A9h, C3h, XXh, in which XXh will be the value being written to this register; this is to protect the register from being written by accident.

7.6 Value RAM — Index 10h- 2Fh

Address 10-3F	Attribute	Default Value	Description
10h	RO		VCC reading. The unit of reading is 8mV.
11h	RO		V1 reading. The unit of reading is 8mV.
12h	RO		V2 reading. The unit of reading is 8mV.
13h	RO		V3 reading. The unit of reading is 8mV.
14h	RO		Temperature 1 reading. The unit of reading is 1°C.
15h	RO		Temperature 2 reading. The unit of reading is 1°C.
16h	RO		FAN1 count reading (MSB)
17h	RO		FAN1 count reading (LSB)
18h	RO		FAN2 count reading (MSB)
19h	RO		FAN2 count reading (LSB)
1Ah~1Eh			Reserved
20h	R/W	FFh	VCC High Limit. The unit is 8mV.
21h	R/W	00h	VCC Low Limit. The unit is 8mV.
22h	R/W	FFh	V1 High Limit. The unit is 8mV.
23h	R/W	00h	V1 Low Limit. The unit is 8mV.
24h	R/W	FFh	V2 High Limit. The unit is 8mV.

25h	R/W	00h	V2 Low Limit. The unit is 8mV.
26h	R/W	FFh	V3 High Limit. The unit is 8mV.
27h	R/W	00h	V3 Low Limit. The unit is 8mV.
28h	R/W	3Ch	Temperature sensor 1 High Limit. The unit is 1°C.
29h	R/W	37h	Temperature sensor 1 Hysteresis Limit. The unit is 1°C.
2A h	R/W	3Ch	Temperature sensor 2 High Limit. The unit is 1°C.
2Bh	R/W	37h	Temperature sensor 2 Hysteresis Limit. The unit is 1°C.
2Ch	R/W	FFh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
2Dh	R/W	FFh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
2Eh	R/W	FFh	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
2Fh	R/W	FFh	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

7.7 IRQ/SMI# ENABLE Register 1 — Index 30h

Power on default: 00h

Bit	Name	Attribute	Description
7	EN_FAN2_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt
6	EN_FAN1_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.
5	EN_VT2_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.
4	EN_VT1_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.

3	EN_V3_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.
2	EN_V2_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.
1	EN_V1_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.
0	EN_VCC_SMI	R/W	A one enables the corresponding interrupt status bit for SMI# interrupt.

7.8 Interrupt Status Register 1 — Index 31h

Power on default: 00h

Bit	Name	Attribute	Description
7	FAN2_STS	R/W	A one indicates fan2 count limit has been exceeded. Write 1 to clear this bit, write 0 will be ignored.
6	FAN1_STS	R/W	A one indicates fan1 count limit has been exceeded. Write 1 to clear this bit, write 0 will be ignored.
5	VT2_STS	R/W	A one indicates a high limit of VT2 has been exceeded from temperature sensor. Write 1 to clear this bit, write 0 will be ignored.
4	VT1_STS	R/W	A one indicates a high limit of VT1 has been exceeded from temperature sensor. Write 1 to clear this bit, write 0 will be ignored.
3	V3_STS	R/W	A one indicates a high or low limit of VIN3 has been exceeded. Write 1 to clear this bit, write 0 will be ignored.
2	V2_STS	R/W	A one indicates a high or low limit of VIN2 has been exceeded. Write 1 to clear this bit, write 0 will be ignored.
1	V1_STS	R/W	A one indicates a high or low limit of VIN1 has been exceeded. Write 1 to clear this bit, write 0 will be ignored.
0	VCC_STS	R/W	A one indicates a high or low limit of VCC has been exceeded. Write 1 to clear this bit, write 0 will be ignored.

7.9 Real Time Status Register 1 — Index 32h

Power on default: 00h

Bit	Name	Attribute	Description

7	FAN2EXC	R/W	A one indicates fan2 count limit has been exceeded. A zero indicates fan2 count is in the safe region.
6	FAN1EXC	R/W	A one indicates fan1 count limit has been exceeded. A zero indicates fan1 count is in the safe region.
5	VT2EXC	R/W	A one indicates a high limit of VT2 has been exceeded. A zero indicates VT2 is below the hysteresis limit.
4	VT1EXC	R/W	A one indicates a high limit of VT1 has been exceeded. A zero indicates VT1 is below the hysteresis limit.
3	V3EXC	R/W	A one indicates a high or low limit of VIN3 has been exceeded. A zero indicates VIN3 is in the safe region.
2	V2EXC	R/W	A one indicates a high or low limit of VIN2 has been exceeded. . A zero indicates VIN2 is in the safe region.
1	V1EXC	R/W	A one indicates a high or low limit of VIN1 has been exceeded. . A zero indicates VIN1 is in the safe region.
0	VCCEXC	R/W	A one indicates a high or low limit of VCC has been exceeded. . A zero indicates VCC is in the safe region.

7.10 IRQ/SMI# ENABLE Register 2 — Index 33h

Power on default: 00h

Bit	Name	Attribute	Description
7-4	Reserved	RO	
3	EN_NZF2_SMI	R/W	Non-Zero-PWM FAN2 SMI enable bit. A zero disables the corresponding interrupt status for SMI# interrupt.
2	EN_NZF1_SMI	R/W	Non-Zero-PWM FAN1 SMI enable bit. A zero disables the corresponding interrupt status for SMI# interrupt.
1	EN_TARF2_SMI	R/W	Target fan2 SMI enable bit. A zero disables the corresponding interrupt status bit for SMI# interrupt
0	EN_TARF1_SMI	R/W	Target fan1 SMI enable bit. A zero disables the corresponding interrupt status bit for SMI# interrupt

7.11 Interrupt Status Register 2 — Index 34h

Power on default: 00h

Bit	Name	Attribute	Description

7-4	Reserved		
3	STS_NZ_FAN2	R/W	A one indicates fan2's PWMOUT duty-cycle is above (RAISE_DUTY + 5) and the current FAN speed is 0 (ie. Fan Count = FFFFh).
2	STS_NZ_FAN1	R/W	A one indicates fan1's PWMOUT duty-cycle is above (RAISE_DUTY + 5) and the current FAN speed is 0 (ie. Fan Count = FFFFh).
1	STS_TAR_FAN2	R/W	A one indicates fan2 reading count is over then fan2 expect count, and the PWMOUT2 duty cycle is full more then the FAN FAULT TIME. Write 1 to clear this bit, write 0 will be ignored.
0	STS_TAR_FAN1	R/W	A one indicates fan1 reading count is over then fan1 expect count, and the PWMOUT1 duty cycle is full more then the FAN FAULT TIME. Write 1 to clear this bit, write 0 will be ignored.

7.12 FAN_FAULT/VOLT_FAULT/OVT ENABLE Register — Index 35h

Power on default: 00h

Bit	Name	Attribute	Description
7	EN_F2_FAULT	R/W	A one enables the fan2 fault status to be indicated in pin FAN_FUALT. This bit is trappable. When PIN3 trapped to high at power-on, this bit is set to 1. When PIN3 trapped to low at power-on, this bit is set to 0.
6	EN_ F1_FAULT	R/W	A one enables the fan1 fault status to be indicated in pin FAN_FUALT. This bit is trappable. When PIN3 trapped to high at power-on, this bit is set to 1. When PIN3 trapped to low at power-on, this bit is set to 0.
5	EN_T2_OVT	R/W	A one enables the VT2 fault status to be indicated in pin OVT. This bit is trappable. When PIN3 trapped to high at power-on, this bit is set to 1. When PIN3 trapped to low at power-on, this bit is set to 0.
4	EN_T1_OVT	R/W	A one enables the VT1 fault status to be indicated in pin OVT. This bit is trappable. When PIN3 trapped to high at power-on, this bit is set to 1. When PIN3 trapped to low at power-on, this bit is set to 0.
3	EN_V3_FAULT	R/W	A one enables the V3 fault status to be indicated in pin VOLT_FUALT pin.
2	EN_V2_FAULT	R/W	A one enables the V2 fault status to be indicated in pin VOLT _FUALT.
1	EN_V1_FAULT	R/W	A one enables the V1 fault status to be indicated in pin VOLT _FUALT.

0	EN_VCC_FAULT	R/W	A one enables the VCC fault status to be indicated in pin VOLT _FUALT.

7.13 REAL TIME Fault Status Register 1 — Index 36h

Power on default: 00h

Bit	Name	Attribute	Description
7	FAN2_FAULT	RO	A one indicates fan2 count limit exceeding.
6	FAN1_FAULT	RO	A one indicates fan1 count limit exceeding.
5	VT2_OVT	RO	This bit will set to 1 from high limit of VT2 is exceeded until the temperature2 is under the VT2 hysteresis Limit
4	VT1_OVT	RO	This bit will set to 1 from high limit of VT1 is exceeded until the temperature1 is under the VT1 hysteresis Limit
3	V3_FAULT	RO	A one indicates a high or low limit of V3 exceeding.
2	V2_FAULT	RO	A one indicates a high or low limit of V2 exceeding.
1	V1_FAULT	RO	A one indicates a high or low limit of V1 exceeding.
0	VCC_FAULT	RO	A one indicates a high or low limit of VCC exceeding.

7.14 NON-ZERO-PWM FAN FAULT ENABLE Register — Index 37h

Power on default: 00h

Bit	Name	Attribute	Description
7-3	Reserved	RO	
1	EN_NZF2_FAULT	R/W	A one enables the FAN2 Non-zero-PWM fault status to be indicated in pin FAN_FUALT. This bit is trappable. When PIN3 trapped to high at power-on, this bit is set to 1. When PIN3 trapped to low at power-on, this bit is set to 0.
0	EN_NZF1_FAULT	R/W	A one enables the FAN1 Non-zero-PWM fault status to be indicated in pin FAN_FUALT. This bit is trappable. When PIN3 trapped to high at power-on, this bit is set to 1. When PIN3 trapped to low at power-on, this bit is set to 0.

7.15 NON-ZERO-PWM REAL TIME Fault Status Register 2 — Index 38h

Power on default: 00h

Bit	Name	Attribute	Description

7	Reserved	RO	
1	FAN2NZEXC2	RO	A one indicates FAN2 Non-zero-PWM fault.
0	FAN1NZEXC2	RO	A one indicates Fan1 Non-zero-PWM fault.

7.16 CHIPID(1) Register – Index 5Ah

Power-on default [7:0] =0000_0011b

Bit	Name	Attribute	Description
7-0	CHIPID	RO	Chip ID, High byte (8'h03).

7.17 CHIPID(2) Register – Index 5Bh

Power-on default [7:0] =0000_0110b

Bit	Name	Attribute	Description
7-0	CHIPID	RO	Chip ID, Low byte (8'h06).

7.18 VENDOR ID(1) Register – Index 5Dh

Power-on default [7:0] =0001_1001b

Bit	Name	Attribute	Description
7-0	VENDOR1	RO	Vendor ID, 8'h19

7.19 VENDOR ID(2) Register – Index 5Eh

Power-on default [7:0] =0011_0100b

Bit	Name	Attribute	Description
7-0	VENDOR2	RO	Vendor ID, 8h34

7.20 Reset Timer Control Register -- Index 60h

Power on default: 00h

Bit	Name	Attribute	Description
7-6	FAN2_MODE	R/W	**00:** FAN2 operates in **SPEED** mode. PWMOUT2 duty-cycle is automatically adjusted according to FAN2 EXPECT register. **01:** FAN2 operates in **TEMPERATURE** mode. PWMOUT2 duty-cycle

			is automatically adjusted according to FAN2 EXPECT register, which will be automatically loaded into preset values according to the current temperature. (When PIN3 power-on trapped to 1, this mode is selected after power-on.) **1X:** FAN2 operates in **MANUAL** mode. Software set the PWMOUT2 duty-cycle directly.
5-4	FAN1_MODE	R/W	**00:** FAN1 operates in **SPEED** mode. PWMOUT1 duty-cycle is automatically adjusted according to FAN1 EXPECT register. **01:** FAN1 operates in **TEMPERATURE** mode. PWMOUT1 duty-cycle is automatically adjusted according to FAN1 EXPECT register, which will be automatically loaded into preset values according to the current temperature. (When PIN3 power-on trapped to 1, this mode is selected after power-on.) **1X:** FAN1 operates in **MANUAL** mode. Software set the PWMOUT1 duty-cycle directly.
3	Reserved		
2	KEEP_DROP_DUTY2	R/W	Set to 1, keep PWMOUT2 duty-cycle decrease to DROP duty and hold.
1	KEEP_DROP_DUTY1	R/W	Set to 1, keep PWMOUT1 duty-cycle decrease to DROP duty and hold.
0	EN_RESET_TIMER	R/W	Set to 1, enable interface_idle timer. Set to 0, disable the timer. When the timer is enabled, if software doesn't access the this chip through GP_CLK and GP_DATA, the reset timer starts to count down according to the value set in INDEX 62H. When it counts down to zero, INDEX[72H, 73H] will be loaded into INDEX[74H,75H].

7.21 Fan Fault Time Register -- Index 61h

Power on default: 02h

Bit	Name	Attribute	Description
7-0	F_FAULT_TIME	R/W	This register determines the time of fan fault. Two conditions cause fan fault event: (1). When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in the time. (2). When PWM_Duty reaches 00h, if the fan speed count can't reach the fan expect count in the time.

			The unit of this register is 1 second. The default value is 3 seconds. (Set to 0 , means 1 seconds. Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….)

7.22 RESET-Timer Time Register -- Index 62h

Power on default: 09h

Bit	Name	Attribute	Description
7-0	F_RESET_TIME	R/W	Interface idle time. The unit of this register is 1 minute. The default value is 10 minute. More details in INDEX 60H.

7.23 FAN STEP Time defined Register -- Index 63h

Power on default: 00h

Bit	Name	Attribute	Description
7-4	FAN_STEP2	R/W	This value determines the increasing or decreasing speed of PWM_Duty. The unit is 0.1 second. (Set to 0, means 0.1 second per step. Set to 1, means 0.2 second per step….)
3:0	FAN_STEP1	R/W	This value determines the increasing or decreasing speed of PWM_Duty The unit is 0.1 second.

7.24 VT1 OFFSET Register -- Index 64h

Power on default: 00h

Bit	Name	Attribute	Description
7-0	T1OFFSET	R/W	VT1 temperature offset register. The offset value is representative in 2's complement. The real temperature value will be added by this offset and then will be put into temperature reading (Value RAM 14h). The offset ranges from -128ºC to +127ºC. 7Fh : +127ºC. 01h : +5ºC. 00h : +0ºC.

			FFh : -1ºC. FEh : -2ºC. 80h : -128ºC.

7.25 VT2 OFFSET Register -- Index 65h

Power on default: 00h

Bit	Name	Attribute	Description
7-0	T2OFFSET	R/W	VT2 temperature offset register. The offset value is representative in 2's complement. The real temperature value will be added by this offset and then will be put into temperature reading (Value RAM 15h). The offset ranges from -128ºC to +127ºC. 7Fh : +127ºC. 01h : +5ºC. 00h : +0ºC. FFh : -1ºC. FEh : -2ºC. 80h : -128ºC.

7.26 PWMOUT1 RAISE DUTY-CYCLE — Index 69h

Power on default: 30h

Bit	Name	Attribute	Description
7-0	FAN1_RAISE_DUTY	R/W	PWMOUT1 will increase duty-cycle from 0 to this value directly.

7.27 PWMOUT2 RAISE DUTY-CYCLE — Index 6Ah

Power on default: 30h

Bit	Name	Attribute	Description
7-0	FAN2_RAISE_DUTY	R/W	PWMOUT2 will increase duty-cycle from 0 to this value directly

7.28 PWMOUT1 DROP DUTY-CYCLE — Index 6Bh

Power on default: 10h

Bit	Name	Attribute	Description
7-0	FAN1_DROP_DUTY	R/W	PWMOUT1 will decrease duty-cycle to 0 from this value directly or keep duty-cycle in this value when CR60 bit1 set to 1.

7.29 PWMOUT2 DROP DUTY-CYCLE — Index 6Ch

Power on default: 10h

Bit	Name	Attribute	Description
7-0	FAN2_DROP_DUTY	R/W	PWMOUT2 will decrease duty-cycle to 0 from this value directly or keep duty-cycle in this value when CR60 bit2 set to 1.

7.30 FAN1 full speed Count Register 1— Index71h

Power on default: 1111_1111b

Bit	Name	Attribute	Description
7-0	FAN1_FULL (LSB)	RO	When power on, the PWMOUT1 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN1 signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN1 after power on, the PWMOUT1 will keep outputting FFh duty cycle.

7.31 FAN1 expect timeout speed Register — Index 72h

Power on default: 0000_0001b

Bit	Name	Attribute	Description
7-0	FAN1_TSPEED (MSB)	R/W	The fan1 timeout count, when software idle timeout is happen, this count will be load to FAN1 expect register. The default count is 11/8 of FAN1_FULL reg. (73% of full speed). This register is only valid at **HALF-AUTOMATIC(SPEED)** mode.

7.32 FAN1 expect timeout speed Register — Index 73h

Power on default: 0101_1101b

Bit	Name	Attribute	Description
7-0	FAN1_TSPEED (LSB)	R/W	The fan1 timeout count, when software idle timeout is happen, this count will be load to FAN1 expect register. The default count is 11/8 of FAN1_FULL reg. (73% of full speed). This register is only valid at **HALF-AUTOMATIC(SPEED)** mode.

7.33 FAN1 expect count Register-- Index 74h

Power on default [7:0] = 0000_0001b

Bit	Name	Attribute	Description
7-0	FAN1_EXPECT (MSB)	R/W	User expect fan1 count value, program this register to control the expect fan1 speed

7.34 FAN1 expect count Register-- Index 75h

Power on default [7:0] = 0101_1101b

Bit	Name	Attribute	Description
7-0	FAN1_EXPECT (LSB)	R/W	User expect fan1 count value, program this register to control the expect fan1 speed.

7.35 FAN1 PWM_duty -- Index 76h

Power on default: 1111_1111b

Bit	Name	Attribute	Description
7-0	PWM_DUTY1	R/W	PWMOUT1 duty cycle. This register is programmable at Manual mode. At SPEED or TEMPERATURE mode, this register reflects current PWMOUT duty-cycle.

7.36 FAN1 Non-zero-PWM Waiting Time -- Index 77h

Power on default: 05h

Bit	Name	Attribute	Description

7-0	F1_NZ_WAIT	R/W	This value determines the gap of current PWMOUT1 duty-cycle and FAN1_RAISE_DUTY. After current PWMOUT1 duty-cycle is larger than (FAN1_RAISE_DUTY + F1_NZ_WAIT), it starts to compare if the current fan count equals to FFFFh, which is one of the condition of FAN1 Non-zero-PWM fault.

7.37 FAN1 Expect Count Tolerance -- Index 78h

Power on default: 0Ah

Bit	Name	Attribute	Description
7-4	Reserved		
3-0	FAN1_EXPTOL	R/W	This value determines the tolerance of fan expect count. When (1). FAN1 current count > (FAN1_EXPECT + FAN1_EXPTOL), Increasing PWM duty. (2). FAN1 current count < (FAN1_EXPECT – FAN1_EXPTOL), Decreasing PWM duty.

7.38 FAN1 Expect Count High Boundary(MSB) -- Index 79h

Power on default: 0Ah

Bit	Name	Attribute	Description
7-0	FAN1_EXPECT_H[15:8]	RO	The MSB of FAN1_EXPECT + FAN1_EXPTOL

7.39 FAN1 Expect Count High Boundary(LSB) -- Index 7Ah

Power on default: 0Ah

Bit	Name	Attribute	Description
7-0	FAN1_EXPECT_H[7:0]	RO	The LSB of FAN1_EXPECT + FAN1_EXPTOL

7.40 FAN1 Expect Count Low Boundary(MSB) -- Index 7Bh

Power on default: 01h

Bit	Name	Attribute	Description
7-0	FAN1_EXPECT_L[15:8]	RO	The MSB of FAN1_EXPECT - FAN1_EXPTOL

7.41 FAN1 Expect Count Low Boundary(LSB) -- Index 7Ch

Power on default: 53h

Bit	Name	Attribute	Description
7-0	FAN1_EXPECT_L[7:0]	RO	The LSB of FAN1_EXPECT - FAN1_EXPTOL

7.42 FAN1 PWMOUT CLOCK FREQUENCY SELECT -- Index 7Dh

Power on default: 53h

Bit	Name	Attribute	Description
7-3	Reserved		
2	FAN1_INV	R/W	Set to 1, invert the signal of PWMOUT1.
1-0	FAN1_PWMCLK_SEL	R/W	Select PWMOUT1 output frequency. 00 : 5.85K Hz 01 : 26.56K Hz 10 : 187.5K Hz 11 : 5.85K Hz

7.43 FAN2 Full speed Register 0 — Index 80h

Power on default: 0000_0000b

Bit	Name	Attribute	Description
7-0	FAN2_FULL(MSB)	R/W	While PIN4 is set to PWMOUT mode, the PWMOUT2 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN1 signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN2 after power on, the PWMOUT2 will

			keep outputting FFh duty cycle.

7.44 FAN2 full speed Register 1— Index 81h

Power on default: 1111_1111b

Bit	Name	Attribute	Description
7-0	FAN2_FULL (LSB)	R/W	While PIN4 is set to PWMOUT mode, the PWMOUT2 will output full duty cycle (FFh) to enable system FAN. After 15 seconds, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register.

7.45 FAN2 expect timeout speed Register — Index 82h

Power on default: 0000_0001b

Bit	Name	Attribute	Description
7-0	FAN2_TSPEED	R/W	The fan2 timeout count, when software idle timeout is happen, this count will be load to FAN1 expect register. The default count is 11/8 of FAN2_FULL reg. (73% of full speed). This register is only valid at **HALF-AUTOMATIC(SPEED)** mode.

7.46 FAN2 expect timeout speed Register — Index 83h

Power on default: 0101_1101b

Bit	Name	Attribute	Description
7-0	FAN2_TSPEED (LSB)	R/W	The fan2 timeout count, when software idle timeout is happen, this count will be load to FAN2 expect register. The default count is 11/8 of FAN2_FULL reg. (73% of full speed). This register is only valid at **HALF-AUTOMATIC(SPEED)** mode.

7.47 FAN2 expect count Register-- Index 84h

Power on default [7:0] = 0000_0001b

Bit	Name	Attribute	Description
7-0	FAN2_EXPECT (MSB)	R/W	User expect fan2 count value, program this register to control the expect fan2 speed

7.48 FAN2 expect count Register-- Index 85h

Power on default [7:0] = 0101_1101b

Bit	Name	Attribute	Description
7-0	FAN2_EXPECT (LSB)	R/W	User expect fan2 count value, program this register to control the expect fan2 speed

7.49 PWM_duty -- Index 86h

Power on default: 1111_1111b

Bit	Name	Attribute	Description
7-0	PWM_DUTY2	R/W	PWMOUT2 duty cycle. This register is programmable at MANUAL mode. At SPEED or TEMPERATURE mode, this register reflects current PWMOUT duty-cycle.

7.50 FAN2 Non-zero-PWM Waiting Time -- Index 87h

Power on default: 05h

Bit	Name	Attribute	Description
7-0	F2_NZ_WAIT	R/W	This value determines the gap of current PWMOUT2 duty-cycle and FAN2_RAISE_DUTY. After current PWMOUT2 duty-cycle is larger than (FAN2_RAISE_DUTY + F2_NZ_WAIT), it starts to compare if the current fan count equals to FFFFh, which is one of the condition of FAN2 Non-zero-PWM fault.

7.51 FAN2 Expect Count Tolerance -- Index 88h

Power on default: 0Ah

Bit	Name	Attribute	Description
7-4	Reserved		
3-0	FAN2_EXPTOL	R/W	This value determines the tolerance of fan expect count. When (1). FAN2 current count > (FAN2_EXPECT + FAN2_EXPTOL), Increasing PWM duty.

			(2). FAN2 current count < (FAN2_EXPECT – FAN2_EXPTOL), Decreasing PWM duty.

7.52 FAN2 Expect Count High Boundary(MSB) -- Index 89h

Power on default: 0Ah

Bit	Name	Attribute	Description
7-0	FAN2_EXPECT_H[15:8]	RO	The MSB of FAN2_EXPECT + FAN2_EXPTOL

7.53 FAN2 Expect Count High Boundary(LSB) -- Index 8Ah

Power on default: 0Ah

Bit	Name	Attribute	Description
7-0	FAN2_EXPECT_H[7:0]	RO	The LSB of FAN2_EXPECT + FAN2_EXPTOL

7.54 FAN2 Expect Count Low Boundary(MSB) -- Index 8Bh

Power on default: 01h

Bit	Name	Attribute	Description
7-0	FAN2_EXPECT_L[15:8]	RO	The MSB of FAN2_EXPECT - FAN2_EXPTOL

7.55 FAN2 Expect Count Low Boundary(LSB) -- Index 8Ch

Power on default: 53h

Bit	Name	Attribute	Description
7-0	FAN2_EXPECT_L[7:0]	RO	The LSB of FAN2_EXPECT - FAN2_EXPTOL

7.56 FAN2 PWMOUT CLOCK FREQUENCY SELECT -- Index 8Dh

Power on default: 53h

Bit	Name	Attribute	Description
7-3	Reserved		
2	FAN2_INV	R/W	Set to 1, invert the signal of PWMOUT2.
1-0	FAN2_PWMCLK_SEL	R/W	Select PWMOUT2 output frequency. 00 : 5.85K Hz 01 : 26.56K Hz 10 : 187.5K Hz 11 : 5.85K Hz

7.57 GPIOx Output Control Register – Index 90h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-4	Reserved	RO	Read back will be 0;
3	GPIO3_OCTRL	R/W	GPIO3 output control. Set to 1 for output function. Set to 0 for input function(default).
2	GPIO2_OCTRL	R/W	GPIO2 output control. If this pin serves as IRQ/SMI#, this bit has no effect. Set to 1 for output function. Set to 0 for input function(default).
1	GPIO1_OCTRL	R/W	GPIO1 output control. Set to 1 for output function. Set to 0 for input function(default).
0	GPIO0_OCTRL	R/W	GPIO0 output control. Set to 1 for output function. Set to 0 for input function(default).

7.58 GPIOx Output Data Register – Index 91h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-4	Reserved	RO	Read back will be 0;
3	GPIO3_ODATA	R/W	GPIO3 output data.
2	GPIO2_ODATA	R/W	GPIO2 output data.
1	GPIO1_ODATA	R/W	GPIO1 output data.
0	GPIO0_ODATA	R/W	GPIO0 output data.

7.59 GPIO1x Input Status Register – Index 92h

Power-on default [7:0] = N.A.

Bit	Name	Attribute	Description
7-4	Reserved	RO	Read back will be 0
3	GPIO3_PSTS	RO	Read the GPIO3 data on the pin.
2	GPIO2_PSTS	RO	Read the GPIO2 data on the pin. If this pin serves as IRQ/SMI#, this bit always indicates 0, that is, read will return 0.
1	GPIO1_PSTS	RO	Read the GPIO1 data on the pin.
0	GPIO0_PSTS	RO	Read the GPIO0 data on the pin.

INDEX A0 -- AD registers – FAN1 CONTROL v.s. TEMPERATURE 1

7.60 VT1 BOUNDARY 1 TEMPERATURE – Index A0h

Power-on default [7:0] =0011_1100b

Bit	Name	Attribute	Description
7-0	BOUND1TMP	R/W	The 1st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 segment **1** speed count registers(INDEX A4h, A5h) will be loaded into FAN1 expect count registers(INDEX 74h,75h). When VT1 temperature is **below** this boundary, FAN1 segment **2** speed count registers(INDEX A6h, A7h) will be loaded into FAN1 expect count registers(INDEX 74h,75h).

7.61 VT1 BOUNDARY 2 TEMPERATURE – Index A1h

Power-on default [7:0] =0011_0010b

Bit	Name	Attribute	Description
7-0	BOUND2TMP	R/W	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 segment **2** speed count registers(INDEX A6h, A7h) will be loaded into FAN1 expect count registers(INDEX 74h,75h). When VT1 temperature is **below** this boundary, FAN1 segment **3** speed count registers(INDEX A8h, A9h) will be loaded into FAN1

			expect count registers(INDEX 74h,75h).

7.62 VT1 BOUNDARY 3 TEMPERATURE – Index A2h

Power-on default [7:0] =0010_1000b

Bit	Name	Attribute	Description
7-0	BOUND3TMP	R/W	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 segment **3** speed count registers(INDEX A8h, A9h) will be loaded into FAN1 expect count registers(INDEX 74h,75h). When VT1 temperature is **below** this boundary, FAN1 segment **4** speed count registers(INDEX AAh, ABh) will be loaded into FAN1 expect count registers(INDEX 74h,75h).

7.63 VT1 BOUNDARY 4 TEMPERATURE – Index A3h

Power-on default [7:0] =0001_1110b

Bit	Name	Attribute	Description
7-0	BOUND4TMP	R/W	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 segment **4** speed count registers(INDEX AAh, ABh) will be loaded into FAN1 expect count registers(INDEX 74h,75h). When VT1 temperature is **below** this boundary, FAN1 segment **5** speed count registers(INDEX ACh, ADh) will be loaded into FAN1 expect count registers(INDEX 74h,75h).

7.64 FAN1 SEGMENT 1 SPEED COUNT (MSB) – Index A4h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC1SPEED (MSB)	R/W	The MSB of 1st expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed, 00h will be loaded into this register.

7.65 FAN1 SEGMENT 1 SPEED COUNT (LSB) – Index A5h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC1SPEED (LSB)	R/W	The LSB of 1st expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed, 00h will be loaded into this register.

7.66 FAN1 SEGMENT 2 SPEED COUNT (MSB) – Index A6h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC2SPEED (MSB)	R/W	The MSB of 2nd expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, the high byte of 112.5% FAN1 FULL SPEED COUND will be loaded into this register. (ie. 88% of FULL SPEED RPM)

7.67 FAN1 SEGMENT 2 SPEED COUNT (LSB) – Index A7h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC2SPEED (LSB)	R/W	The LSB of 2nd expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, the low byte of 112.5% FAN1 FULL SPEED COUND will be loaded into this register.

7.68 FAN1 SEGMENT 3 SPEED COUNT (MSB) – Index A8h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC3SPEED (MSB)	R/W	The MSB of 3rd expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, the high byte of 131.25% FAN1 FULL SPEED COUND will be loaded into this register. (ie. 76% of FULL SPEED RPM)

7.69 FAN1 SEGMENT 3 SPEED COUNT (LSB) – Index A9h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC3SPEED (LSB)	R/W	The LSB of 3rd expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, the low byte of 131.25% FAN1 FULL SPEED COUND will be loaded into this register. (ie. 76% of FULL SPEED RPM)

7.70 FAN1 SEGMENT 4 SPEED COUNT (MSB) – Index AAh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC4SPEED (MSB)	R/W	The MSB of 4th expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, the high byte of 156.25% FAN1 FULL SPEED COUND will be loaded into this register. (ie. 64% of FULL SPEED RPM)

7.71 FAN1 SEGMENT 4 SPEED COUNT (LSB) – Index ABh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC4SPEED (LSB)	R/W	The LSB of 4th expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, the low byte of 156.25% FAN1 FULL SPEED COUND will be loaded into this register. (ie. 64% of FULL SPEED RPM)

7.72 FAN1 SEGMENT 5 SPEED COUNT (MSB) – Index ACh

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	Description
7-0	SEC5SPEED (MSB)	R/W	The MSB of 5th expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, FFh will be loaded into this register.

7.73 FAN1 SEGMENT 5 SPEED COUNT (LSB) – Index ADh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC5SPEED (LSB)	R/W	The LSB of 5th expected fan speed for FAN1 in temperature mode. After detecting FAN1 full speed count, FFh will be loaded into this register.

INDEX B0 -- BD registers – FAN2 CONTROL v.s. TEMPERATURE 2

7.74 VT2 BOUNDARY 1 TEMPERATURE – Index B0h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	BOUND1TMP	R/W	The 1st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 segment **1** speed count registers(INDEX B4h, B5h) will be loaded into FAN1 expect count registers(INDEX 84h,85h). When VT2 temperature is **below** this boundary, FAN2 segment **2** speed count registers(INDEX B6h, B7h) will be loaded into FAN2 expect count registers(INDEX 84h,85h).

7.75 VT2 BOUNDARY 2 TEMPERATURE – Index B1h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	BOUND2TMP	R/W	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 segment **2** speed count registers(INDEX B6h, B7h) will be loaded into FAN2 expect count registers(INDEX 84h,85h). When VT2 temperature is **below** this boundary, FAN2 segment **3** speed count registers(INDEX B8h, B9h) will be loaded into FAN2 expect count registers(INDEX 84h,85h).

7.76 VT2 BOUNDARY 3 TEMPERATURE – Index B2h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	BOUND3TMP	R/W	The 3rd BOUNDARY temperature for VT2 in temperature mode.

			When VT2 temperature is **exceed** this boundary, FAN2 segment **3** speed count registers(INDEX B8h, B9h) will be loaded into FAN2 expect count registers(INDEX 84h,85h). When VT2 temperature is **below** this boundary, FAN2 segment **4** speed count registers(INDEX BAh, BBh) will be loaded into FAN2 expect count registers(INDEX 84h,85h).

7.77 VT2 BOUNDARY 4 TEMPERATURE – Index B3h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	BOUND4TMP	R/W	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 segment **4** speed count registers(INDEX BAh, BBh) will be loaded into FAN2 expect count registers(INDEX 84h,85h). When VT2 temperature is **below** this boundary, FAN2 segment 5 speed count registers(INDEX BCh, BDh) will be loaded into FAN2 expect count registers(INDEX 84h,85h).

7.78 FAN2 SEGMENT 1 SPEED COUNT (MSB) – Index B4h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC1SPEED (MSB)	R/W	The MSB of 1st expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed, 00h will be loaded into this register.

7.79 FAN2 SEGMENT 1 SPEED COUNT (LSB) – Index B5h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC1SPEED (LSB)	R/W	The LSB of 1st expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed, 00h will be loaded into this register.

7.80 FAN2 SEGMENT 2 SPEED COUNT (MSB) – Index B6h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC2SPEED (MSB)	R/W	The MSB of 2nd expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, the high byte of 112.5% FAN2 FULL SPEED COUND will be loaded into this register. (ie. 88% of FULL SPEED RPM)

7.81 FAN2 SEGMENT 2 SPEED COUNT (LSB) – Index B7h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC2SPEED (LSB)	R/W	The LSB of 2nd expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, the low byte of 112.5% FAN2 FULL SPEED COUND will be loaded into this register. (ie. 88% of FULL SPEED RPM)

7.82 FAN2 SEGMENT 3 SPEED COUNT (MSB) – Index B8h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC3SPEED (MSB)	R/W	The MSB of 3rd expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, the high byte of 131.25% FAN2 FULL SPEED COUND will be loaded into this register. (ie. 76% of FULL SPEED RPM)

7.83 FAN2 SEGMENT 3 SPEED COUNT (LSB) – Index B9h

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC3SPEED (LSB)	R/W	The LSB of 3rd expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, the low byte of 131.25% FAN2 FULL SPEED COUND will be loaded into this register. (ie. 76% of FULL SPEED RPM)

7.84 FAN2 SEGMENT 4 SPEED COUNT (MSB) – Index BAh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC4SPEED (MSB)	R/W	The MSB of 4th expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, the high byte of 156.25% FAN2 FULL SPEED COUND will be loaded into this register. (ie. 64% of FULL SPEED RPM)

7.85 FAN2 SEGMENT 4 SPEED COUNT (LSB) – Index BBh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC4SPEED (LSB)	R/W	The LSB of 4th expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, the low byte of 156.25% FAN2 FULL SPEED COUND will be loaded into this register. (ie. 64% of FULL SPEED RPM)

7.86 FAN2 SEGMENT 5 SPEED COUNT (MSB) – Index BCh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC5SPEED (MSB)	R/W	The MSB of 5th expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, FFh will be loaded into this register.

7.87 FAN2 SEGMENT 5 SPEED COUNT (LSB) – Index BDh

Power-on default [7:0] =0000_0000b

Bit	Name	Attribute	Description
7-0	SEC5SPEED (LSB)	R/W	The LSB of 5th expected fan speed for FAN2 in temperature mode. After detecting FAN2 full speed count, FFh will be loaded into this register.

7.88 BJTOFFSET1 (for VT1) – Index C0h

Power-on default [7:0] = AEh

Bit	Name	Attribute	Description
7-0	BJTOFFSET1	R/W	Used to adjust VT1 BJT offset.

7.89 BJTGAIN1 (for VT1) – Index C1h

Power-on default [7:0] = 04h

Bit	Name	Attribute	Description
7-5	Reserved		
4-0	BJTGAIN_CTRL1	R/W	Used to adjust VT1 BJT gain. BJTGAIN is a 23 bits control bus. 0h: BJTGAIN = 000001h 1h: BJTGAIN = 000002h 2h: BJTGAIN = 000004h 3h: BJTGAIN = 000008h 4h: BJTGAIN = 000010h (default value) 5h: BJTGAIN = 000020h 6h: BJTGAIN = 000040h 7h: BJTGAIN = 000080h 8h: BJTGAIN = 000100h : 16h: BJTGAIN = 400000h

7.90 BJTOFFSET2 (for VT2) – Index C2h

Power-on default [7:0] = AEh

Bit	Name	Attribute	Description
7-0	BJTOFFSET2	R/W	Used to adjust VT2 BJT offset.

7.91 BJTGAIN2 (for VT1) – Index C3h

Power-on default [7:0] = 04h

Bit	Name	Attribute	Description
7-3	Reserved		
4-0	BJTGAIN_CTRL2	R/W	Used to adjust VT2 BJT gain. 0h: BJTGAIN = 000001h 1h: BJTGAIN = 000002h

			2h: BJTGAIN = 000004h 3h: BJTGAIN = 000008h 4h: BJTGAIN = 000010h (default value) 5h: BJTGAIN = 000020h 6h: BJTGAIN = 000040h 7h: BJTGAIN = 000080h 8h: BJTGAIN = 000100h : 16h: BJTGAIN = 400000h

8 Electron Characteristic

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 4.0	V
Input Voltage	-0.5 to 5.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

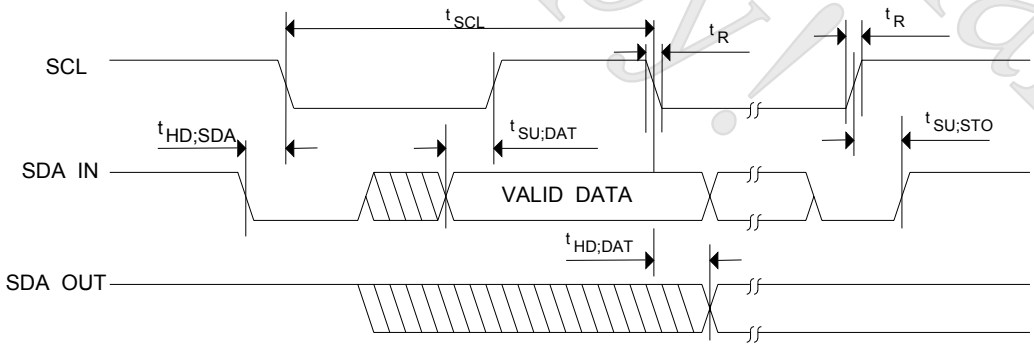
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS

I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Hysteresis	VTH	0.5	1.2		V	VDD = 3.3 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0V

7.2 DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD_{16} - Open-drain output pin with sink capability of 16 mA						
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
IN_t - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3V
Hysteresis	VTH	0.5	1.2		V	VDD = 3.3 V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V

8.3 AC Characteristics



Serial Bus Timing Diagram

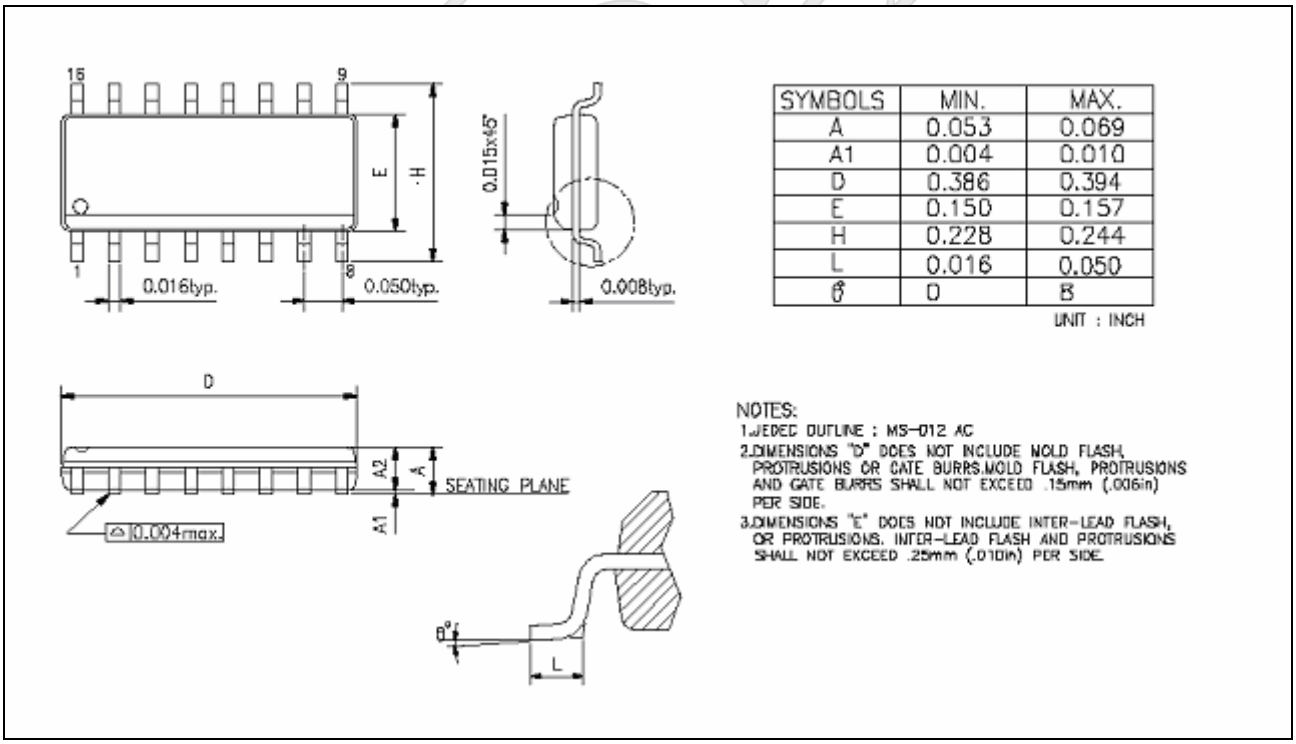
Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

9 Ordering Information

Part Number	Package Type	Production Flow
F75375S	16 PIN SOP	Commercial, 0°C to +70°C
F75375SG	16 PIN SOP(Green Package)	Commercial, 0°C to +70°C

10 Package Dimensions (16SOP 150mil)



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11 Application Circuit