SFC3.3-4
Low Voltage ChipClamp™ Flip Chip TVS Diode Array

PROTECTION PRODUCTS

Description

The SFC3.3-4 is a quad flip chip TVS diode array. They are state-of-the-art devices that utilize solid-state EPD TVS technology for superior clamping performance and DC electrical characteristics. The SFC series TVS diodes are designed to protect sensitive semiconductor components from damage or latch-up due to electrostatic discharge (ESD) and other voltage induced transient events.

The SFC3.3-4 is a 6-bump, 0.5mm pitch flip chip array with a 3x2 bump grid. It measures approximately 1.5 by 1.0 mm. It has a very low profile of < 0.65 mm. This is a crucial specification for many portable applications. Each device will protect up to four data or I/O lines. The flip chip design results in lower inductance, virtually eliminating voltage overshoot due to leads and interconnecting bond wires.

The devices are constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over silicon-avalanche diode processes.

They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Features

- 150 Watts peak pulse power (tp = 8/20μs)
- Transient protection for data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20μs)
- Small chip scale package requires less board space
- Low profile (< 0.65mm)
- No need for underfill material
- Protects four I/O or data lines
- Low clamping voltage
- Working voltage: 3.3V
- Solid-state EPD TVS technology

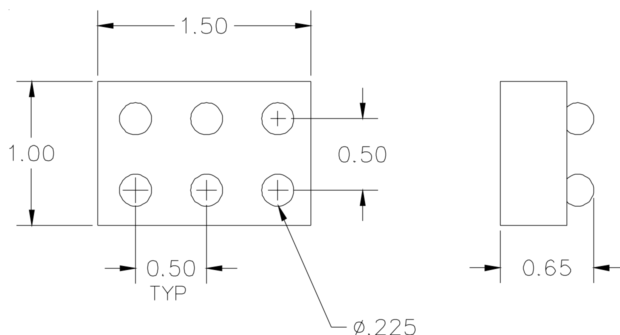
Mechanical Characteristics

- JEDEC MO-211, 0.50 mm Flip Chip Package
- Non-conductive top side coating
- Marking : Marking Code
- Packaging : Tape and Reel

Applications

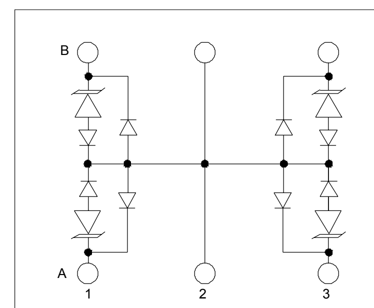
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDAs)
- Notebook and Hand Held Computers
- Portable Instrumentation
- Pagers
- Smart Cards
- MP3 Players

Device Dimensions



SFC3.3-4 Maximum Dimensions (mm)

Schematic & PIN Configuration



3 x 2 Grid Flip Chip TVS (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	150	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	15	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	>25 >15	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.5			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V, T=25°C		0.05	0.5	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs Any I/O to Ground			4.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs Any I/O to Ground			6.8	V
Clamping Voltage	V_C	I_{PP} = 15A, tp = 8/20µs Any I/O to Ground			9.5	V
Forward Clamping Voltage	V_F	I_{PP} = 1A, tp = 8/20µs Ground to any I/O			1.7	V
Junction Capacitance	C_j	Each I/O pin and Ground V_R = 0V, f = 1MHz		75	100	pF

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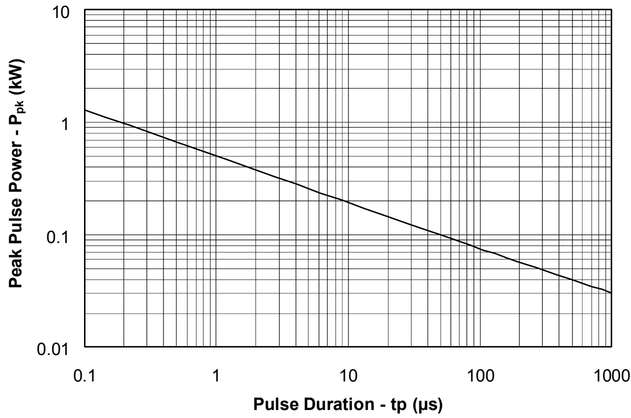
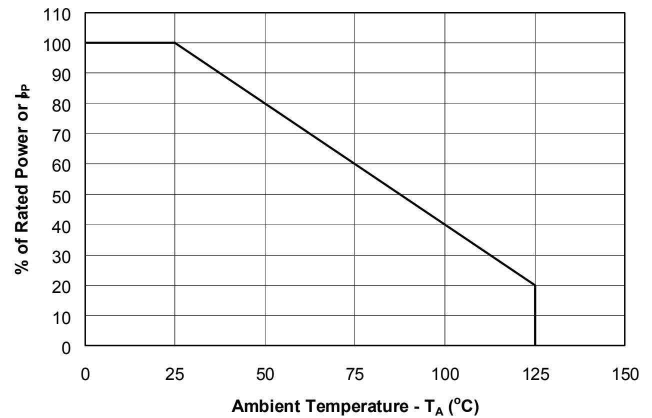
Typical Characteristics

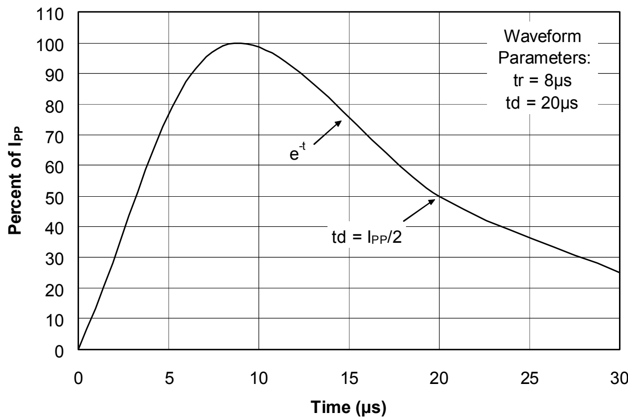
Non-Repetitive Peak Pulse Power vs. Pulse Time



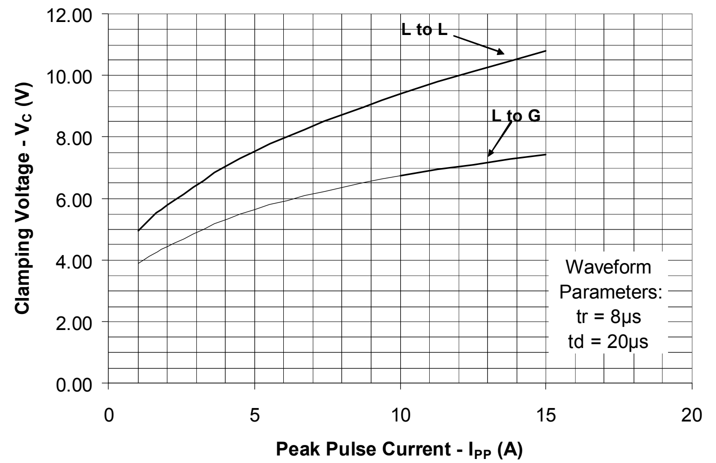
Power Derating Curve



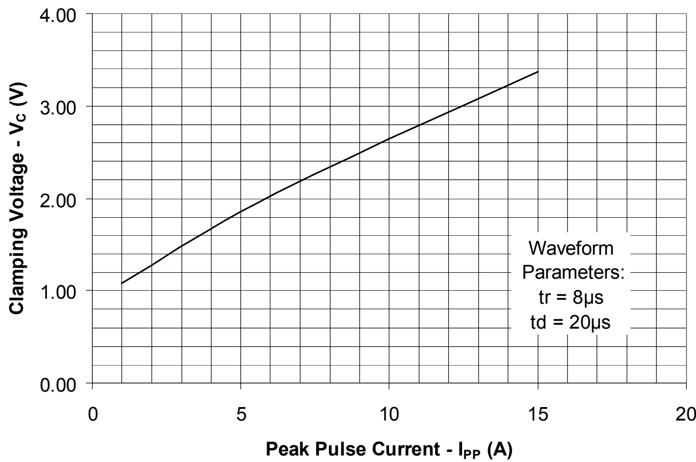
Pulse Waveform



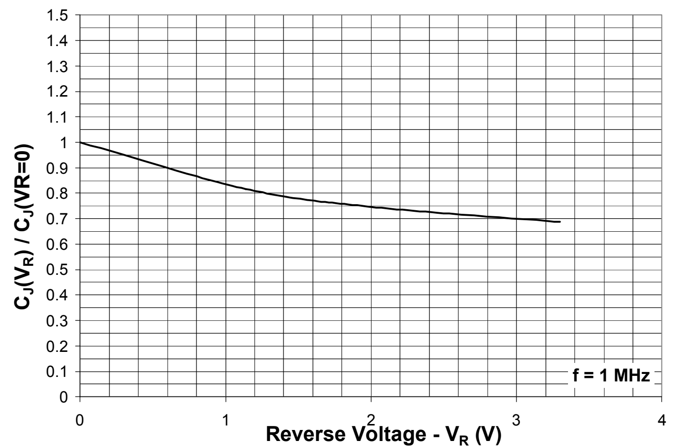
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Normalized Junction Capacitance vs. Reverse Voltage



Applications Information

Device Connection Options

The SFC3.3-4 has solder bumps located in a 3 x 2 matrix layout on the active side of the device. The bumps are designated by the numbers 1 - 3 along the horizontal axis and letters A - B along the vertical axis. The lines to be protected are connected at bumps A1, B1, A3, and B3. Bumps A2 and B2 are connected to ground. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.
Due to the “snap-back” characteristics of the low voltage TVS, it is not recommended that any of the I/O bumps be directly connected to a DC source greater than snap-back votlage (V_{SB}) as the device can latch on as described the EPD TVS characteristics section.

Flip Chip TVS

Flip chip TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. They are compatible with current pick and place equipment further reducing manufacturing costs. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

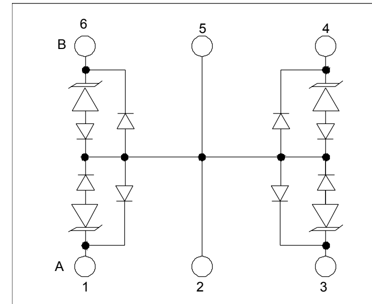
Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the SFC3.3-4. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.225 ± 0.010 mm with a solder mask opening of 0.350 ± 0.025 mm.

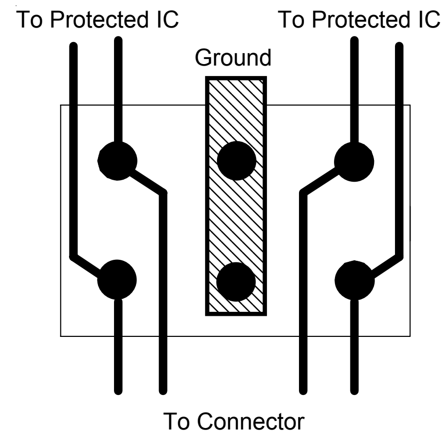
Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems

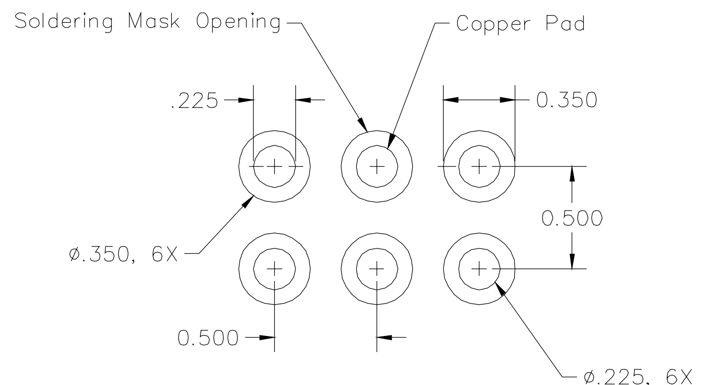
Device Schematic and Pin Configuration



Layout Example



NSMD Package Footprint



and should be avoided.

Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mm thick, laser cut, electro-polished stencil with 0.275mm square apertures and rounded corners is recommended.

Reflow Profile

The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020 for assembly of small body components. During reflow, the component will self-align itself on the pad.

EPD TVS Characteristics

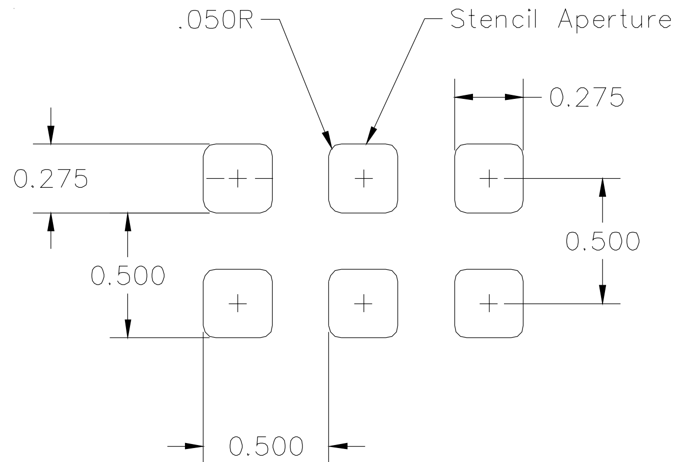
The SFC3.3-4 is constructed using Semtech's proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the SFC3.3-4 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex nppn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. Since the EPD TVS devices use a 4-layer structure, they exhibit a slightly different IV characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (V_{RWM}). During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage (V_{PT}) is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

When the TVS is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristics due to its structures. This point is defined on the curve by the snap-back voltage (V_{SB}) and snap-back current (I_{SB}). To return to a non-conducting state, the current through the device must fall below the I_{SB} (approximately <50mA) and the voltage must fall below the V_{SB} (normally 2.8 volts for a 3.3V device). If a 3.3V TVS is connected to 3.3V DC source, it will never fall below the snap-back voltage of 2.8V and will therefore stay in a conducting state.

The SFC3.3-4 is the first device to combine the advantages of flip chip technology with those of the EPD process technology.

Stencil Design



Assembly Guideline for Pb-Free Soldering

The following are recommendations for the assembly of this device:

Assembly Parameter	Recommendation
Solder Ball Composition	95.5Sn/3.8Ag/0.7Cu
Solder Stencil Design	Same as the SnPb design
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Composition	Sn Ag (3-4) Cu (0.5-0.9)
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	per JEDEC J-STD-020
PCB Solder Pad Design	Same as the SnPb Design
PCB Pad Finish	OSP or AuNi

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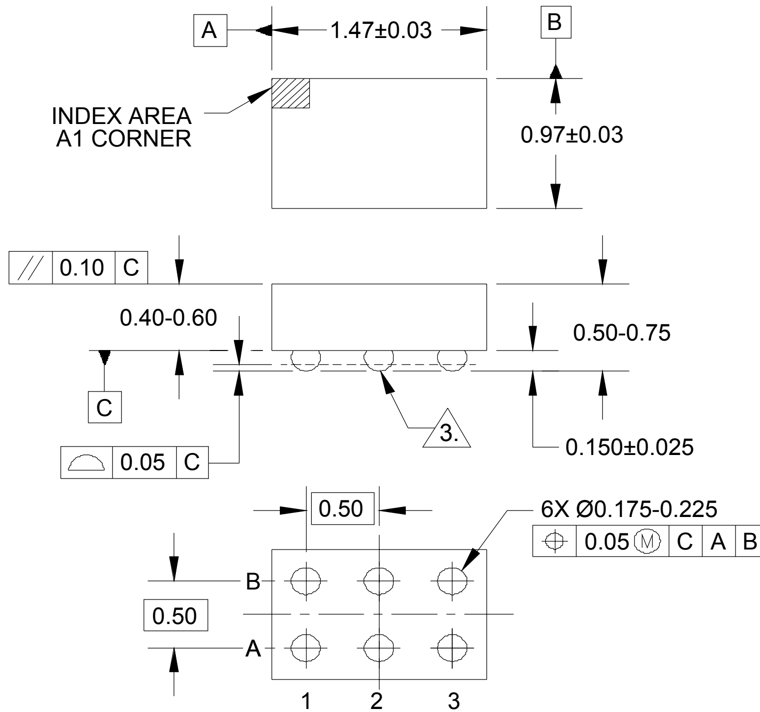
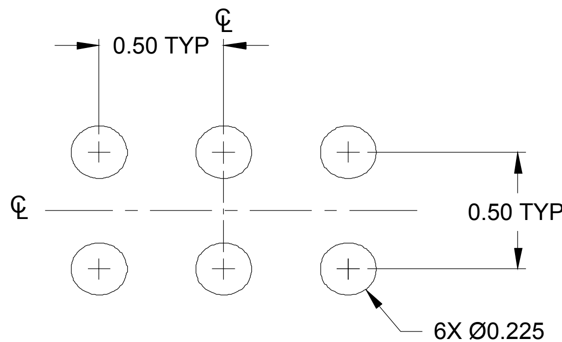
Outline Drawing - 3x2 Grid Flip Chip



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC REGISTRATION MO-211.
3. Sn95.5/Ag3.8/Cu0.7 FOR Pb-FREE DEVICES.

Land Pattern - 3x2 Grid Flip Chip



NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

PROTECTION PRODUCTS

Marking Codes

Part Number	Marking Code
SFC3.3-4	F43U

Top Coating: The top (non-bump side) of the device is a black non-conductive coating. This material is compliant with UL 94V-0 flammability requirements.

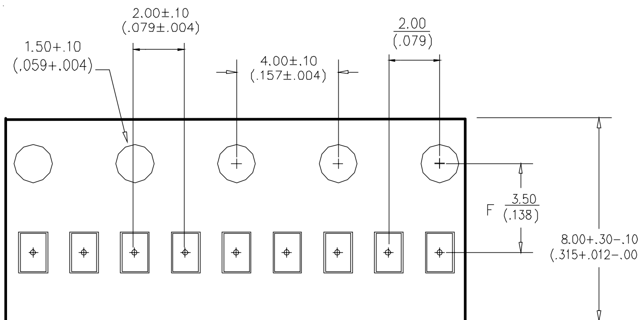
Ordering Information

Part Number	Pitch Option	Qty per Reel	Reel Size
SFC3.3-4.BCT [1]	2mm	3,000	7 Inch

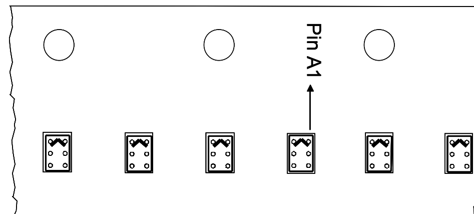
Notes
(1) Lead Free Solder Balls

ChipClamp is a mark of Semtech Corporation

Tape and Reel Specification



Tape Specifications



Device Orientation

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