Arasan
The Bus Stops Here

Actel
CompanionCore

PRODUCT OVERVIEW

Features

- Low-power Actel AGL600-FG256 IGLOO family FPGA
- Micro-SD connector for Micro-SD memory modules
- SD/MMC Connector for SD, MMC4, RS-MMC, Mini-SD, MMC Plus, RS MMC Plus cards
- On-board power regulators for 3.3 V and 1.2/1.5 V core power
- Interfaces with Marvell Littleton PXA3xx VLIO interface using JAE 160-pin connectors
- Flash*Freeze™ demonstration functionality
- FLASHPRO JTAG connector for programming
- Capability to measure current for individual I/O banks and core
- Meets SD Host Controller specification Version 2.0 Part A2
- Meets SDIO card v2.0 specification
- Supports Embedded SDIO Specification Version 0.92 Draft
- Supports Test Register to generate events by software
- Supports high-capacity Ver2.00 Card
- Supports non-DMA, SDMA, ADMA1, and ADMA2 modes
- Meets MMC specifications version 3.31 and 4.2
- Supports MMCplus, MMCmobile
- Meets CE-ATA Digital Protocol revision 1.1RC
- Up to 200 Mbps with 4 parallel SD data lines and 416 Mbps with 8 parallel MMC 4.2 data lines
- Supports CE-ATA Digital Protocol commands (CMD39/CMD60/CMD61)
- Host clock rate from 0 to 52 MHz
- CRC7 and CRC16 modules
- Supports direct R/W (IO52) and extended R/W (IO53) commands
- Supports Read Wait Control, Suspend/Resume operations

Storage Solution for Marvell's PXA300/310 Platform

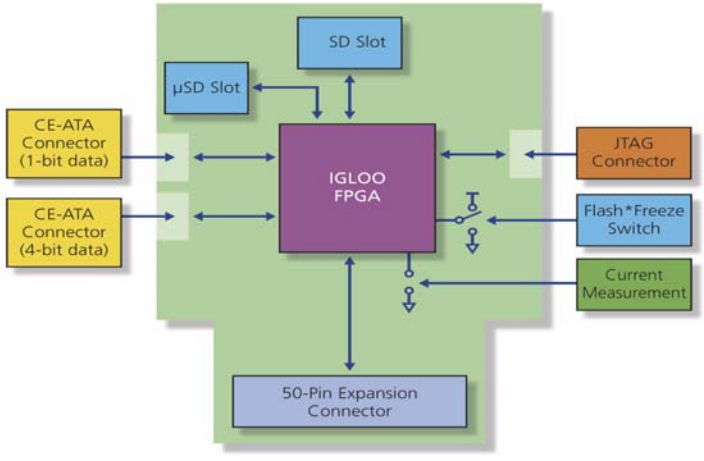
Overview

The SD2.0/MMC4.2/CE-ATA storage solution has been developed in cooperation with ARASAN Chip Systems for Actel AGL600-FG256 low-power IGLOO FPGA. The Actel IGLOO family of reprogrammable, full-featured flash FPGAs is designed to meet the demanding power and area requirements of today's portable electronics. Based on the Actel nonvolatile flash technology and single-chip ProASIC®3 FPGA architecture, the 1.2 V / 1.5 V operating voltage family offers the industry's lowest power consumption - as low as 5 µW.

The storage daughter board interfaces with Marvell's PXA300/310 processor through the data flash interface (DFI). Arasan SD2.0/MMC4.2/CE-ATA Host IP core in the Actel IGLOO device provides a low-cost and low-power solution.

The Arasan SD2.0/MMC4.2/CE-ATA (CE-ATA 2) Host Controller core consists of the SD 2.0, SDIO 2.0, MMC4.2, and CE-ATA 1.1 controllers. The Arasan CE-ATA 2 Host is fully compliant with the SD Host specification version 2.0 with Advanced-DMA support, MMC specification version 4.2, and CE-ATA Digital Protocol revision 1.1RC. It supports SPI, SD 1-bit, SD 4-bit, and MMC 8-bit modes. The CE-ATA 2 Host core is designed to support high-speed and full-speed SD data transfers. In application with an AHB interface, the Arasan CE-ATA 2 Host core communicates with the ARM® processor at a clock speed up to 300 MHz. The CE-ATA 2 Host controller includes a DMA controller and a FIFO that is expandable from a minimum size of 4 x 32-bit. An optional CPRM functional block can be incorporated to perform a Cipher algorithm for encryption and decryption.

The Storage Solution Functional Block Diagram



Version 1.0

SD 2.0 Compliant
SDIO 2.0 Compliant

MMC 4.2 compliant

CE-ATA 1.1 compliant

Storage Solution for Marvell's PXA300/310 Platform

SD/SDIO Bus Interface Unit:

SD 2.0, SDIO 1.2, MMC3.31, MMC4.2, and CE-ATA devices communicate with the host controller through the SD/MMC Bus Interface Unit (BIU). The BIU consists of the Command Decoder, Response Generator, Transmitter/Receiver, and Power Control/Switch units. SD1, SD4, and SPI modes are supported. Other BIU functions include the 16-bit CRC generator and checker for the data lines, 7-bit CRC generator and checker for the command and response lines, interrupt state machine, and BIU Master state machine.

Advanced DMA:

The controller supports SDMA, ADMA1, and ADMA2. The Single Operation DMA (SDMA) algorithm forms a performance bottleneck by interruption at every page boundary. ADMA adopts the scatter-gather DMA algorithm so that higher data transfer speed is available. ADMA provides data transfer between system memory and the SD card without interruption of CPU execution. ADMA can support both 32-bit and 64-bit system memory addressing. ADMA1 can support data transfer of only 4 KB aligned data in system memory. ADMA2 improves the restriction so that data of any location and any size can be transferred in system memory.

AHB/APB Interface:

The Arasan SD2.0/MMC4.2/CE-ATA Host core provides a Programmed I/O method in which the ARM host driver transfers data using the Buffer Data Port register. The AHB Slave has direct access to the Host Control registers and these registers can be programmed by the ARM processor through the AHB Slave interface. Data transactions are performed through the AHB Slave interface with the Programmed I/O method. The AHB Interface initiates a read or write transaction with the memory if the data transaction is a DMA data transfer.

MMC4.2/CE-ATA Interface:

The MMC interface conforms with the MMC system specification 4.2. It supports 8-bit MMC mode, Error Correction Code (ECC), MMCplus and MMCmobile card types. The CE-ATA Host Controller conforms with CE-ATA Digital Protocol revision 1.1RC, and with support for CE-ATA Digital Protocol commands (CMD39 /CMD60 / CMD61). The CE-ATA interface allows for lower pin count, better power utilization, voltages tailored to battery-based applications, and more efficient command protocol.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- ReUse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Items:

- SD/SDIO Host Validation Platform
- SDIO Device Development Board
- SD/MMC/CE-ATA WinCE stack

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux, and Windows® XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

About Arasan:

Arasan Chip Systems, Inc. founded in 1995, is a leading supplier of Reusable Intellectual Property (IP) cores, semiconductors, and electronic design services. Arasan's product portfolio is focused on Bus Interfaces and includes IP for MIPI, USB 1.1 and USB 2.0, PCI, SDIO, and CE-ATA technologies. Arasan is headquartered in San Jose, California, with design centers in India and support options available in Taiwan, China, and Europe.

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Data Sheet Links:

SD/MMC4.2/CE-ATA Host Core:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit: www.arasan.com